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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

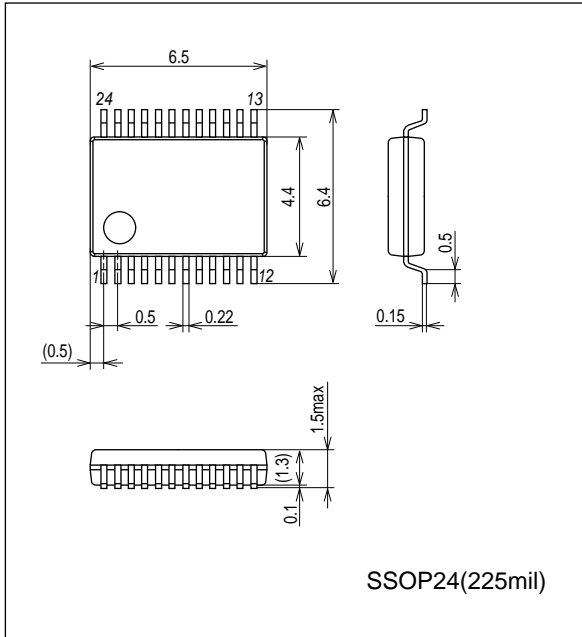
#### Details

Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOP (0.236", 6.00mm Width)
Supplier Device Package	24-MFPSJ
Purchase URL	<a href="https://www.e-xfl.com/product-detail/onsemi/lc87f2g08au-ssop-e">https://www.e-xfl.com/product-detail/onsemi/lc87f2g08au-ssop-e</a>

# LC87F2G08A

## Package Dimensions

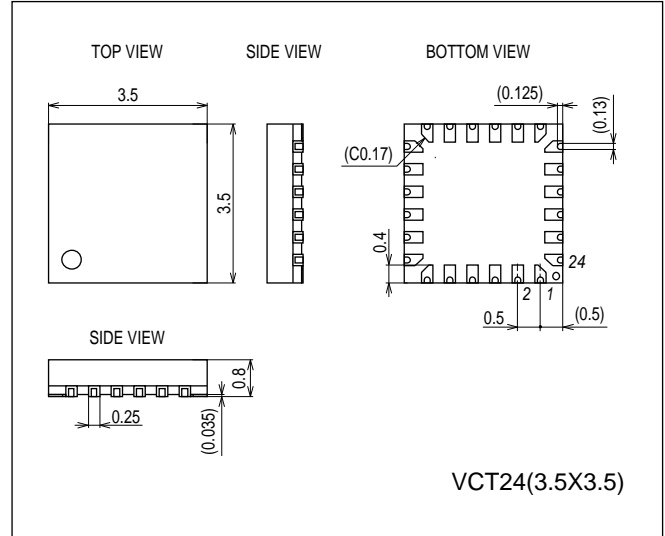
unit : mm (typ)  
3287



## Package Dimensions

unit : mm (typ)  
3322A

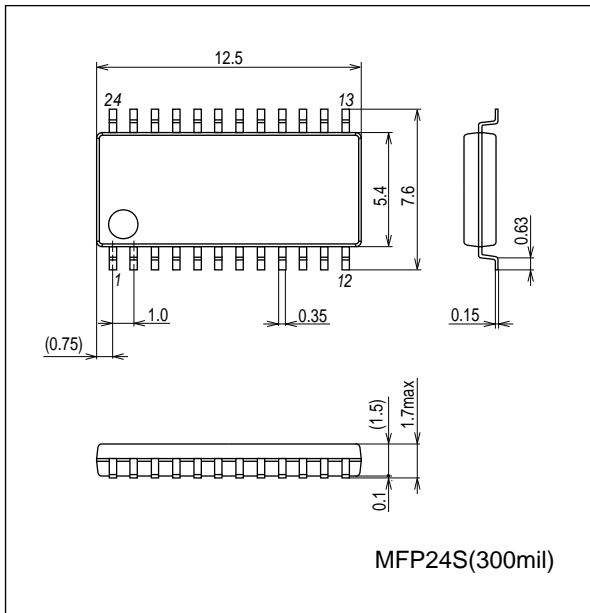
(Build-to-order)



## Package Dimensions

unit : mm (typ)  
3112B

(Discontinued)



### ■ Minimum Bus Cycle

- 83.3ns (12MHz at  $V_{DD}=2.7V$  to 5.5V)
- 100ns (10MHz at  $V_{DD}=2.2V$  to 5.5V)
- 250ns (4MHz at  $V_{DD}=1.8V$  to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

### ■ Minimum Instruction Cycle Time

- 250ns (12MHz at  $V_{DD}=2.7V$  to 5.5V)
- 300ns (10MHz at  $V_{DD}=2.2V$  to 5.5V)
- 750ns (4MHz at  $V_{DD}=1.8V$  to 5.5V)

**■ Ports**

- Normal withstand voltage I/O ports
  - Ports I/O direction can be designated in 1-bit units 11 (P1n, P20, P21, P70)
  - Ports I/O direction can be designated in 4-bit units 8 (P0n)
- Dedicated oscillator ports/input ports 2 (CF1/XT1, CF2/XT2)
- Reset pin 1 ( $\overline{\text{RES}}$ )
- Power pins 2 ( $V_{SS1}$ ,  $V_{DD1}$ )

**■ Timers**

- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)  $\times$  2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler  $\times$  2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)  
(toggle outputs also possible from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)  
(The lower-order 8 bits can be used as PWM)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  - 2) Interrupts are programmable in 5 different time schemes

**■ High-Speed Clock Counter**

- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- Can generate output real time.

**■ SIO**

- SIO0: 8-bit Synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3tCYC)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

**■ UART**

- Full Duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

**■ AD Converter: 12 bits/8 bits  $\times$  8 channels**

- 12 bits/8 bits AD converter resolution selectable

**■ Remote Control Receiver Circuit (sharing pins with P15, SCK1, INT3, and T0IN)**

- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

**■Clock Output Function**

- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

**■Watchdog Timer**

- External RC watchdog timer
- Interrupt and reset signals selectable

**■Interrupts**

- 18 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0

- Priority levels  $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

**■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)****■High-speed Multiplication/Division Instructions**

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits  $\times$  16 bits (12 tCYC execution time)
- 16 bits  $\div$  8 bits (8 tCYC execution time)
- 24 bits  $\div$  16 bits (12 tCYC execution time)

**■Oscillation Circuits**

- Internal oscillation circuits
  - Low-speed RC oscillation circuit : For system clock (100kHz)
  - Medium-speed RC oscillation circuit : For system clock (1MHz)
  - Multifrequency RC oscillation circuit : For system clock (8MHz)
- External oscillation circuits
  - Hi-speed CF oscillation circuit: For system clock, with internal Rf
  - Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf
  - 1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  - 2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

**■System Clock Divider Function**

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2 $\mu$ s, 2.4 $\mu$ s, 4.8 $\mu$ s, 9.6 $\mu$ s, 19.2 $\mu$ s, 38.4 $\mu$ s, and 76.8 $\mu$ s (at a main clock rate of 10MHz).

## ■Internal Reset Function

- Power-on reset (POR) function
  - 1) POR reset is generated only at power-on time.
  - 2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  - 2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

## ■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
    - 1) Oscillation is not halted automatically.
    - 2) There are three ways of resetting the HALT mode.
      - (1) Setting the reset pin to the low level
      - (2) System resetting by watchdog timer or low-voltage detection
      - (3) Occurrence of an interrupt
  - HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
    - 1) The CF, RC, and crystal oscillators automatically stop operation.
    - 2) There are four ways of resetting the HOLD mode.
      - (1) Setting the reset pin to the lower level.
      - (2) System resetting by watchdog timer or low-voltage detection
      - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4
        - \* INT0 and INT1 HOLD mode reset is available only when level detection is set.
      - (4) Having an interrupt source established at port 0.
  - X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
    - 1) The CF and RC oscillators automatically stop operation.
    - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
    - 3) There are five ways of resetting the X'tal HOLD mode.
      - (1) Setting the reset pin to the low level.
      - (2) System resetting by watchdog timer or low-voltage detection.
      - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4
        - \* INT0 and INT1 HOLD mode reset is available only when level detection is set.
      - (4) Having an interrupt source established at port 0.
      - (5) Having an interrupt source established in the base timer circuit.
- Note: Available only when X'tal oscillation is selected.

## ■Onchip Debugger

- Supports software debugging with the IC mounted on the target board.
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.  
DBGP0 (P0), DBGP1 (P1)

## ■Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.  
Note: This data security function does not necessarily provide absolute data security.

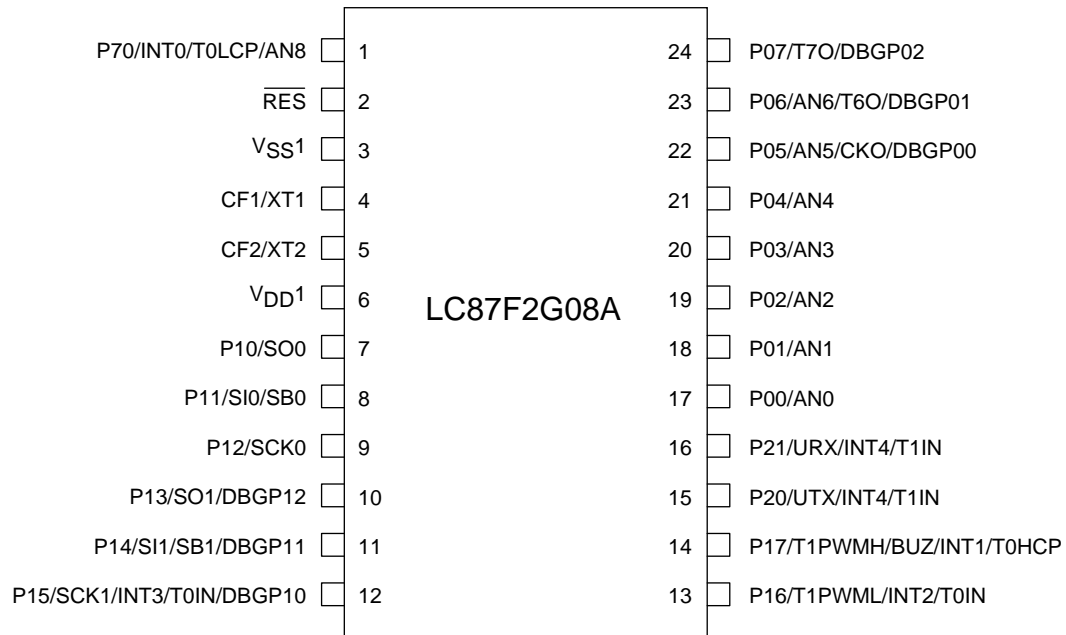
## ■Development Tools

- On-chip debugger: (1) TCB87 type B + LC87D2G08A  
(2) TCB87 TypeB + LC87F2G08A  
(3) TCB87 TypeC (3 wire version) + LC87D2G08A  
(4) TCB87 TypeC (3 wire version) + LC87F2G08A

Note: LC87F2G08A has an On-chip debugger but its function is limited.

# LC87F2G08A

## Pin Assignment



Top view

MFP24S (300mil) "Lead-free Type"

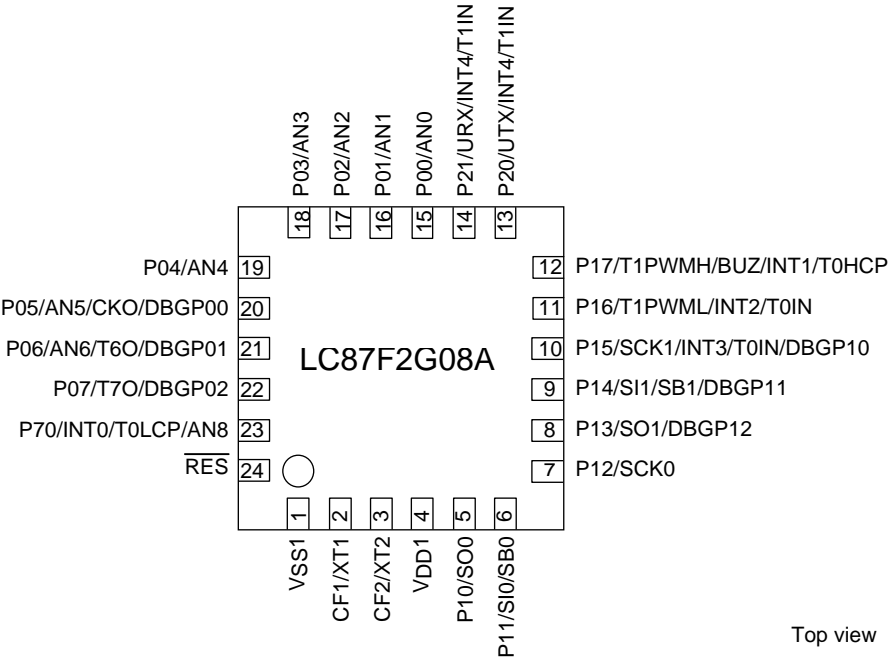
MFP24SJ (300mil) "Lead-/Halogen-free Type"

SSOP24 (225mil) "Lead-free Type"

MFP24S/ MFP24SJ/ SSOP24	NAME
1	P70/INT0/T0LCP/AN8
2	RES
3	VSS1
4	CF1/XT1
5	CF2/XT2
6	VDD1
7	P10/SO0
8	P11/SI0/SB0
9	P12/SCK0
10	P13/SO1/DBGP12
11	P14/SI1/SB1/DBGP11
12	P15/SCK1/INT3/T0IN/DBGP10

MFP24S/ MFP24SJ/ SSOP24	NAME
13	P16/T1PWML/INT2/T0IN
14	P17/T1PWMH/BUZ/INT1/T0HCP
15	P20/UTX/INT4/T1IN
16	P21/URX/INT4/T1IN
17	P00/AN0
18	P01/AN1
19	P02/AN2
20	P03/AN3
21	P04/AN4
22	P05/AN5/CKO/DBGP00
23	P06/AN6/T6O/DBGP01
24	P07/T7O/DBGP02

LC87F2G08A

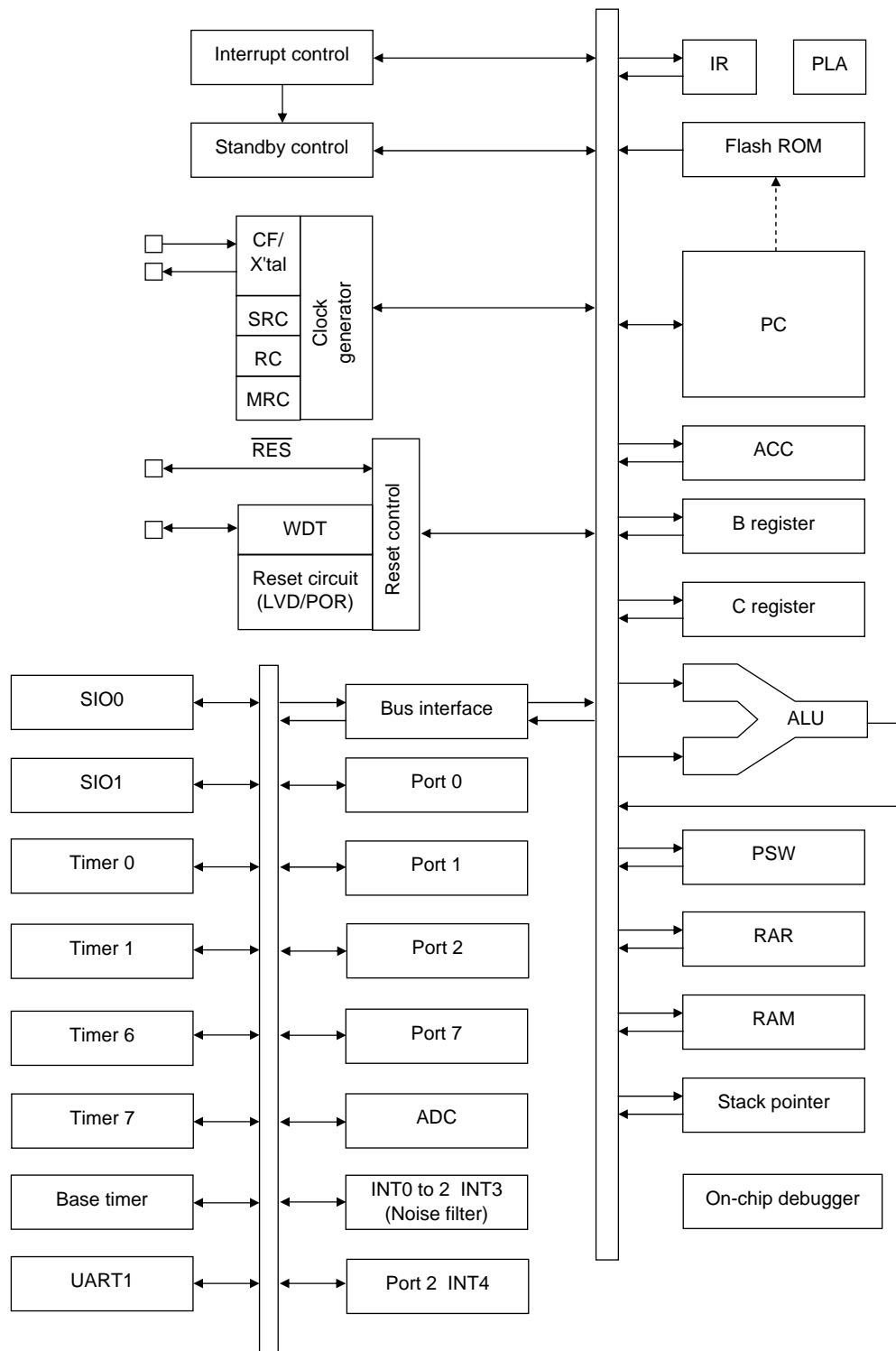


VCT24(3.5×3.5) “Lead-/Halogen-free Type” (build-to-order)

VCT24	NAME
1	VSS1
2	CF1/XT1
3	CF2/XT2
4	VDD1
5	P10/SO0
6	P11/SI0/SB0
7	P12/SCK0
8	P13/SO1/DBGP12
9	P14/SI1/SB1/DBGP11
10	P15/SCK1/INT3/T0IN/DBGP10
11	P16/T1PWML/INT2/T0IN
12	P17/T1PWMH/BUZ/INT1/T0HCP

VCT24	NAME
13	P20/UTX/INT4/T1IN
14	P21/URX/INT4/T1IN
15	P00/AN0
16	P01/AN1
17	P02/AN2
18	P03/AN3
19	P04/AN4
20	P05/AN5/CKO/DBGP00
21	P06/AN6/T6O/DBGP01
22	P07/T7O/DBGP02
23	P70/INT0/T0LCP/AN8
24	RES

# System Block Diagram





## LC87F2G08A

Continued from preceding page.

Continued from preceding page.

Pin Name	I/O	Description	Option												
Port 7	I/O	<ul style="list-style-type: none"><li>• 1-bit I/O port</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions</li></ul> <p>P70: INT0 input / HOLD reset input / timer 0L capture input / watchdog timer output</p> <p>P70(AN8): AD converter input</p> <p>Interrupt acknowledge types</p> <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising &amp; Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr></table>		Rising	Falling	Rising & Falling	H level	L level	INT0	enable	enable	disable	enable	enable	No
			Rising	Falling	Rising & Falling	H level	L level								
INT0			enable	enable	disable	enable	enable								
P70															
RES	I/O	External reset input / internal reset output	No												
CF1/XT1	I	<ul style="list-style-type: none"><li>• Ceramic resonator or 32.768kHz crystal oscillator input pin</li><li>• Pin function</li></ul> <p>General-purpose input port</p>	No												
CF2/XT2	I/O	<ul style="list-style-type: none"><li>• Ceramic resonator or 32.768kHz crystal oscillator output pin</li><li>• Pin function</li></ul> <p>General-purpose input port</p>	No												

### Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

# LC87F2G08A

**Allowable Operating Conditions** at Ta = -40°C to +85°C, V<sub>SS</sub>1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	V <sub>DD</sub> (1)	V <sub>DD</sub> 1	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	V
	V <sub>DD</sub> (2)		0.294μs ≤ tCYC ≤ 200μs		2.2		5.5	
	V <sub>DD</sub> (3)		0.735μs ≤ tCYC ≤ 200μs		1.8		5.5	
Memory sustaining supply voltage	V <sub>HD</sub>	V <sub>DD</sub> 1	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	V <sub>IH</sub> (1)	Ports 1, 2, P70 port input/ interrupt side		1.8 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	Ports 0		1.8 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	Port 70 watchdog timer side		1.8 to 5.5	0.9V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	CF1, RES		1.8 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
Low level input voltage	V <sub>IL</sub> (1)	Ports 1, 2, P70 port input/ interrupt side		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
				1.8 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	Ports 0		4.0 to 5.5	V <sub>SS</sub>		0.15V <sub>DD</sub> +0.4	
				1.8 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (3)	Port 70 watchdog timer side		1.8 to 5.5	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0	
	V <sub>IL</sub> (4)	CF1, RES		1.8 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	μs
				2.2 to 5.5	0.294		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open	2.7 to 5.5	0.1		12	MHz
			• System clock frequency division ratio=1/1	1.8 to 5.5	0.1		4	
			• External system clock duty=50±5%					
			• CF2 pin open	3.0 to 5.5	0.2		24.4	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• System clock frequency division ratio=1/2	2.0 to 5.5	0.2		8	MHz
			• External system clock duty=50±5%					
	FmCF(2)	CF1, CF2	12MHz ceramic oscillation. See Fig. 1.	2.7 to 5.5		12		
	FmCF(3)	CF1, CF2	10MHz ceramic oscillation. See Fig. 1.	2.2 to 5.5		10		
			4MHz ceramic oscillation. CF oscillation normal amplifier size selected. (CFLAMP=0) See Fig. 1.	1.8 to 5.5		4		
			4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	2.2 to 5.5		4		
	FmMRC		Frequency variable RC oscillation. 1/2 frequency division ration. (RCCTD=0) (Note 2-4)	2.7 to 5.5	7.44	8.0	8.56	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	1.8 to 5.5	50	100	200	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100μs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

# LC87F2G08A

**Electrical Characteristics** at Ta = -40°C to +85°C, V<sub>SS</sub>1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2, P70, $\overline{\text{RES}}$	Output disabled Pull-up resistor off V <sub>IN</sub> =V <sub>DD</sub> (Including output Tr's off leakage current)	1.8 to 5.5			1	$\mu\text{A}$
	I <sub>IH</sub> (2)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	1.8 to 5.5			15	
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2, P70, $\overline{\text{RES}}$	Output disabled Pull-up resistor off V <sub>IN</sub> =V <sub>SS</sub> (Including output Tr's off leakage current)	1.8 to 5.5	-1			$\mu\text{A}$
	I <sub>IL</sub> (2)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	1.8 to 5.5	-15			
High level output voltage	V <sub>OH</sub> (1)	Ports 0, 1, 2	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			V
	V <sub>OH</sub> (2)		I <sub>OH</sub> =-0.35mA	2.7 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)		I <sub>OH</sub> =-0.15mA	1.8 to 5.5	V <sub>DD</sub> -0.4			
Low level output voltage	V <sub>OL</sub> (1)	Ports 0, 1, 2	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (2)		I <sub>OL</sub> =1.4mA	2.7 to 5.5			0.4	
	V <sub>OL</sub> (3)		I <sub>OL</sub> =0.8mA	1.8 to 5.5			0.4	
	V <sub>OL</sub> (4)	P70	I <sub>OL</sub> =1.4mA	2.7 to 5.5			0.4	
	V <sub>OL</sub> (5)		I <sub>OL</sub> =0.8mA	1.8 to 5.5			0.4	
	V <sub>OL</sub> (6)	P00, P01	I <sub>OL</sub> =25mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (7)		I <sub>OL</sub> =4mA	2.7 to 5.5			0.4	
	V <sub>OL</sub> (8)		I <sub>OL</sub> =2mA	1.8 to 5.5			0.4	
Pull-up resistance	R <sub>pu</sub> (1)	Ports 0, 1, 2 P70	V <sub>OH</sub> =0.9V <sub>DD</sub> When Port 0 selected low-impedance pull-up.	4.5 to 5.5	15	35	80	k $\Omega$
	R <sub>pu</sub> (2)			1.8 to 4.5	18	50	230	
	R <sub>pu</sub> (3)	Port 0	V <sub>OH</sub> =0.9V <sub>DD</sub> When Port 0 selected high-impedance pull-up.	1.8 to 5.5	100	210	400	
Hysteresis voltage	V <sub>HYS</sub> (1)	Ports 1, 2, P70, $\overline{\text{RES}}$		2.7 to 5.5		0.1V <sub>DD</sub>		V
	V <sub>HYS</sub> (2)			1.8 to 2.7		0.07V <sub>DD</sub>		
Pin capacitance	CP	All pins	For pins other than that under test: V <sub>IN</sub> =V <sub>SS</sub> f=1MHz Ta=25°C	1.8 to 5.5		10		pF

# LC87F2G08A

**Serial I/O Characteristics** at Ta = -40°C to +85°C, VSS1 = 0V

## 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SB0(P11), SIO(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			μs
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-2)	1.8 to 5.5			(1/3)tCYC +0.08	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-2)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-2)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), S11(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			μs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	1.8 to 5.5			(1/3)tCYC +0.08	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

# LC87F2G08A

**Pulse Input Conditions** at Ta = -40°C to +85°C, V<sub>SS</sub>1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P17), INT2(P16), INT4(P20 to P21)	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 or 1 are enabled.</li> </ul>	1.8 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	1.8 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	1.8 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P15) when noise filter time constant is 1/128	<ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>	1.8 to 5.5	256			
	tPIL(5)	$\overline{\text{RES}}$	<ul style="list-style-type: none"> <li>Resetting is enabled.</li> </ul>	1.8 to 5.5	200			μs

## LC87F2G08A

### Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, V<sub>SS</sub>1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification			
					min	typ	max	unit
POR release voltage	PORRL		<ul style="list-style-type: none"> <li>Select from option. (Note 7-1)</li> </ul>	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		<ul style="list-style-type: none"> <li>See Fig. 7. (Note 7-2)</li> </ul>			0.7	0.95	
Power supply rise time	PORIS		<ul style="list-style-type: none"> <li>Power supply rise time from 0V to 1.6V.</li> </ul>				100	ms

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

### Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, V<sub>SS</sub>1=0V

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification			
					min	typ	max	unit
LVD reset voltage (Note 8-2)	LVDET		<ul style="list-style-type: none"> <li>Select from option. (Note 8-1) (Note 8-3)</li> <li>See Fig. 8.</li> </ul>	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD hysteresys width	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		<ul style="list-style-type: none"> <li>See Fig. 8. (Note 8-4)</li> </ul>			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		<ul style="list-style-type: none"> <li>LVDET-0.5V</li> <li>See Fig. 9.</li> </ul>		0.2			ms

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

# LC87F2G08A

## Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	V <sub>DD</sub> 1	<ul style="list-style-type: none"><li>• FmCF=12MHz ceramic oscillation mode</li><li>• System clock set to 12MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	2.7 to 5.5		7.4	13.0	mA
			<ul style="list-style-type: none"><li>• FmCF=12MHz ceramic oscillation mode</li><li>• System clock set to 12MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	2.7 to 3.6		4.4	8.1	
	IDDOP(2)		<ul style="list-style-type: none"><li>• CF1=24MHz external clock</li><li>• System clock set to CF1 side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li></ul>	3.0 to 5.5		9.7	16.2	
			<ul style="list-style-type: none"><li>• CF1=24MHz external clock</li><li>• System clock set to CF1 side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li></ul>	3.0 to 3.6		5.3	8.7	
	IDDOP(3)		<ul style="list-style-type: none"><li>• FmCF=10MHz ceramic oscillation mode</li><li>• System clock set to 10MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	2.2 to 5.5		6.6	11.9	
			<ul style="list-style-type: none"><li>• FmCF=10MHz ceramic oscillation mode</li><li>• System clock set to 10MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	2.2 to 3.6		4.0	7.4	
	IDDOP(4)		<ul style="list-style-type: none"><li>• FmCF=4MHz ceramic oscillation mode</li><li>• System clock set to 4MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	1.8 to 5.5		2.9	6.5	
			<ul style="list-style-type: none"><li>• FmCF=4MHz ceramic oscillation mode</li><li>• System clock set to 4MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	1.8 to 3.6		2.2	4.2	
	IDDOP(5)		<ul style="list-style-type: none"><li>• CF oscillation low amplifier size selected. (CFLAMP=1)</li><li>• FmCF=4MHz ceramic oscillation mode</li><li>• System clock set to 4MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/4 frequency division ratio</li></ul>	2.2 to 5.5		1.1	2.5	
			<ul style="list-style-type: none"><li>• CF oscillation low amplifier size selected. (CFLAMP=1)</li><li>• FmCF=4MHz ceramic oscillation mode</li><li>• System clock set to 4MHz side</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/4 frequency division ratio</li></ul>	2.2 to 3.6		0.6	1.3	
	IDDOP(6)		<ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Internal low speed RC oscillation stopped.</li><li>• System clock set to internal medium speed RC oscillation.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li></ul>	1.8 to 5.5		0.6	1.7	
			<ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Internal low speed RC oscillation stopped.</li><li>• System clock set to internal medium speed RC oscillation.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li></ul>	1.8 to 3.6		0.3	0.9	
	IDDOP(7)		<ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• System clock set to 8MHz with frequency variable RC oscillation</li><li>• 1/1 frequency division ratio</li></ul>	2.7 to 5.5		5.0	9.1	
			<ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Internal low speed and medium speed RC oscillation stopped.</li><li>• System clock set to 8MHz with frequency variable RC oscillation</li><li>• 1/1 frequency division ratio</li></ul>	2.7 to 3.6		3.6	5.8	
	IDDOP(8)		<ul style="list-style-type: none"><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal low speed RC oscillation.</li><li>• Internal medium speed RC oscillation sopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	1.8 to 5.5		75	370	μA
			<ul style="list-style-type: none"><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal low speed RC oscillation.</li><li>• Internal medium speed RC oscillation sopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	1.8 to 3.6		46	192	
	IDDOP(9)		<ul style="list-style-type: none"><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal low speed RC oscillation.</li><li>• Internal medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	5.0		75	176	
			<ul style="list-style-type: none"><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal low speed RC oscillation.</li><li>• Internal medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	3.3		46	115	
			<ul style="list-style-type: none"><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal low speed RC oscillation.</li><li>• Internal medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li><li>• Ta=-10 to +50°C</li></ul>	2.5		35	85	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

Continued on next page.

# LC87F2G08A

Continued from preceding page.

Parameter	Symbol	Pin/ remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(7)	V <sub>DD</sub> 1	<div>• HALT mode</div> <div>• FsX'tal=32.768kHz crystal oscillation mode</div> <div>• Internal low speed and medium speed RC oscillation stopped.</div> <div>• System clock set to 8MHz with frequency variable RC oscillation</div> <div>• 1/1 frequency division ratio</div>	2.7 to 5.5		1.8	3.5	mA
			2.7 to 3.6		1.1	2.0		
	IDDHALT(8)		<div>• HALT mode</div> <div>• External FsX'tal and FmCF oscillation stopped.</div> <div>• System clock set to internal low speed RC oscillation.</div> <div>• Internal medium speed RC oscillation stopped.</div> <div>• Frequency variable RC oscillation stopped.</div> <div>• 1/1 frequency division ratio</div>	1.8 to 5.5		23	260	μA
			1.8 to 3.6		13	119		
	IDDHALT(9)		<div>• HALT mode</div> <div>• External FsX'tal and FmCF oscillation stopped.</div> <div>• System clock set to internal low speed RC oscillation.</div> <div>• Internal medium speed RC oscillation stopped.</div> <div>• Frequency variable RC oscillation stopped.</div> <div>• 1/1 frequency division ratio</div> <div>• Ta=-10 to +50°C</div>	5.0		23	65	
			3.3		13	35		
			2.5		9.2	25		
	IDDHALT(10)		<div>• HALT mode</div> <div>• FsX'tal=32.768kHz crystal oscillation mode</div> <div>• System clock set to 32.768kHz side</div> <div>• Internal low speed and medium speed RC oscillation stopped.</div> <div>• Frequency variable RC oscillation stopped.</div> <div>• 1/2 frequency division ratio</div>	1.8 to 5.5		25	112	
			1.8 to 3.6		8.5	56		
	IDDHALT(11)		<div>• HALT mode</div> <div>• FsX'tal=32.768kHz crystal oscillation mode</div> <div>• System clock set to 32.768kHz side</div> <div>• Internal low speed and medium speed RC oscillation stopped.</div> <div>• Frequency variable RC oscillation stopped.</div> <div>• 1/2 frequency division ratio</div> <div>• Ta=-10 to +50°C</div>	5.0		25	69	
			3.3		8.5	29		
			2.5		4.2	15		
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)	<div>HOLD mode</div> <div>• CF1=V<sub>DD</sub> or open (External clock mode)</div>	1.8 to 5.5		0.04	30		
		1.8 to 3.6		0.02	21			
	IDDHOLD(2)	<div>HOLD mode</div> <div>• CF1=V<sub>DD</sub> or open (External clock mode)</div> <div>• Ta=-10 to +50°C</div>	5.0		0.04	2.3		
		3.3		0.02	1.5			
		2.5		0.017	1.2			
	IDDHOLD(3)	<div>HOLD mode</div> <div>• CF1=V<sub>DD</sub> or open (External clock mode)</div> <div>• LVD option selected</div>	1.8 to 5.5		3.2	35		
		1.8 to 3.6		2.7	24			
	IDDHOLD(4)	<div>HOLD mode</div> <div>• CF1=V<sub>DD</sub> or open (External clock mode)</div> <div>• Ta=-10 to +50°C</div> <div>• LVD option selected</div>	5.0		3.2	6.5		
3.3			2.7	4.5				
2.5			2.5	4.2				
Timer HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(5)	<div>Timer HOLD mode</div> <div>• FsX'tal=32.768 kHz crystal oscillation mode</div>	1.8 to 5.5		22	106		
		1.8 to 3.6		7.5	45			
	IDDHOLD(6)	<div>Timer HOLD mode</div> <div>• FsX'tal=32.768kHz crystal oscillation mode</div> <div>• Ta=-10 to +50°C</div>	5.0		22	62		
		3.3		7.5	23			
			2.5		2.9	12		

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.



# LC87F2G08A

## F-ROM Programming Characteristics at Ta = +10°C to +55°C, VSS1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
Onboard programming current	IDDFW(1)	V <sub>DD</sub> 1	• Only current of the Flash block.	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	μs

## UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, VSS1 = 0V

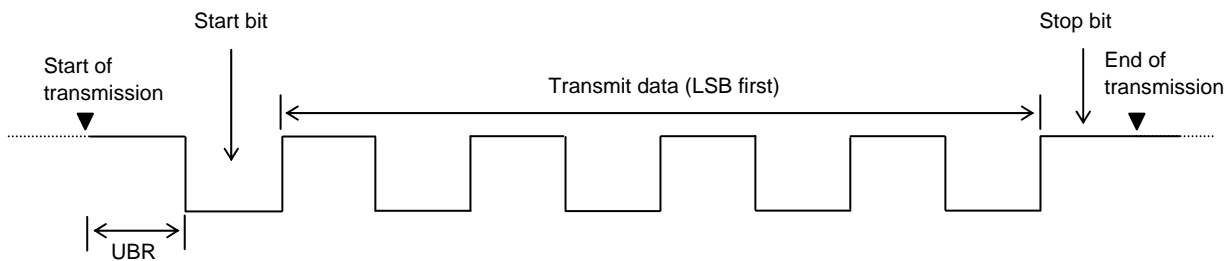
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
Transfer rate	UBR	UTX(P20) URX(P21)		1.8 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)

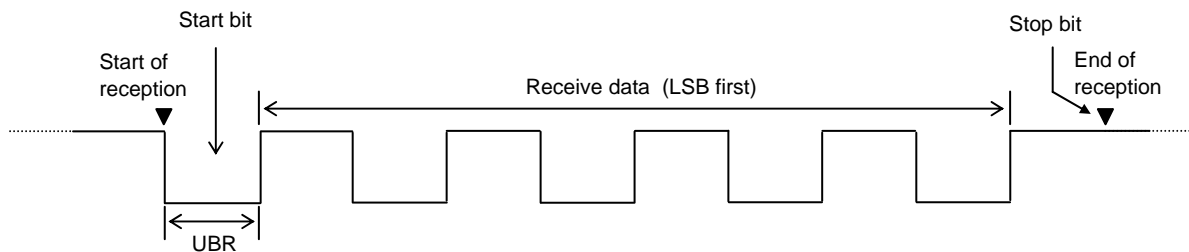
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: None

### Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



### Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



## LC87F2G08A

### Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

- CF oscillation normal amplifier size selected (CFLAMP=0)

#### ■MURATA

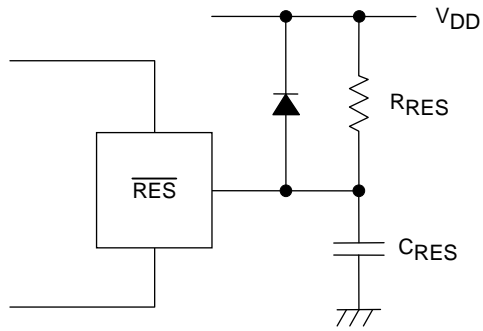
Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	1.0k	2.7 to 5.5	0.1	0.5	Internal C1, C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.2 to 3.6	0.1	0.5	
					Open	1.0k	2.3 to 5.5	0.1	0.5	
8MHz	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	1.0k	2.5 to 5.5	0.1	0.5	
	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1.5k	2.2 to 5.5	0.1	0.5	
6MHz	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1.0k	2.2 to 3.6	0.1	0.5	
	SMD	CSTLS8M00G53-B0	(15)	(15)	Open	1.5k	2.4 to 5.5	0.1	0.5	
4MHz	LEAD	CSTCR6M00G53-R0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.1	0.5	
	SMD	CSTLS6M00G53-B0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.1	0.5	
4MHz	LEAD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 2.7	0.2	0.6	
	SMD	CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	1.9 to 5.5	0.2	0.6	

- CF oscillation low amplifier size selected (CFLAMP=1)

#### ■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.0k	2.3 to 2.7	0.2	0.6	Internal C1,C2
					Open	2.2k	2.5 to 5.5	0.2	0.6	
	LEAD	CSTCR4M00G53095-R0	(15)	(15)	Open	1.0k	2.1 to 2.7	0.2	0.7	
		CSTLS4M00G53-B0	(15)	(15)	Open	1.0k	2.3 to 2.7	0.2	0.6	
					Open	2.2k	2.5 to 5.5	0.2	0.6	
		CSTLS4M00G53095-B0	(15)	(15)	Open	1.0k	2.1 to 2.7	0.2	0.7	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V<sub>DD</sub> goes above the operating voltage lower limit (see Figure 3).



Note:  
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 4 Reset Circuit

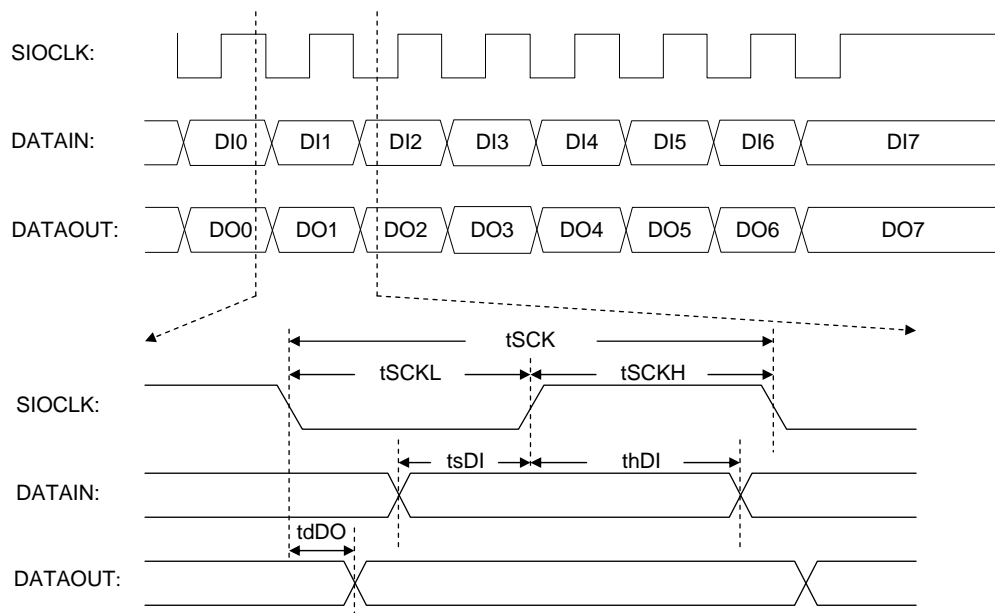


Figure 5 Serial I/O Output Waveforms

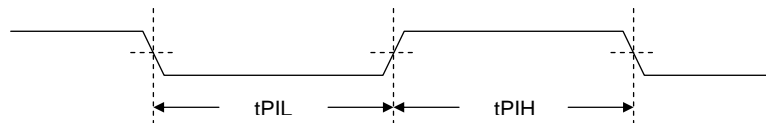


Figure 6 Pulse Input Timing Signal Waveform

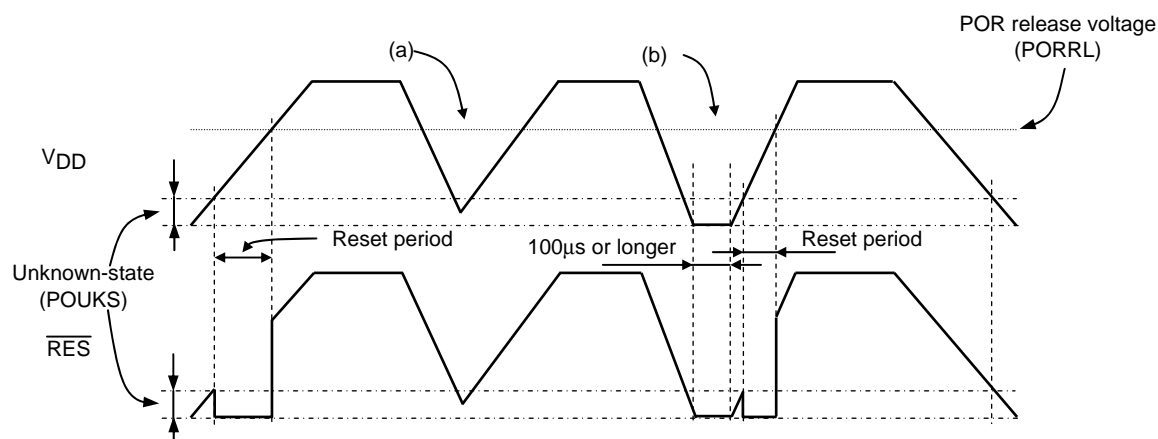


Figure 7 Waveform observed when only POR is used (LVD not used)  
(RESET pin: Pull-up resistor  $R_{RES}$  only)

- The POR function generates a reset only when power is turned on starting at the  $V_{SS}$  level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the  $V_{SS}$  level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the  $V_{SS}$  level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

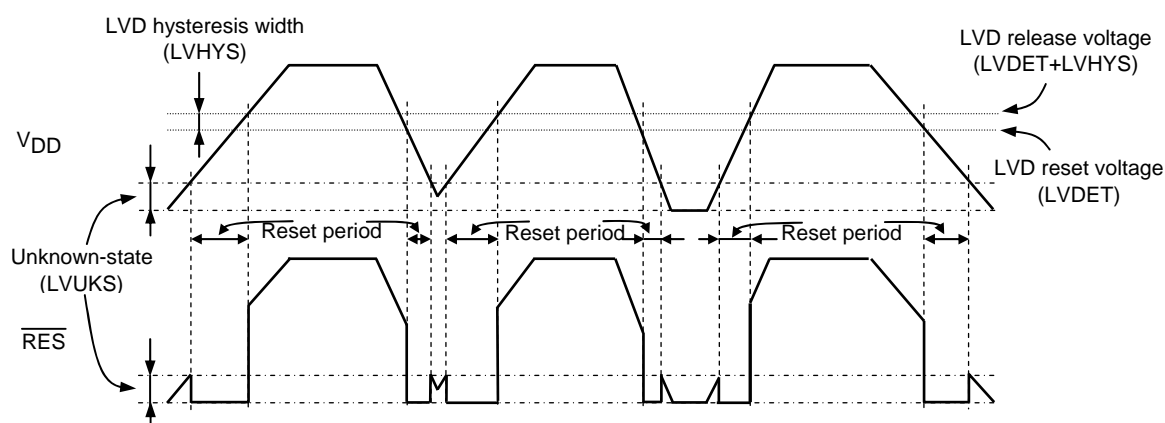


Figure 8 Waveform observed when both POR and LVD functions are used  
(RESET pin: Pull-up resistor  $R_{RES}$  only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

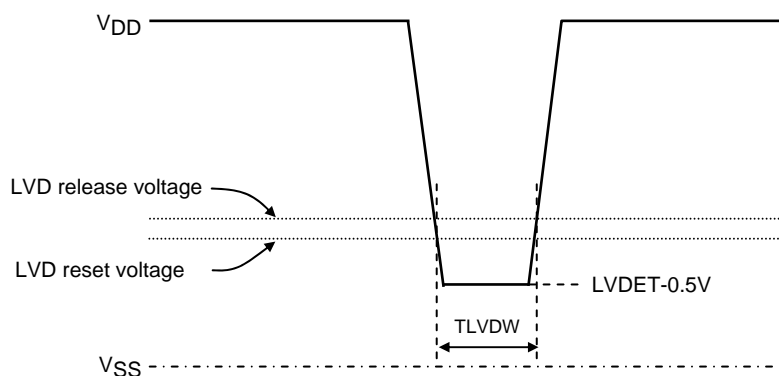


Figure 9 Low voltage detection minimum width  
(Example of momentary power loss/Voltage variation waveform)

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