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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | - |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | SIO, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-SOP (0.236", 6.00mm Width) |
| Supplier Device Package | 24-MFPSJ |
| Purchase URL | https://www.e-xfl.com/product-detail/onsemi/lc87f2g08aumj-zh |

■Ports

- Normal withstand voltage I/O ports
  Ports I/O direction can be designated in 1-bit units — 11 (P1n, P20, P21, P70)
  Ports I/O direction can be designated in 4-bit units — 8 (P0n)
- Dedicated oscillator ports/input ports — 2 (CF1/XT1, CF2/XT2)
- Reset pin — 1 ($\overline{RES}$)
- Power pins — 2 ($V_{SS}1$, $V_{DD}1$)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■High-Speed Clock Counter

- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- Can generate output real time.

■SIO

- SIO0: 8-bit Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3tCYC)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART

- Full Duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■AD Converter: 12 bits/8 bits × 8 channels

- 12 bits/8 bits AD converter resolution selectable

■Remote Control Receiver Circuit (sharing pins with P15, SCK1, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Clock Output Function
- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts
- 18 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|---|---|---|---|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4 |
| 4 | 0001BH | H or L | INT3/base timer |
| 5 | 00023H | H or L | T0H |
| 6 | 0002BH | H or L | T1L/T1H |
| 7 | 00033H | H or L | SIO0/UART1 receive |
| 8 | 0003BH | H or L | SIO1/UART1 transmit |
| 9 | 00043H | H or L | ADC/T6/T7 |
| 10 | 0004BH | H or L | Port 0 |

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- Internal oscillation circuits
  Low-speed RC oscillation circuit : For system clock (100kHz)
  Medium-speed RC oscillation circuit : For system clock (1MHz)
  Multifrequency RC oscillation circuit : For system clock (8MHz)
- External oscillation circuits
  Hi-speed CF oscillation circuit: For system clock, with internal Rf
  Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf
  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Internal Reset Function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the base timer circuit.
     Note: Available only when X'tal oscillation is selected.

■Onchip Debugger

- Supports software debugging with the IC mounted on the target board.
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
  DBGP0 (P0), DBGP1 (P1)

■Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Development Tools

- On-chip debugger: (1) TCB87 type B + LC87D2G08A
  (2) TCB87 TypeB + LC87F2G08A
  (3) TCB87 TypeC (3 wire version) + LC87D2G08A
  (4) TCB87 TypeC (3 wire version) + LC87F2G08A

Note: LC87F2G08A has an On-chip debugger but its function is limited.

■Flash ROM Programming Boards

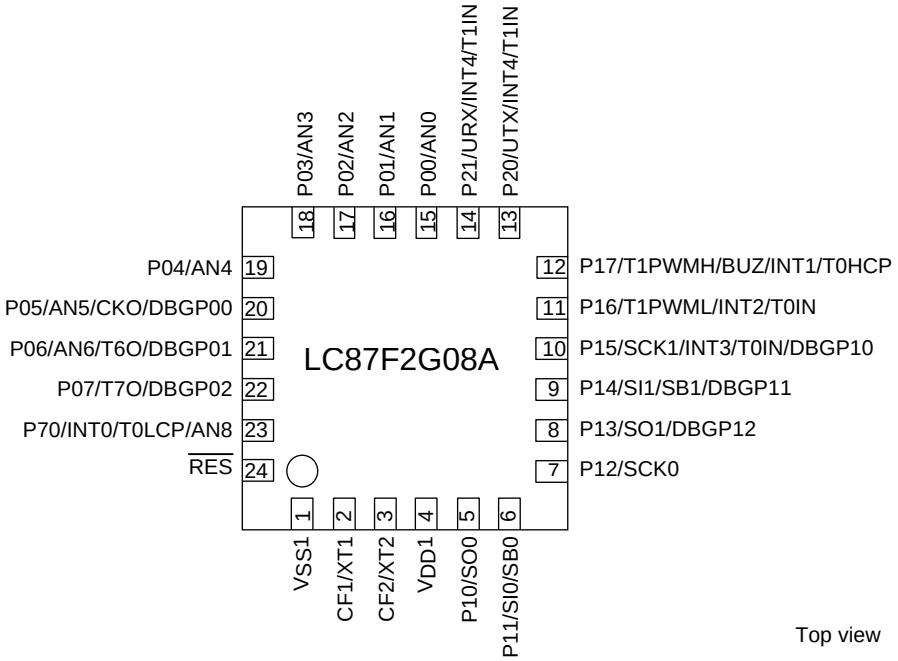
| Package | Programming boards |
|---|---|
| MFP24S(300mil) | W87F2GM |
| MFP24SJ(300mil) | W87F2GMJ |
| SSOP24(225mil) | W87F2GS |
| VCT24(3.5×3.5) | (build-to-order) |

■Flash ROM Programmer

| Maker | | Model | Supported version | Device |
|---|---|---|---|---|
| Flash Support Group, Inc. (FSG) | Single Programmer | AF9708<br>AF9709/AF9709B/AF9709C<br>(Including Ando Electric Co., Ltd. models) | Rev 02.72 or later | LC87F2H08A |
| | Gang Programmer | AF9723/AF9723B(Main body)<br>(Including Ando Electric Co., Ltd. models) | - | - |
| | | AF9833(Unit)<br>(Including Ando Electric Co., Ltd. models) | - | - |
| Flash Support Group, Inc. (FSG) + Our company (Note 1) | In-circuit Programmer | AF9101/AF9103(Main body)<br>(FSG models) | (Note 2) | LC87F2G08A |
| | | SIB87(Inter Face Driver)<br>(Our company model) | | |
| Our company | Single/Gang Programmer | SKK/SKK Type B<br>(SanyoFWS) | Application Version 1.04 or later<br>Chip Data Version 2.10 or later | LC87F2G08A |
| | In-circuit/Gang Programmer | SKK-DBG Type B<br>(SanyoFWS) | | |

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or Our company for the information.



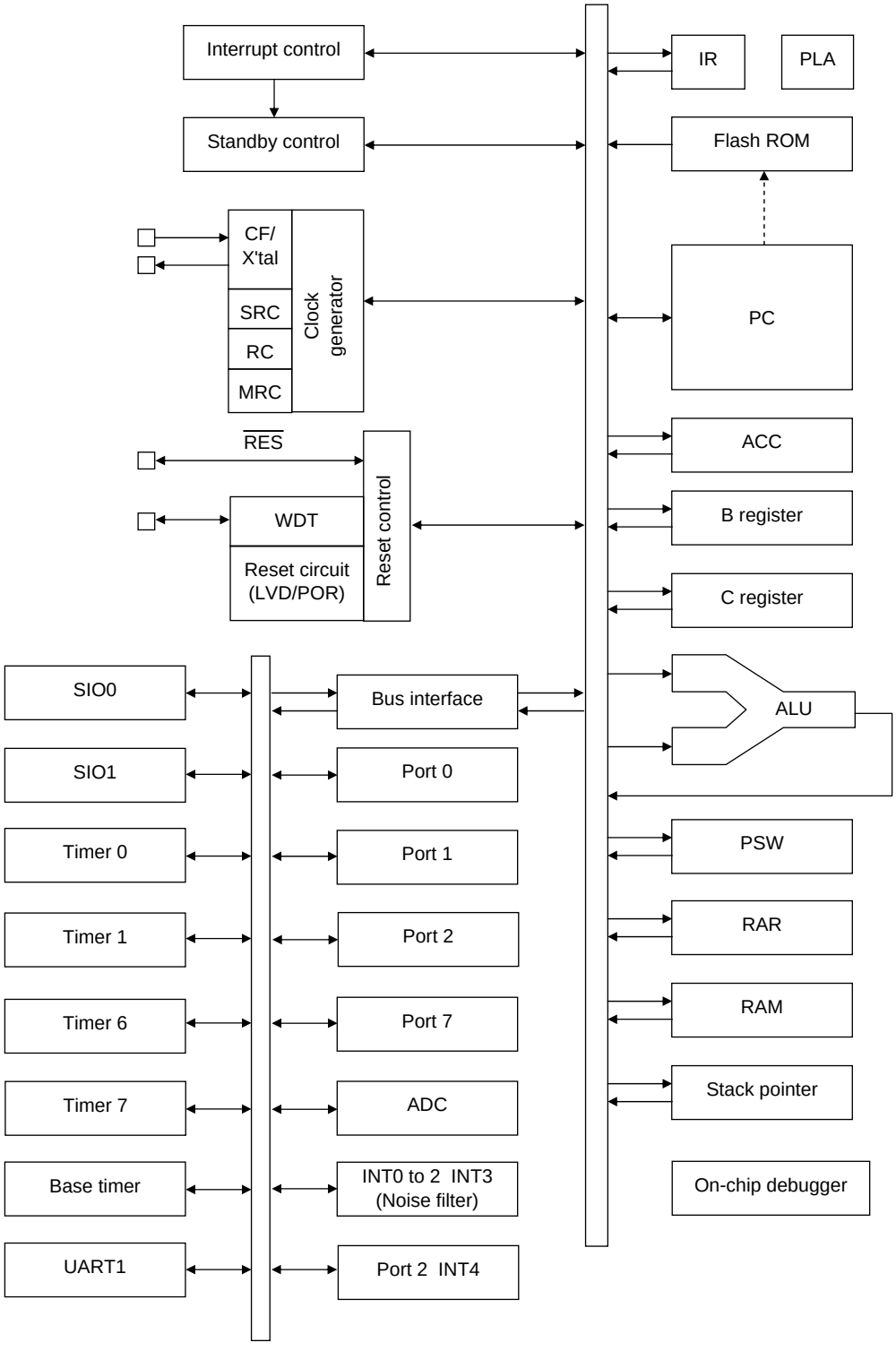

Top view

VCT24(3.5×3.5) “Lead-/Halogen-free Type” (build-to-order)

| VCT24 | NAME |
|---|---|
| 1 | $V_{SS}1$ |
| 2 | CF1/XT1 |
| 3 | CF2/XT2 |
| 4 | $V_{DD}1$ |
| 5 | P10/SO0 |
| 6 | P11/SI0/SB0 |
| 7 | P12/SCK0 |
| 8 | P13/SO1/DBGP12 |
| 9 | P14/SI1/SB1/DBGP11 |
| 10 | P15/SCK1/INT3/T0IN/DBGP10 |
| 11 | P16/T1PWML/INT2/T0IN |
| 12 | P17/T1PWMH/BUZ/INT1/T0HCP |

| VCT24 | NAME |
|---|---|
| 13 | P20/UTX/INT4/T1IN |
| 14 | P21/URX/INT4/T1IN |
| 15 | P00/AN0 |
| 16 | P01/AN1 |
| 17 | P02/AN2 |
| 18 | P03/AN3 |
| 19 | P04/AN4 |
| 20 | P05/AN5/CKO/DBGP00 |
| 21 | P06/AN6/T6O/DBGP01 |
| 22 | P07/T7O/DBGP02 |
| 23 | P70/INT0/T0LCP/AN8 |
| 24 | $\overline{\text{RES}}$ |

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0<br>P00 to P07</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 4-bit units<br>• Pull-up resistors can be turned on and off in 4-bit units.<br>• HOLD reset input<br>• Port 0 interrupt input<br>• Pin functions<br>P05: System clock output<br>P06: Timer 6 toggle output<br>P07: Timer 7 toggle output<br>P00(AN0) to P06(AN6): AD converter input<br>P05(DBGP00) to P07(DBGP02): On-chip debugger 0 port</td><td>Yes</td></tr>
<tr><td>Port 1<br>P10 to P17</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Pin functions<br>P10: SIO0 data output<br>P11: SIO0 data input/bus I/O<br>P12: SIO0 clock I/O<br>P13: SIO1 data output<br>P14: SIO1 data input / bus I/O<br>P15: SIO1 clock I/O / INT3 input (with noise filter) / timer 0 event input / timer 0H capture input<br>P16: Timer 1PWML output / INT2 input/HOLD reset input/timer 0 event input / timer 0L capture input<br>P17: Timer 1PWMH output / beeper output / INT1 input / HOLD reset input / timer 0H capture input<br>P15(DBGP10) to P13(DBGP12): On-chip-debugger 1 port<br>Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 2<br>P20 to P21</td><td>I/O</td><td>• 2-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Pin functions<br>P20: UART transmit<br>P21: UART receive<br>P20 to P21: INT4 input / HOLD reset input / timer 1 event input / timer 0L capture input / timer 0H capture input<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7<br>P70</td><td>I/O</td><td>• 1-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Pin functions<br>P70: INT0 input / HOLD reset input / timer 0L capture input / watchdog timer output<br>P70(AN8): AD converter input<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input / internal reset output</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic resonator or 32.768kHz crystal oscillator input pin<br>• Pin function<br>General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic resonator or 32.768kHz crystal oscillator output pin<br>• Pin function<br>General-purpose input port</td><td>No</td></tr>
</table>

## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port Name | Option selected in units of | Option type | Output type | Pull-up resistor |
|---|---|---|---|---|
| P00 to P07 | 1 bit | 1 | CMOS | Programmable (Note 1) |
| | | 2 | Nch-open drain | No |
| P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P20 to P21 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P70 | - | No | Nch-open drain | Programmable |

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

**Absolute Maximum Ratings** at Ta = 25°C, $V_{SS}1$ =0V

| Parameter | | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$ | | | -0.3 | | +6.5 | V |
| Input voltage | | $V_I$ | CF1, CF2 | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$ | Ports 0, 1, 2, P70 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH | Ports 0, 1, 2 | CMOS output select Per 1 applicable pin | | -10 | | | mA |
| | Mean output current (Note 1-1) | IOMH | Ports 0, 1, 2 | CMOS output select Per 1 applicable pin | | -7.5 | | | |
| | Total output current | ΣIOAH(1) | P10 to P14 | Total of all applicable pins | | -20 | | | |
| | | ΣIOAH(2) | Ports 0, 2 P15 to P17 | Total of all applicable pins | | -20 | | | |
| | | ΣIOAH(3) | Ports 0, 1, 2 | Total of all applicable pins | | -25 | | | |
| Low level output current | Peak output current | IOPL(1) | P02 to P07 Ports 1, 2 | Per 1 applicable pin | | | | 20 | |
| | | IOPL(2) | P00, P01 | Per 1 applicable pin | | | | 30 | |
| | | IOPL(3) | P70 | Per 1 applicable pin | | | | 10 | |
| | Mean output current (Note 1-1) | IOML(1) | P02 to P07 Ports 1, 2 | Per 1 applicable pin | | | | 15 | |
| | | IOML(2) | P00, P01 | Per 1 applicable pin | | | | 20 | |
| | | IOML(3) | P70 | Per 1 applicable pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | P10 to P14 | Total of all applicable pins | | | | 50 | |
| | | ΣIOAL(2) | Port 0, 2, P15 to P17 | Total of all applicable pins | | | | 60 | |
| | | ΣIOAL(3) | Ports 0, 1, 2 | Total of all applicable pins | | | | 70 | |
| | | ΣIOAL(4) | P70 | Total of all applicable pins | | | | 7.5 | |
| Power Dissipation | | Pd max(1) | MFP24S(300mil) | Ta=-40 to +85°C Package only | | | | 129 | mW |
| | | Pd max(2) | | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | 229 | |
| | | Pd max(3) | MFP24SJ(300mil) | Ta=-40 to +85°C Package only | | | | 171 | |
| | | Pd max(4) | | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | 393 | |
| | | Pd max(5) | SSOP24(225mil) | Ta=-40 to +85°C Package only | | | | 111 | |
| | | Pd max(6) | | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | 334 | |
| | | Pd max(7) | VCT24(3.5×3.5) | Ta=-40 to +85°C Package only | | | | T.B.D | |
| | | Pd max(8) | | Ta=-40 to +85°C Package with thermal resistance board | | | | T.B.D | |
| Operating ambient temperature | | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Conditions** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Operating supply voltage (Note 2-1) | $V_{DD}(1)$ | $V_{DD}1$ | 0.245µs ≤ tCYC ≤ 200µs | | 2.7 | | 5.5 | V |
| | $V_{DD}(2)$ | | 0.294µs ≤ tCYC ≤ 200µs | | 2.2 | | 5.5 | |
| | $V_{DD}(3)$ | | 0.735µs ≤ tCYC ≤ 200µs | | 1.8 | | 5.5 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1$ | RAM and register contents sustained in HOLD mode. | | 1.6 | | | |
| High level input voltage | $V_{IH}(1)$ | Ports 1, 2, P70 port input/ interrupt side | | 1.8 to 5.5 | $0.3V_{DD}+0.7$ | | $V_{DD}$ | |
| | $V_{IH}(2)$ | Ports 0 | | 1.8 to 5.5 | $0.3V_{DD}+0.7$ | | $V_{DD}$ | |
| | $V_{IH}(3)$ | Port 70 watchdog timer side | | 1.8 to 5.5 | $0.9V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(4)$ | CF1, $\overline{RES}$ | | 1.8 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1, 2, P70 port input/ interrupt side | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}+0.4$ | |
| | | | | 1.8 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | Ports 0 | | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}+0.4$ | |
| | | | | 1.8 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 70 watchdog timer side | | 1.8 to 5.5 | $V_{SS}$ | | $0.8V_{DD}-1.0$ | |
| | $V_{IL}(4)$ | CF1, $\overline{RES}$ | | 1.8 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-1) | tCYC (Note 2-2) | | | 2.7 to 5.5 | 0.245 | | 200 | µs |
| | | | | 2.2 to 5.5 | 0.294 | | 200 | |
| | | | | 1.8 to 5.5 | 0.735 | | 200 | |
| External system clock frequency | FEXCF | CF1 | • CF2 pin open<br>• System clock frequency division ratio=1/1<br>• External system clock duty=50±5% | 2.7 to 5.5 | 0.1 | | 12 | MHz |
| | | | | 1.8 to 5.5 | 0.1 | | 4 | |
| | | | • CF2 pin open<br>• System clock frequency division ratio=1/2<br>• External system clock duty=50±5% | 3.0 to 5.5 | 0.2 | | 24.4 | |
| | | | | 2.0 to 5.5 | 0.2 | | 8 | |
| Oscillation frequency range (Note 2-3) | FmCF(1) | CF1, CF2 | 12MHz ceramic oscillation. See Fig. 1. | 2.7 to 5.5 | | 12 | | MHz |
| | FmCF(2) | CF1, CF2 | 10MHz ceramic oscillation. See Fig. 1. | 2.2 to 5.5 | | 10 | | |
| | FmCF(3) | CF1, CF2 | 4MHz ceramic oscillation. CF oscillation normal amplifier size selected. (CFLAMP=0) See Fig. 1. | 1.8 to 5.5 | | 4 | | |
| | | | 4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1. | 2.2 to 5.5 | | 4 | | |
| | FmMRC | | Frequency variable RC oscillation. 1/2 frequency division ration. (RCCTD=0) (Note 2-4) | 2.7 to 5.5 | 7.44 | 8.0 | 8.56 | |
| | FmRC | | Internal medium-speed RC oscillation | 1.8 to 5.5 | 0.5 | 1.0 | 2.0 | |
| | FmSRC | | Internal low-speed RC oscillation | 1.8 to 5.5 | 50 | 100 | 200 | kHz |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation See Fig. 2. | 1.8 to 5.5 | | 32.768 | | |

Note 2-1: $V_{DD}$ must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100µs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

**Electrical Characteristics** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| High level input current | $I_{IH}$(1) | Ports 0, 1, 2, P70, $\overline{RES}$ | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{DD}$<br>(Including output Tr's off leakage current) | 1.8 to 5.5 | | | 1 | μA |
| | $I_{IH}$(2) | CF1 | $V_{IN}=V_{DD}$ | 1.8 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}$(1) | Ports 0, 1, 2, P70, $\overline{RES}$ | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{SS}$<br>(Including output Tr's off leakage current) | 1.8 to 5.5 | -1 | | | |
| | $I_{IL}$(2) | CF1 | $V_{IN}=V_{SS}$ | 1.8 to 5.5 | -15 | | | |
| High level output voltage | $V_{OH}$(1) | Ports 0, 1, 2 | $I_{OH}$=-1mA | 4.5 to 5.5 | $V_{DD}$-1 | | | V |
| | $V_{OH}$(2) | | $I_{OH}$=-0.35mA | 2.7 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}$(3) | | $I_{OH}$=-0.15mA | 1.8 to 5.5 | $V_{DD}$-0.4 | | | |
| Low level output voltage | $V_{OL}$(1) | Ports 0, 1, 2 | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}$(2) | | $I_{OL}$=1.4mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}$(3) | | $I_{OL}$=0.8mA | 1.8 to 5.5 | | | 0.4 | |
| | $V_{OL}$(4) | P70 | $I_{OL}$=1.4mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}$(5) | | $I_{OL}$=0.8mA | 1.8 to 5.5 | | | 0.4 | |
| | $V_{OL}$(6) | P00, P01 | $I_{OL}$=25mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}$(7) | | $I_{OL}$=4mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}$(8) | | $I_{OL}$=2mA | 1.8 to 5.5 | | | 0.4 | |
| Pull-up resistance | Rpu(1) | Ports 0, 1, 2<br>P70 | $V_{OH}$=0.9$V_{DD}$<br>When Port 0 selected<br>low-impedance pull-up. | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 1.8 to 4.5 | 18 | 50 | 230 | |
| | Rpu(3) | Port 0 | $V_{OH}$=0.9$V_{DD}$<br>When Port 0 selected<br>high-impedance pull-up. | 1.8 to 5.5 | 100 | 210 | 400 | |
| Hysteresis voltage | VHYS(1) | Ports 1, 2, P70, $\overline{RES}$ | | 2.7 to 5.5 | | 0.1$V_{DD}$ | | V |
| | VHYS(2) | | | 1.8 to 2.7 | | 0.07$V_{DD}$ | | |
| Pin capacitance | CP | All pins | For pins other than that under test:<br>$V_{IN}=V_{SS}$<br>f=1MHz<br>Ta=25°C | 1.8 to 5.5 | | 10 | | pF |

**Serial I/O Characteristics** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | • See Fig. 5. | 1.8 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected<br>• See Fig. 5. | 1.8 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(1) | SB0(P11), SI0(P11) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 5. | 1.8 to 5.5 | 0.05 | | | µs |
| | Data hold time | | thDI(1) | | | | 0.05 | | | |
| Serial output | Input clock | Output delay time | tdD0(1) | SO0(P10), SB0(P11) | • Continuous data transmission/reception mode (Note 4-1-2) | 1.8 to 5.5 | | | (1/3)tCYC +0.08 | |
| | | | tdD0(2) | | • Synchronous 8-bit mode (Note 4-1-2) | | | | 1tCYC +0.08 | |
| | Output clock | | tdD0(3) | | (Note 4-1-2) | | | | (1/3)tCYC +0.08 | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig. 5. | 1.8 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected<br>• See Fig. 5. | 1.8 to 5.5 | 2 | | | tSCK |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 5. | 1.8 to 5.5 | 0.05 | | | µs |
| | Data hold time | | thDI(2) | | | | 0.05 | | | |
| Serial output | Output delay time | | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 5. | 1.8 to 5.5 | | | (1/3)tCYC +0.08 | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

**Pulse Input Conditions** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70),<br>INT1(P17),<br>INT2(P16),<br>INT4(P20 to P21) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 1.8 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P15) when noise filter time constant is 1/1 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 1.8 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P15) when noise filter time constant is 1/32 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are nabled. | 1.8 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P15) when noise filter time constant is 1/128 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 1.8 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{\text{RES}}$ | • Resetting is enabled. | 1.8 to 5.5 | 200 | | | µs |

**Consumption Current Characteristics** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

| Parameter | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Normal mode consumption current (Note 9-1) (Note 9-2) | IDDOP(1) | $V_{DD}1$ | • FmCF=12MHz ceramic oscillation mode<br>• System clock set to 12MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 2.7 to 5.5 | | 7.4 | 13.0 | mA |
| | | | | 2.7 to 3.6 | | 4.4 | 8.1 | |
| | IDDOP(2) | | • CF1=24MHz external clock<br>• System clock set to CF1 side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 3.0 to 5.5 | | 9.7 | 16.2 | |
| | | | | 3.0 to 3.6 | | 5.3 | 8.7 | |
| | IDDOP(3) | | • FmCF=10MHz ceramic oscillation mode<br>• System clock set to 10MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 2.2 to 5.5 | | 6.6 | 11.9 | |
| | | | | 2.2 to 3.6 | | 4.0 | 7.4 | |
| | IDDOP(4) | | • FmCF=4MHz ceramic oscillation mode<br>• System clock set to 4MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 1.8 to 5.5 | | 2.9 | 6.5 | |
| | | | | 1.8 to 3.6 | | 2.2 | 4.2 | |
| | IDDOP(5) | | • CF oscillation low amplifier size selected. (CFLAMP=1)<br>• FmCF=4MHz ceramic oscillation mode<br>• System clock set to 4MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/4 frequency division ratio | 2.2 to 5.5 | | 1.1 | 2.5 | |
| | | | | 2.2 to 3.6 | | 0.6 | 1.3 | |
| | IDDOP(6) | | • FsX'tal=32.768kHz crystal oscillation mode<br>• Internal low speed RC oscillation stopped.<br>• System clock set to internal medium speed RC oscillation.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 1.8 to 5.5 | | 0.6 | 1.7 | |
| | | | | 1.8 to 3.6 | | 0.3 | 0.9 | |
| | IDDOP(7) | | • FsX'tal=32.768kHz crystal oscillation mode<br>• Internal low speed and medium speed RC oscillation stopped.<br>• System clock set to 8MHz with frequency variable RC oscillation<br>• 1/1 frequency division ratio | 2.7 to 5.5 | | 5.0 | 9.1 | |
| | | | | 2.7 to 3.6 | | 3.6 | 5.8 | |
| | IDDOP(8) | | • External FsX'tal and FmCF oscillation stopped.<br>• System clock set to internal low speed RC oscillation.<br>• Internal medium speed RC oscillation sopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 1.8 to 5.5 | | 75 | 370 | µA |
| | | | | 1.8 to 3.6 | | 46 | 192 | |
| | IDDOP(9) | | • External FsX'tal and FmCF oscillation stopped.<br>• System clock set to internal low speed RC oscillation.<br>• Internal medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio<br>• Ta=-10 to +50°C | 5.0 | | 75 | 176 | |
| | | | | 3.3 | | 46 | 115 | |
| | | | | 2.5 | | 35 | 85 | |

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Normal mode consumption current (Note 9-1) (Note 9-2) | IDDOP(10) | $V_{DD}$1 | • FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 1.8 to 5.5 | | 38 | 139 | µA |
| | | | | 1.8 to 3.6 | | 15 | 66 | |
| | IDDOP(11) | | • FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio<br>• Ta=-10 to +50°C | 5.0 | | 38 | 101 | |
| | | | | 3.3 | | 15 | 46 | |
| | | | | 2.5 | | 9.0 | 28 | |
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(1) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• System clock set to 12MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 2.7 to 5.5 | | 3.1 | 5.6 | mA |
| | | | | 2.7 to 3.6 | | 1.6 | 2.9 | |
| | IDDHALT(2) | | • HALT mode<br>• CF1=24MHz external clock<br>• System clock set to CF1 side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 3.0 to 5.5 | | 4.9 | 8.6 | |
| | | | | 3.0 to 3.6 | | 2.3 | 3.8 | |
| | IDDHALT(3) | | • HALT mode<br>• FmCF=10MHz ceramic oscillation mode<br>• System clock set to 10MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 2.2 to 5.5 | | 2.7 | 5.3 | |
| | | | | 2.2 to 3.6 | | 1.4 | 2.6 | |
| | IDDHALT(4) | | • HALT mode<br>• FmCF=4MHz ceramic oscillation mode<br>• System clock set to 4MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 1.8 to 5.5 | | 1.4 | 3.5 | |
| | | | | 1.8 to 3.6 | | 0.7 | 1.3 | |
| | IDDHALT(5) | | • HALT mode<br>• CF oscillation low amplifier size selected. (CFLAMP=1)<br>• FmCF=4MHz ceramic oscillation mode<br>• System clock set to 4MHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/4 frequency division ratio | 2.2 to 5.5 | | 0.7 | 1.8 | |
| | | | | 2.2 to 3.6 | | 0.3 | 0.7 | |
| | IDDHALT(6) | | • HALT mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• Internal low speed RC oscillation stopped.<br>• System clock set to internal medium speed RC oscillation<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 1.8 to 5.5 | | 0.4 | 1.1 | |
| | | | | 1.8 to 3.6 | | 0.2 | 0.5 | |

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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| Parameter | Symbol | Pin/ remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(7) | $V_{DD}$1 | • HALT mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• Internal low speed and medium speed RC oscillation stopped.<br>• System clock set to 8MHz with frequency variable RC oscillation<br>• 1/1 frequency division ratio | 2.7 to 5.5 | | 1.8 | 3.5 | mA |
| | | | | 2.7 to 3.6 | | 1.1 | 2.0 | |
| | IDDHALT(8) | | • HALT mode<br>• External FsX'tal and FmCF oscillation stopped.<br>• System clock set to internal low speed RC oscillation.<br>• Internal medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 1.8 to 5.5 | | 23 | 260 | μA |
| | | | | 1.8 to 3.6 | | 13 | 119 | |
| | IDDHALT(9) | | • HALT mode<br>• External FsX'tal and FmCF oscillation stopped.<br>• System clock set to internal low speed RC oscillation.<br>• Internal medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio<br>• Ta=-10 to +50°C | 5.0 | | 23 | 65 | |
| | | | | 3.3 | | 13 | 35 | |
| | | | | 2.5 | | 9.2 | 25 | |
| | IDDHALT(10) | | • HALT mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 1.8 to 5.5 | | 25 | 112 | |
| | | | | 1.8 to 3.6 | | 8.5 | 56 | |
| | IDDHALT(11) | | • HALT mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low speed and medium speed RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio<br>• Ta=-10 to +50°C | 5.0 | | 25 | 69 | |
| | | | | 3.3 | | 8.5 | 29 | |
| | | | | 2.5 | | 4.2 | 15 | |
| HOLD mode consumption current (Note 9-1) (Note 9-2) | IDDHOLD(1) | | HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode) | 1.8 to 5.5 | | 0.04 | 30 | |
| | | | | 1.8 to 3.6 | | 0.02 | 21 | |
| | IDDHOLD(2) | | HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• Ta=-10 to +50°C | 5.0 | | 0.04 | 2.3 | |
| | | | | 3.3 | | 0.02 | 1.5 | |
| | | | | 2.5 | | 0.017 | 1.2 | |
| | IDDHOLD(3) | | HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• LVD option selected | 1.8 to 5.5 | | 3.2 | 35 | |
| | | | | 1.8 to 3.6 | | 2.7 | 24 | |
| | IDDHOLD(4) | | HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• Ta=-10 to +50°C<br>• LVD option selected | 5.0 | | 3.2 | 6.5 | |
| | | | | 3.3 | | 2.7 | 4.5 | |
| | | | | 2.5 | | 2.5 | 4.2 | |
| Timer HOLD mode consumption current (Note 9-1) (Note 9-2) | IDDHOLD(5) | | Timer HOLD mode<br>• FsX'tal=32.768 kHz crystal oscillation mode | 1.8 to 5.5 | | 22 | 106 | |
| | | | | 1.8 to 3.6 | | 7.5 | 45 | |
| | IDDHOLD(6) | | Timer HOLD mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• Ta=-10 to +50°C | 5.0 | | 22 | 62 | |
| | | | | 3.3 | | 7.5 | 23 | |
| | | | | 2.5 | | 2.9 | 12 | |

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

**F-ROM Programming Characteristics** at Ta = +10°C to +55°C, $V_{SS}1$ = 0V

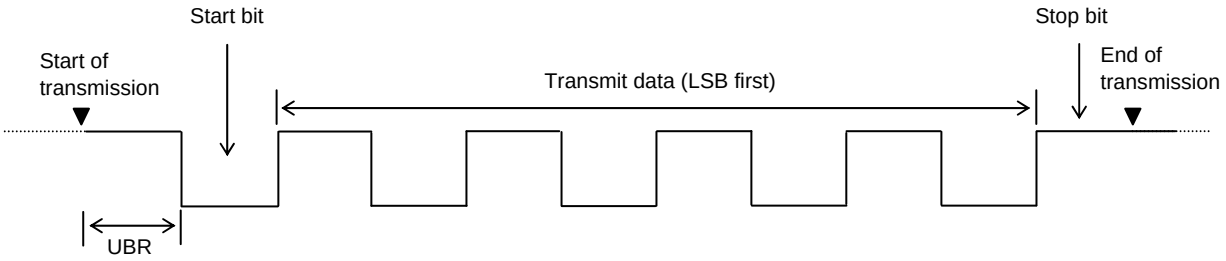
| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | $V_{DD}1$ | • Only current of the Flash block. | 2.2 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erasing time | 2.2 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • Programming time | | | 40 | 60 | µs |

**UART (Full Duplex) Operating Conditions** at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

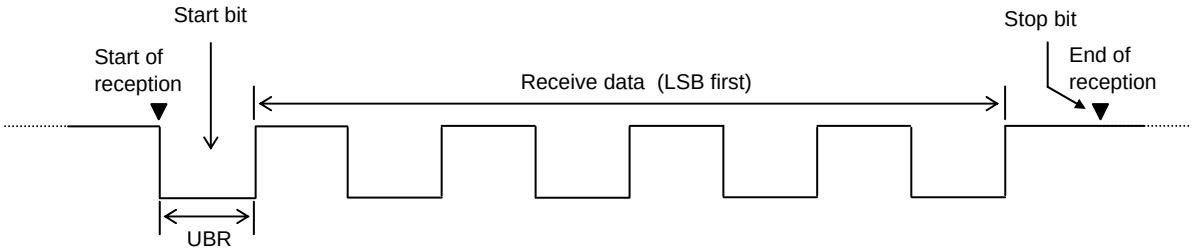
| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Transfer rate | UBR | UTX(P20)<br>URX(P21) | | 1.8 to 5.5 | 16/3 | | 8192/3 | tCYC |

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)




Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator
■EPSON TOYOCOM

| Nominal Frequency | Type | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rf [Ω] | Rd [Ω] | | typ [s] | max [s] | |
| 32.768kHz | SMD | MC-306 | 9 | 9 | Open | 330k | 1.8 to 5.5 | 1.4 | 4.0 | Applicable CL value = 7.0pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 3).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

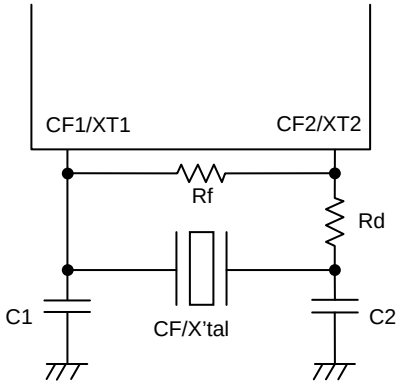



Figure 1 CF and XT Oscillator Circuit

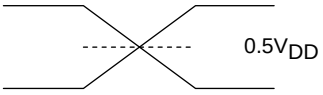
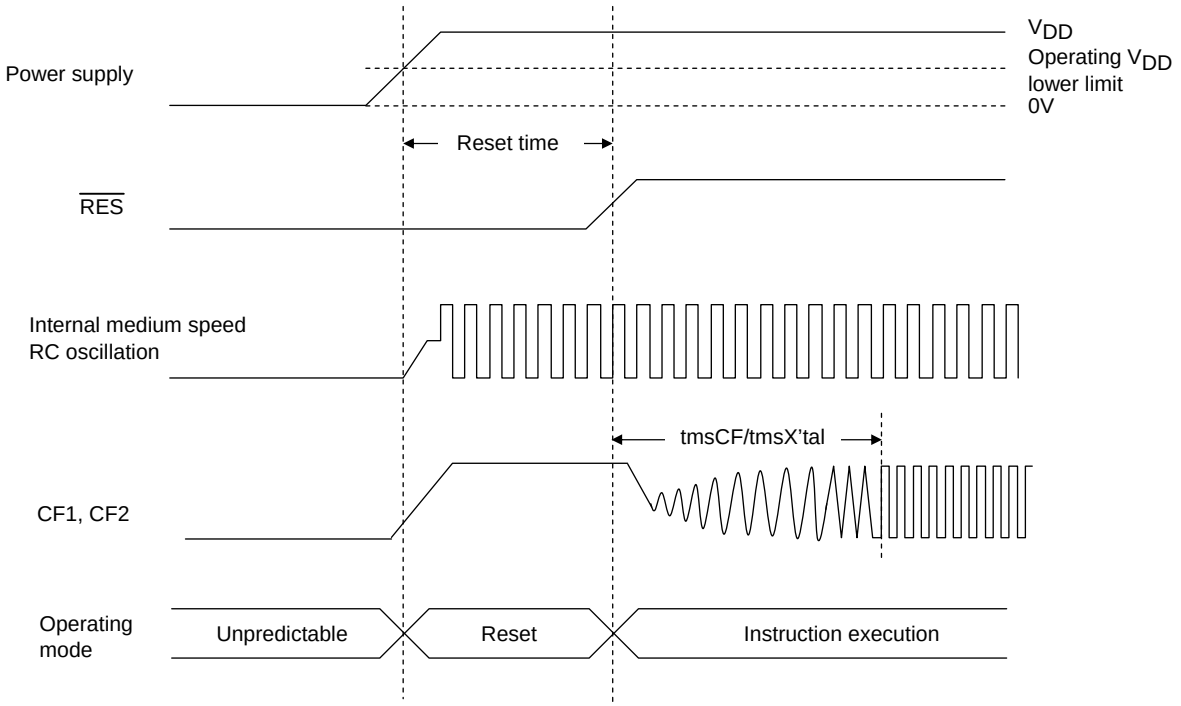
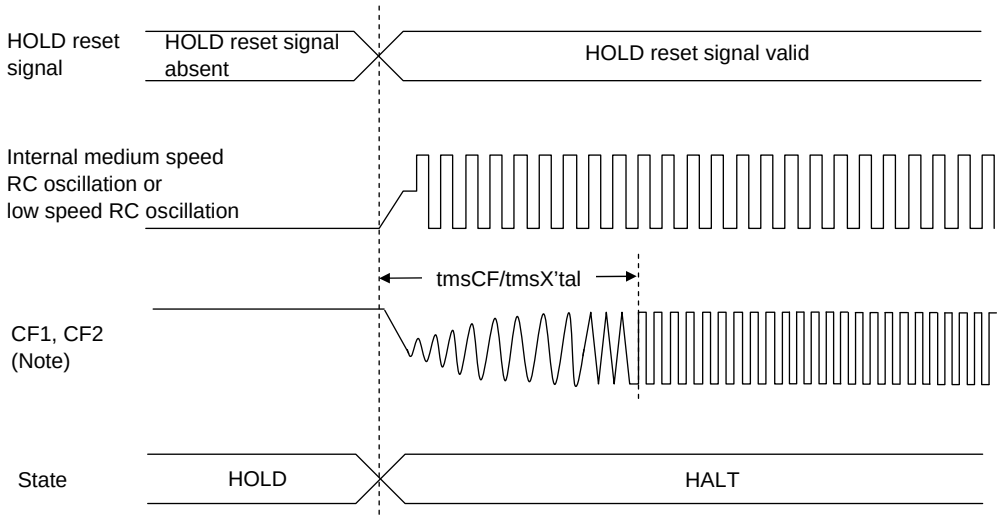



Figure 2 AC Timing Measurement Point




Reset Time and Oscillation Stabilization Time




HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times

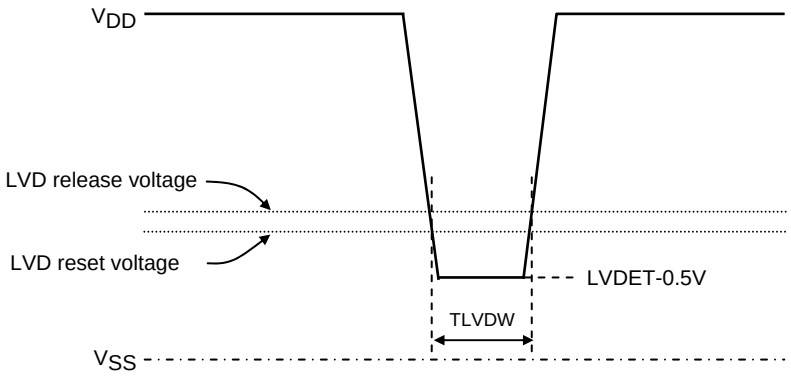



Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)