Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy9af115mapmc-g-mne2

Watch dog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except STOP modes.

External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 fast General Purpose I/O Ports@ 100pin Package
- Some ports are 5V tolerant I/O (MB9AF115MA/NA, MB9AF116MA/NA only)
  Please see "Pin Description" to confirm the corresponding pins.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- Built-in High-speed CR Clock : 4 MHz
- Built-in Low-speed CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock Supervisor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three Low-Power Consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug

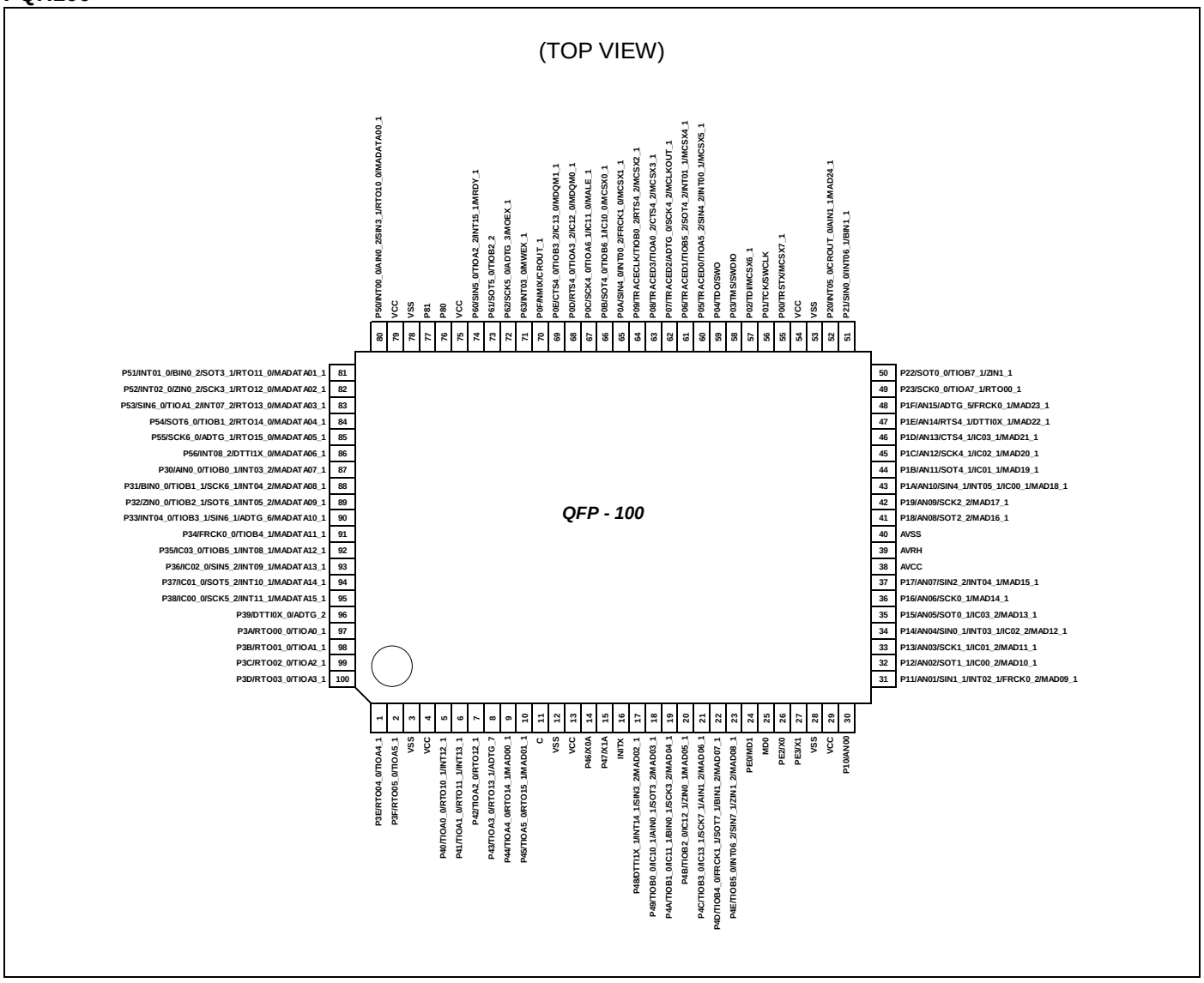
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM)*
  *: Mb9AF111LA/MA, F112LA/MA, F114LA/MA, F115MA and F116MA support only SWJ-DP.

Power Supply

- VCC = 2.7V to 5.5V: Correspond to the wide range voltage.

Contents

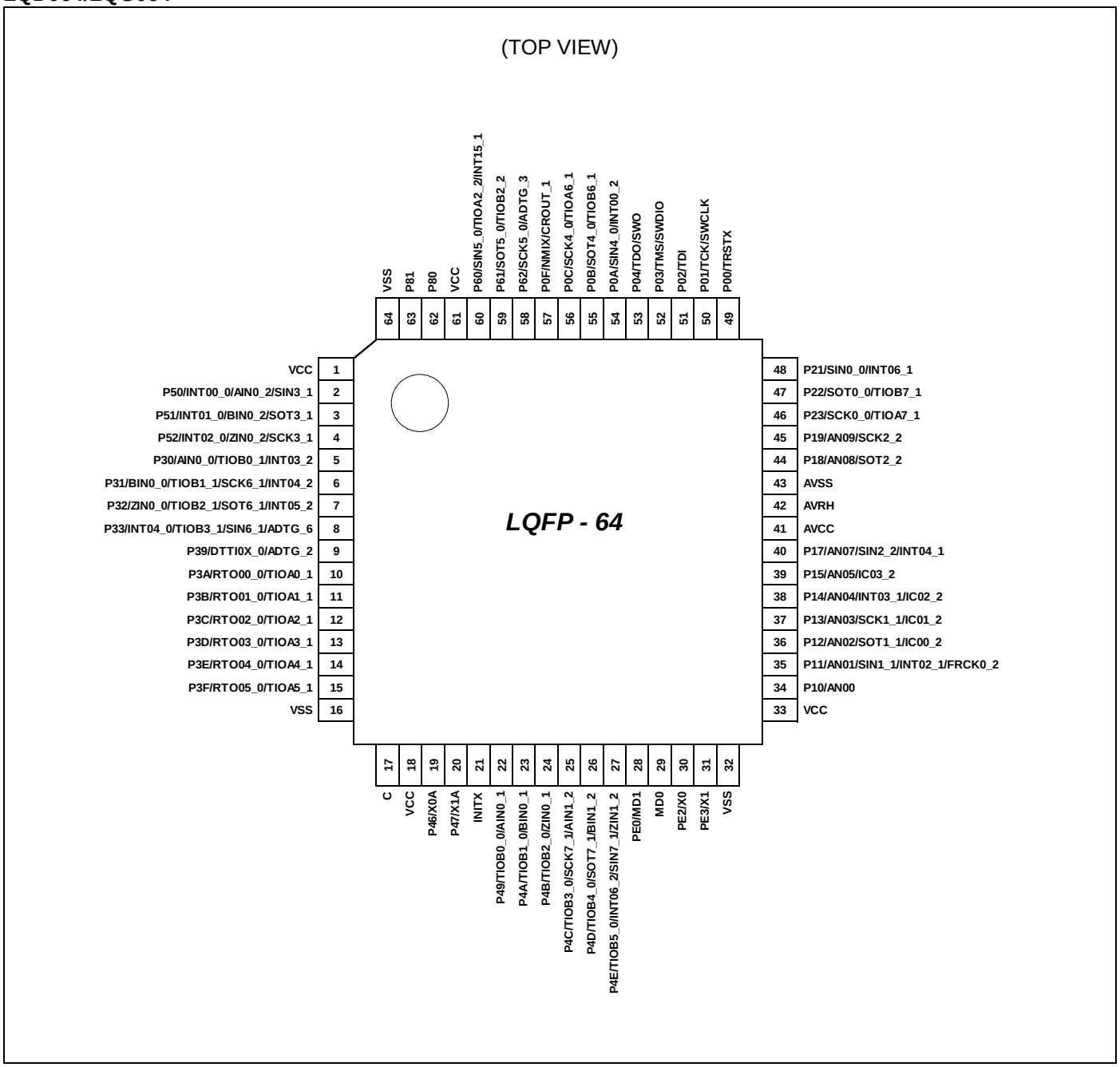
PQH100



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQD064/LQG064



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
23	1	H3	18	14	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	2	J2	19	15	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	3	L1	20	16	VSS	-	
26	4	J1	-	-	VCC	-	
27	5	J4	-	-	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	H
28	6	L5	-	-	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	H
29	7	K5	-	-	P42 TIOA2_0 RTO12_1 (PPG12_1)	G	I
30	8	J5	-	-	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7	G	I
31	9	H5	21 -	-	P44 TIOA4_0 MAD00_1 RTO14_1 (PPG14_1)	G	I
32	10	L6	22 -	-	P45 TIOA5_0 MAD01_1 RTO15_1 (PPG14_1)	G	I
-	-	K2	-	-	VSS	-	
-	-	J3	-	-	VSS	-	
-	-	H4	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
44	22	J7	34	26	P4D	E / I*	I
					TIOB4_0		
					SOT7_1 (SDA7_1)		
					BIN1_2		
				-	FRCK1_1		
					MAD07_1		
45	23	K8	35	27	P4E	E / I*	I
					TIOB5_0		
					INT06_2		
					SIN7_1		
					ZIN1_2		
				-	MAD08_1		
46	24	K9	36	28	MD1	C	P
					PE0		
47	25	L8	37	29	MD0	J	D
48	26	L9	38	30	X0	A	A
					PE2		
49	27	L10	39	31	X1	A	B
					PE3		
50	28	L11	40	32	VSS	-	
51	29	K11	41	33	VCC	-	
52	30	J11	42	34	P10	F	K
					AN00		
53	31	J10	43	35	P11	F	L
					AN01		
					SIN1_1		
					INT02_1		
					FRCK0_2		
				-	MAD09_1		
54	32	J8	44	36	P12	F	K
					AN02		
					SOT1_1 (SDA1_1)		
					IC00_2		
				-	MAD10_1		
-	-	K10	-	-	VSS	-	
-	-	J9	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
65	43	F9	55	-	P1A AN10 SIN4_1 INT05_1 IC00_1 MAD18_1	F	L
66	44	E11	56	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_1	F	K
67	45	E10	-	-	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_1	F	K
68	46	F8	-	-	P1D AN13 CTS4_1 IC03_1 MAD21_1	F	K
69	47	E9	-	-	P1E AN14 RTS4_1 DTTI0X_1 MAD22_1	F	K
70	48	D11	-	-	P1F AN15 ADTG_5 FRCK0_1 MAD23_1	F	K
-	-	B10	-	-	VSS	-	
-	-	C9	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
90	68	C6	70	-	P0D	E	I
					RTS4_0		
					TIOA3_2		
					IC12_0		
					MDQM0_1		
91	69	A5	71	-	P0E	E	I
					CTS4_0		
					TIOB3_2		
					IC13_0		
					MDQM1_1		
92	70	B5	72	57	P0F	E	J
					NMIX		
					CROUT_1		
93	71	D6	73	-	P63	E	H
					INT03_0		
					MWEX_1		
94	72	C5	74	58	P62	E	I
					SCK5_0 (SCL5_0)		
					ADTG_3		
				-	MOEX_1		
95	73	B4	75	59	P61	E	I
					SOT5_0 (SDA5_0)		
					TIOB2_2		
96	74	C4	76	60	P60	E / I*	H
					SIN5_0		
					TIOA2_2		
					INT15_1		
				-	MRDY_1		
97	75	A4	77	61	VCC	-	
98	76	A3	78	62	P80	H	O
99	77	A2	79	63	P81	H	O
100	78	A1	80	64	VSS	-	

*: 5V tolerant I/O on MB9AF115MA/NA and MB9AF116MA/NA

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	-
	ADTG_1		7	85	D3	7	-
	ADTG_2		18	96	F4	13	9
	ADTG_3		94	72	C5	74	58
	ADTG_4		-	-	-	-	-
	ADTG_5		70	48	D11	-	-
	ADTG_6		12	90	E4	12	8
	ADTG_7		30	8	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	30	J11	42	34
	AN01		53	31	J10	43	35
	AN02		54	32	J8	44	36
	AN03		55	33	H10	45	37
	AN04		56	34	H9	46	38
	AN05		57	35	H7	47	39
	AN06		58	36	G10	48	-
	AN07		59	37	G9	49	40
	AN08		63	41	G8	53	44
	AN09		64	42	F10	54	45
	AN10		65	43	F9	55	-
	AN11		66	44	E11	56	-
	AN12		67	45	E10	-	-
	AN13		68	46	F8	-	-
	AN14		69	47	E9	-	-
	AN15		70	48	D11	-	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-
	TIOA0_1		19	97	G3	14	10
	TIOA0_2		85	63	B7	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	22
	TIOB0_1		9	87	E1	9	5
	TIOB0_2		86	64	C7	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-
	TIOA1_1		20	98	H1	15	11
	TIOA1_2		5	83	D1	5	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	23
	TIOB1_1		10	88	E2	10	6
	TIOB1_2		6	84	D2	6	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Debugger	SWCLK	Serial wire debug interface clock input	78	56	B9	62	50
	SWDIO	Serial wire debug interface data input / output	80	58	A8	64	52
	SWO	Serial wire viewer output	81	59	B8	65	53
	TCK	JTAG test clock input	78	56	B9	62	50
	TDI	JTAG test data input	79	57	B11	63	51
	TDO	JTAG debug data output	81	59	B8	65	53
	TMS	JTAG test mode state input/output	80	58	A8	64	52
	TRACECLK	Trace CLK output of ETM	86	64	C7	-	-
	TRACED0	Trace data output of ETM	82	60	C8	-	-
	TRACED1		83	61	D9	-	-
	TRACED2		84	62	A7	-	-
	TRACED3		85	63	B7	-	-
	TRSTX	JTAG test reset input	77	55	A9	61	49
External Bus	MAD00_1	External bus interface address bus	31	9	H5	21	-
	MAD01_1		32	10	L6	22	-
	MAD02_1		39	17	K6	29	-
	MAD03_1		40	18	J6	30	-
	MAD04_1		41	19	L7	31	-
	MAD05_1		42	20	K7	32	-
	MAD06_1		43	21	H6	33	-
	MAD07_1		44	22	J7	34	-
	MAD08_1		45	23	K8	35	-
	MAD09_1		53	31	J10	43	-
	MAD10_1		54	32	J8	44	-
	MAD11_1		55	33	H10	45	-
	MAD12_1		56	34	H9	46	-
	MAD13_1		57	35	H7	47	-
	MAD14_1		58	36	G10	48	-
	MAD15_1		59	37	G9	49	-
	MAD16_1		63	41	G8	53	-
	MAD17_1		64	42	F10	54	-
	MAD18_1		65	43	F9	55	-
	MAD19_1		66	44	E11	56	-
	MAD20_1		67	45	E10	-	-
	MAD21_1		68	46	F8	-	-
	MAD22_1		69	47	E9	-	-
	MAD23_1		70	48	D11	-	-
	MAD24_1		74	52	C10	60	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
External Interrupt	INT00_0	External interrupt request 00 input pin	2	80	C1	2	2
	INT00_1		82	60	C8	-	-
	INT00_2		87	65	D7	67	54
	INT01_0	External interrupt request 01 input pin	3	81	C2	3	3
	INT01_1		83	61	D9	-	-
	INT02_0	External interrupt request 02 input pin	4	82	B3	4	4
	INT02_1		53	31	J10	43	35
	INT03_0	External interrupt request 03 input pin	93	71	D6	73	-
	INT03_1		56	34	H9	46	38
	INT03_2		9	87	E1	9	5
	INT04_0	External interrupt request 04 input pin	12	90	E4	12	8
	INT04_1		59	37	G9	49	40
	INT04_2		10	88	E2	10	6
	INT05_0	External interrupt request 05 input pin	74	52	C10	60	-
	INT05_1		65	43	F9	55	-
	INT05_2		11	89	E3	11	7
	INT06_1	External interrupt request 06 input pin	73	51	C11	59	48
	INT06_2		45	23	K8	35	27
	INT07_2	External interrupt request 07 input pin	5	83	D1	5	-
	INT08_1	External interrupt request 08 input pin	14	92	F2	-	-
	INT08_2		8	86	D5	8	-
	INT09_1	External interrupt request 09 input pin	15	93	F3	-	-
	INT10_1	External interrupt request 10 input pin	16	94	G1	-	-
	INT11_1	External interrupt request 11 input pin	17	95	G2	-	-
	INT12_1	External interrupt request 12 input pin	27	5	J4	-	-
	INT13_1	External interrupt request 13 input pin	28	6	L5	-	-
	INT14_1	External interrupt request 14 input pin	39	17	K6	29	-
	INT15_1	External interrupt request 15 input pin	96	74	C4	76	60
	NMIX	Non-Maskable Interrupt input	92	70	B5	72	57

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 1	DTTI1X_0	Input signal of waveform generator to control outputs RTO10 to RTO15 of multi-function timer 1	8	86	D5	8	-
	DTTI1X_1		39	17	K6	29	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	65	D7	67	-
	FRCK1_1		44	22	J7	34	-
	IC10_0	16-bit input capture input pin of multi-function timer 1. ICxx describes channel number.	88	66	A6	68	-
	IC10_1		40	18	J6	30	-
	IC11_0		89	67	B6	69	-
	IC11_1		41	19	L7	31	-
	IC12_0		90	68	C6	70	-
	IC12_1		42	20	K7	32	-
	IC13_0		91	69	A5	71	-
	IC13_1		43	21	H6	33	-
	RTO10_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	2	80	C1	2	-
	RTO10_1 (PPG10_1)		27	5	J4	-	-
	RTO11_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	3	81	C2	3	-
	RTO11_1 (PPG10_1)		28	6	L5	-	-
	RTO12_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	4	82	B3	4	-
	RTO12_1 (PPG12_1)		29	7	K5	-	-
	RTO13_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	5	83	D1	5	-
	RTO13_1 (PPG12_1)		30	8	J5	-	-
	RTO14_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	6	84	D2	6	-
	RTO14_1 (PPG14_1)		31	9	H5	21	-
	RTO15_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	7	85	D3	7	-
	RTO15_1 (PPG14_1)		32	10	L6	22	-

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enabled	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0"
O	GPIO pin	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/Input enabled

*1: Oscillation is stopped at sub timer mode, low-speed CR timer mode, and stop mode.

*2: Oscillation is stopped at stop mode.

12.3 DC Characteristics

12.3.1 Current rating

(V_{CC} = AV_{CC}= 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
RUN mode current	I_{CC}	VCC	PLL RUN mode	CPU : 40MHz, Peripheral : 40MHz, Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *5	32	41	mA	*1
				CPU : 40MHz, Peripheral : 40MHz, Flash 3Wait FRWTR.RWT = 00 FSYNDN.SD = 011 *5	21	28	mA	*1
			High-speed CR RUN mode	CPU/ Peripheral : 4MHz*2 Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	3.9	7.7	mA	*1
			Sub RUN mode	CPU/ Peripheral : 32kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *6	0.15	3.2	mA	*1
			Low-speed CR RUN mode	CPU/ Peripheral : 100kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.2	3.3	mA	*1
SLEEP mode current	I_{CCS}		PLL SLEEP mode	Peripheral : 40MHz *5	10	15	mA	*1
			High-speed CR SLEEP mode	Peripheral : 4MHz*2	1.2	4.4	mA	*1
			Sub SLEEP mode	Peripheral : 32kHz *6	0.1	3.1	mA	*1
			Low-speed CR SLEEP mode	Peripheral : 100kHz	0.1	3.1	mA	*1

*1: When all ports are fixed.

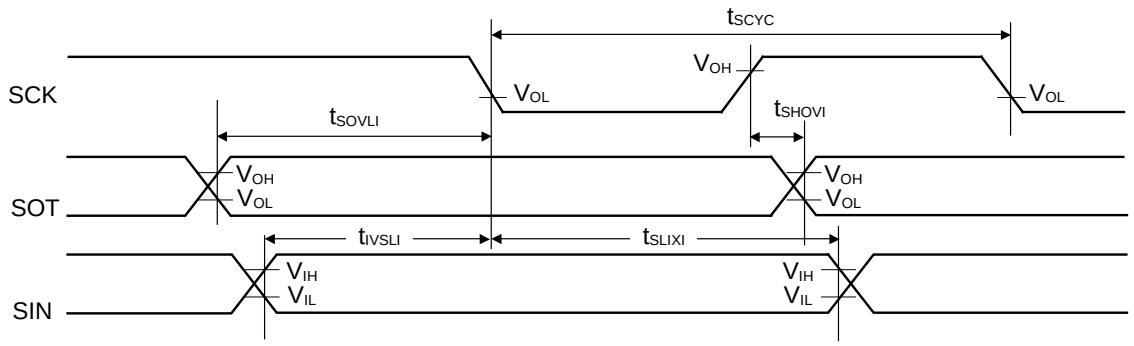
*2: When setting it to 4MHz by trimming.

*3: T_A =+25°C, V_{CC}=5.5V

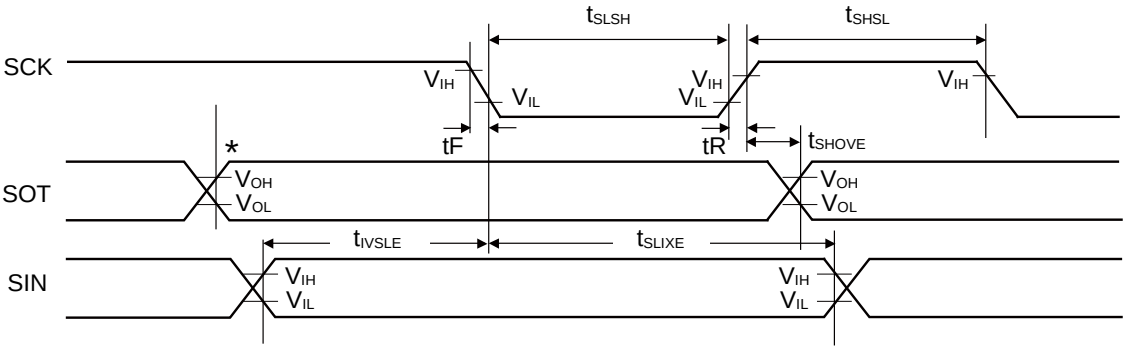
*4: T_A =+105°C, V_{CC}=5.5V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)



Master mode



Slave mode

*: Changes when writing to TDR register

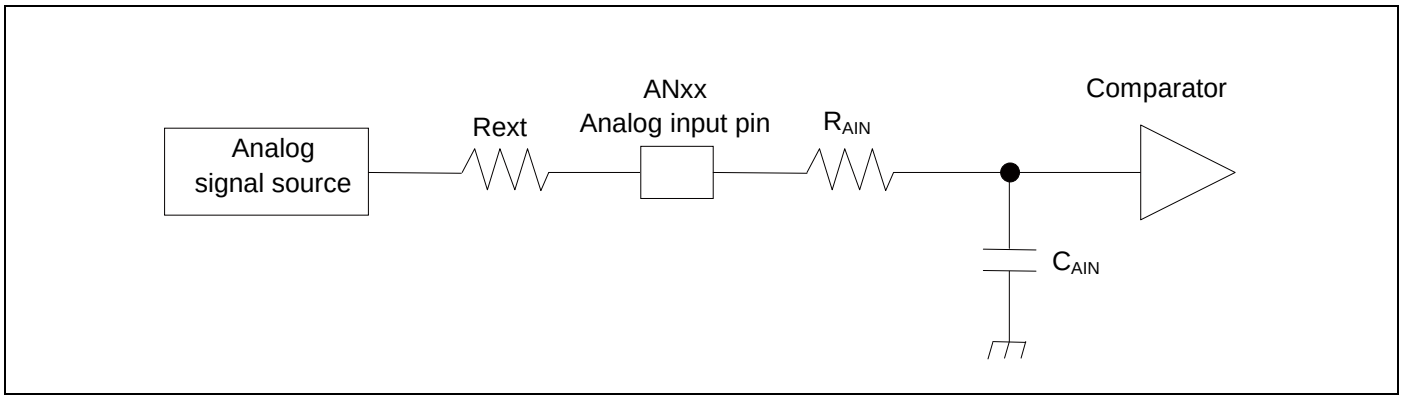
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓⟶ SOT delay time	t_{SLOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑⟶SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT ⟶ SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ ⟶ SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑⟶ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L= 30pF.



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts	: Sampling time	
R_{AIN}	: input resistor of A/D = 2kΩ	$4.5 \leq AV_{CC} \leq 5.5$
	input resistor of A/D = 3.8kΩ	$2.7 \leq AV_{CC} < 4.5$
C_{AIN}	:input capacity of A/D = 12.9pF	$2.7 \leq AV_{CC} \leq 5.5$
Rext	: Output impedance of external circuit	

(Equation 2) $Tc = Tcck \times 14$

Tc	: Compare time
Tcck	: Compare clock cycle