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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af111lapmc-g-jne2

External Bus Interface*

- Supports SRAM, NOR Flash device
- Up to 8 chip selects
- 8/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size : Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY function

*: MB9AF111LA, F312LA and F314LA do not support External Bus Interface

DMA Controller (8 channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32bit (4Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 16 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3units*
- Conversion time: 1.0μs@5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4steps)

*: MB9AF111LA, F112LA, F114LA built-in 2units

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Multi-function Timer (Max 2 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activation compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead timer function
- Input capture function
- A/D converter activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 2 units)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each timer channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from Low-Power Consumption mode.

- Interval timer: up to 64s(Max)@ Sub Clock : 32.768kHz

1. Product Lineup

Memory Size

Product name	MB9AF111LA/MA/NA	MB9AF112LA/MA/NA MB9AF112L	MB9AF114LA/MA/NA MB9AF114L
On-chip Flash memory	64Kbytes	128Kbytes	256Kbytes
On-chip SRAM	16Kbytes	16Kbytes	32Kbytes

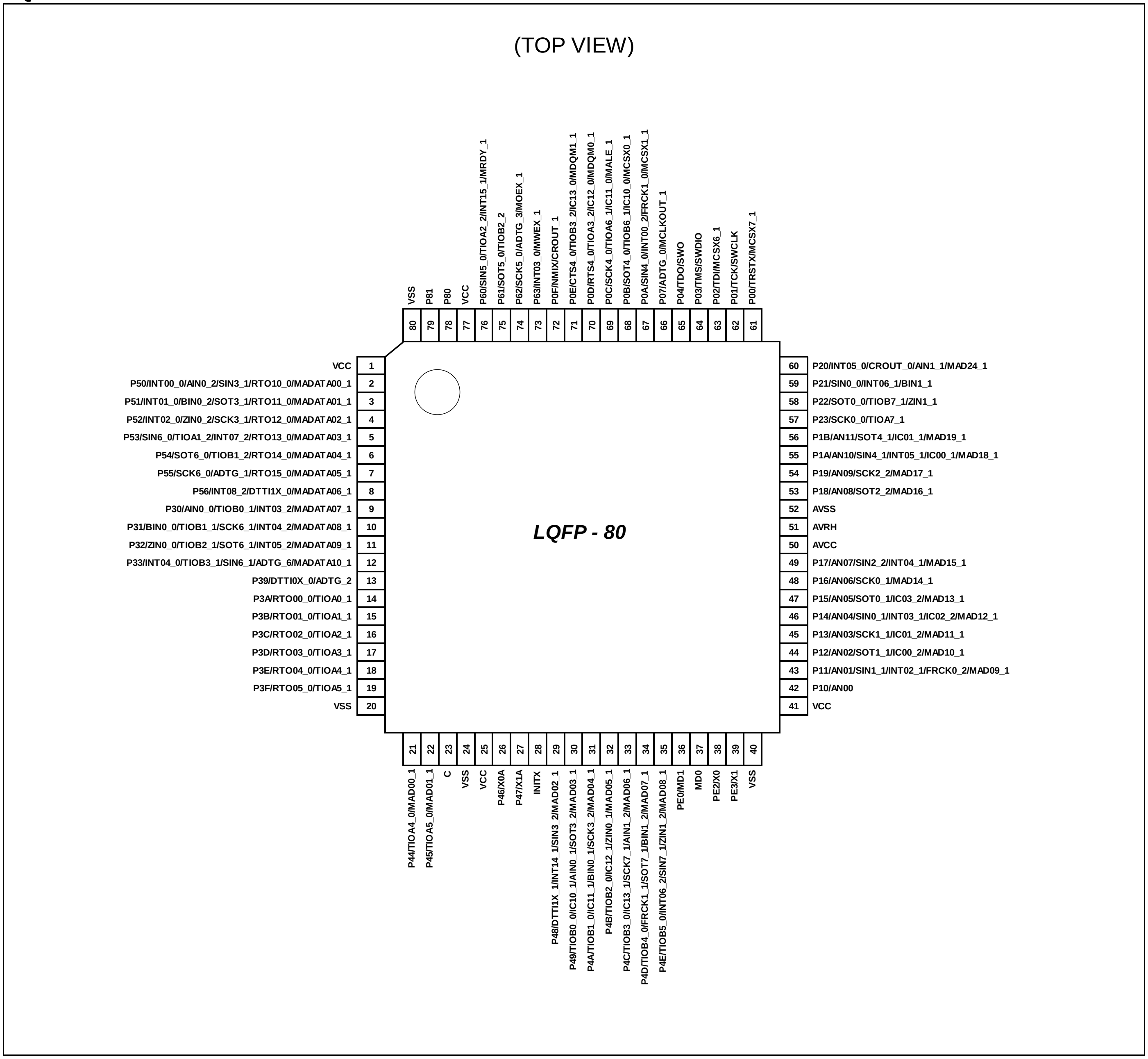
Product name	MB9AF115MA/NA	MB9AF116MA/NA
On-chip Flash memory	384Kbytes	512Kbytes
On-chip SRAM	32Kbytes	32Kbytes

Function

Product name			MB9AF111LA MB9AF112LA MB9AF114LA MB9AF112L MB9AF114L	MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA	MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA
Pin count			64	80	100
CPU			Cortex-M3		
	Freq.		40MHz		
Power supply voltage range			2.7V to 5.5V		
DMAC			8ch.		
External Bus Interface			-	Addr:21-bit (Max) Data:8-bit CS:4 (Max) Support: SRAM, NOR Flash	Addr:25-bit (Max) Data:8/16-bit CS:8 (Max) Support: SRAM, NOR Flash
Multi-function Serial Interface (UART/CSIO/LIN/I²C)			8ch. (Max) ch.4 to ch.7: FIFO (16steps x 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF-Timer	A/D activation compare	3ch.	1 unit	2 units (Max)	
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
QPRC			2ch. (Max)		
Dual Timer			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			8 pins (Max) + NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O ports			51 pins (Max)	66 pins (Max)	83 pins (Max)
12-bit A/D converter			9ch. (2 units)	12ch. (3 units)	16ch. (3 units)
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP		SWJ-DP/ETM

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the I/O port according to your function use.
See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

LQH080



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LBC112

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	P81	P80	VCC	P0E	P0B	P07	TMS/ SWDIO	TRSTX	VCC	VSS
B	VCC	VSS	P52	P61	P0F	P0C	P08	TDO/ SWO	TCK/ SWCLK	VSS	TDI
C	P50	P51	VSS	P60	P62	P0D	P09	P05	VSS	P20	P21
D	P53	P54	P55	VSS	P56	P63	P0A	VSS	P06	P23	AN15
E	P30	P31	P32	P33	Index			P22	AN14	AN12	AN11
F	P34	P35	P36	P39				AN13	AN10	AN09	AVRH
G	P37	P38	P3A	P3D				AN08	AN07	AN06	AVSS
H	P3B	P3C	P3E	VSS	P44	P4C	AN05	VSS	AN04	AN03	AVCC
J	VCC	P3F	VSS	P40	P43	P49	P4D	AN02	VSS	AN01	AN00
K	VCC	VSS	X1A	INITX	P42	P48	P4B	P4E	MD1	VSS	VCC
L	VSS	C	X0A	VSS	P41	P45	P4A	MD0	X0	X1	VSS

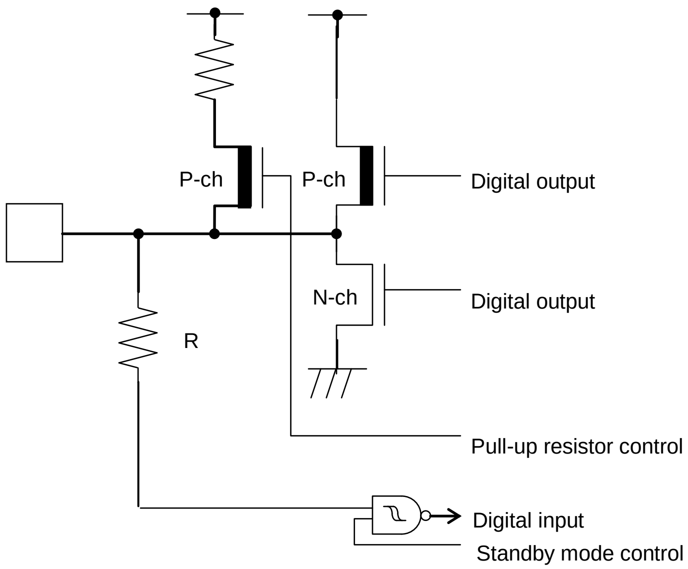
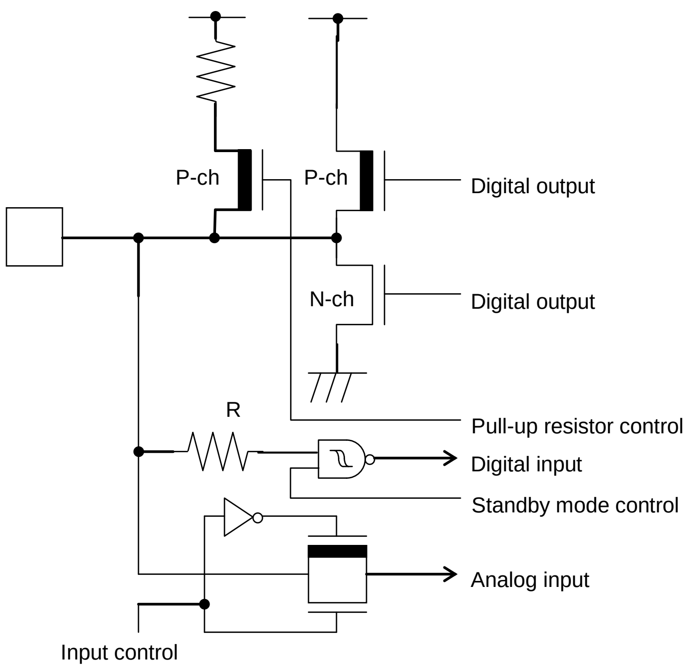
Note:

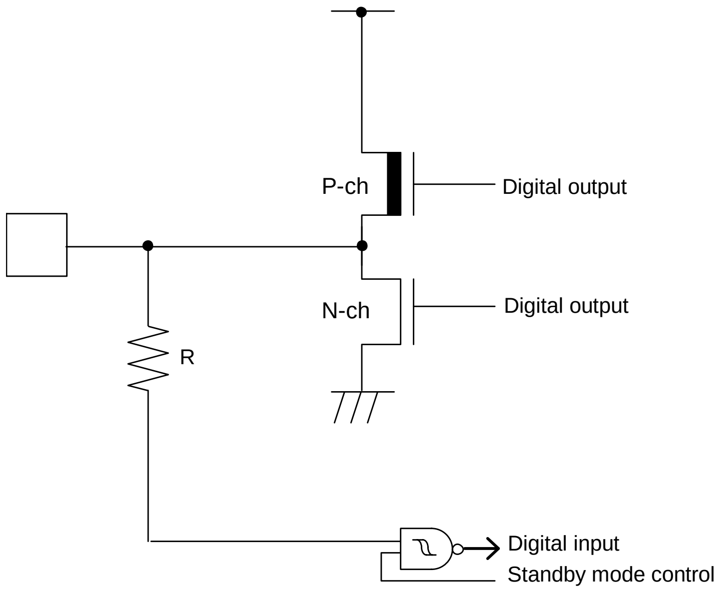
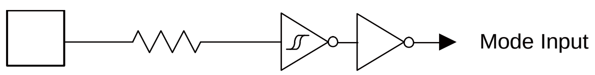
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P30	General-purpose I/O port 3	9	87	E1	9	5
	P31		10	88	E2	10	6
	P32		11	89	E3	11	7
	P33		12	90	E4	12	8
	P34		13	91	F1	-	-
	P35		14	92	F2	-	-
	P36		15	93	F3	-	-
	P37		16	94	G1	-	-
	P38		17	95	G2	-	-
	P39		18	96	F4	13	9
	P3A		19	97	G3	14	10
	P3B		20	98	H1	15	11
	P3C		21	99	H2	16	12
	P3D		22	100	G4	17	13
	P3E		23	1	H3	18	14
	P3F		24	2	J2	19	15
	P40	General-purpose I/O port 4	27	5	J4	-	-
	P41		28	6	L5	-	-
	P42		29	7	K5	-	-
	P43		30	8	J5	-	-
	P44		31	9	H5	21	-
	P45		32	10	L6	22	-
	P46		36	14	L3	26	19
	P47		37	15	K3	27	20
	P48		39	17	K6	29	-
	P49		40	18	J6	30	22
	P4A		41	19	L7	31	23
	P4B		42	20	K7	32	24
	P4C		43	21	H6	33	25
	P4D		44	22	J7	34	26
	P4E		45	23	K8	35	27
	P50	General-purpose I/O port 5	2	80	C1	2	2
	P51		3	81	C2	3	3
	P52		4	82	B3	4	4
	P53		5	83	D1	5	-
	P54		6	84	D2	6	-
	P55		7	85	D3	7	-
	P56		8	86	D5	8	-
	P60	General-purpose I/O port 6	96	74	C4	76	60
	P61		95	73	B4	75	59
	P62		94	72	C5	74	58
	P63		93	71	D6	73	-
	P80	General-purpose I/O port 8	98	76	A3	78	62
	P81		99	77	A2	79	63
	PE0	General-purpose I/O port E	46	24	K9	36	28
	PE2		48	26	L9	38	30
	PE3		49	27	L10	39	31

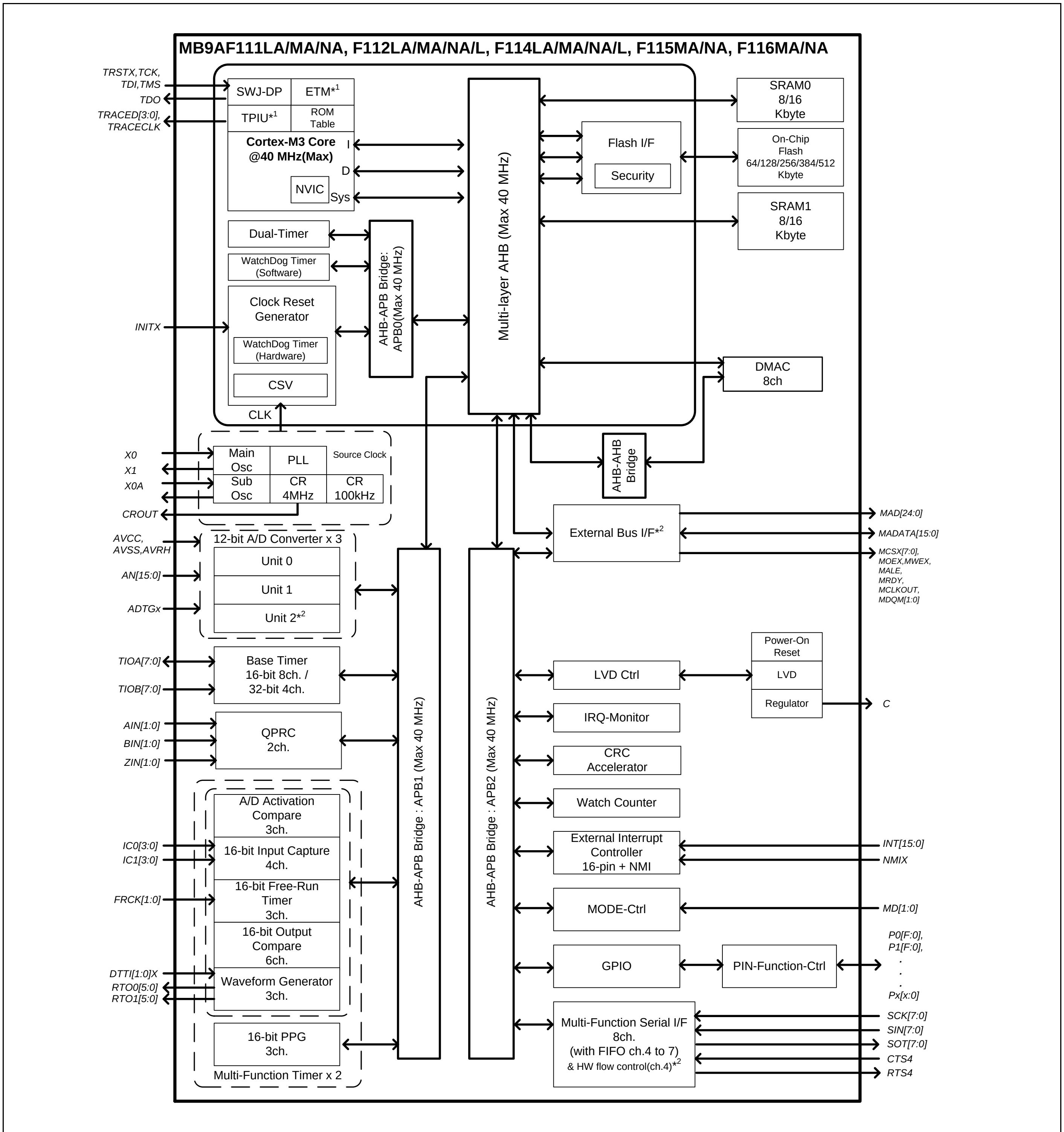
Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	87	65	D7	67	54
	SIN4_1		65	43	F9	55	-
	SIN4_2		82	60	C8	-	-
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	55
	SOT4_1 (SDA4_1)		66	44	E11	56	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	90	68	C6	70	-
	RTS4_1		69	47	E9	-	-
	RTS4_2		86	64	C7	-	-
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	91	69	A5	71	-
	CTS4_1		68	46	F8	-	-
	CTS4_2		85	63	B7	-	-
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	96	74	C4	76	60
	SIN5_2		15	93	F3	-	-
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 1	DTTI1X_0	Input signal of waveform generator to control outputs RTO10 to RTO15 of multi-function timer 1	8	86	D5	8	-
	DTTI1X_1		39	17	K6	29	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	65	D7	67	-
	FRCK1_1		44	22	J7	34	-
	IC10_0	16-bit input capture input pin of multi-function timer 1. ICxx describes channel number.	88	66	A6	68	-
	IC10_1		40	18	J6	30	-
	IC11_0		89	67	B6	69	-
	IC11_1		41	19	L7	31	-
	IC12_0		90	68	C6	70	-
	IC12_1		42	20	K7	32	-
	IC13_0		91	69	A5	71	-
	IC13_1		43	21	H6	33	-
	RTO10_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	2	80	C1	2	-
	RTO10_1 (PPG10_1)		27	5	J4	-	-
	RTO11_0 (PPG10_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output mode.	3	81	C2	3	-
	RTO11_1 (PPG10_1)		28	6	L5	-	-
	RTO12_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	4	82	B3	4	-
	RTO12_1 (PPG12_1)		29	7	K5	-	-
	RTO13_0 (PPG12_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output mode.	5	83	D1	5	-
	RTO13_1 (PPG12_1)		30	8	J5	-	-
	RTO14_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	6	84	D2	6	-
	RTO14_1 (PPG14_1)		31	9	H5	21	-
	RTO15_0 (PPG14_0)	Waveform generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output mode.	7	85	D3	7	-
	RTO15_1 (PPG14_1)		32	10	L6	22	-

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}=-4mA, I_{OL}=4mA • When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}=-4mA, I_{OL}=4mA • When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • I_{OH}=-4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input

8. Block Diagram



*1: For the MB9AF111LA/MA, F112LA/MA, MB9AF114LA/MA, MB9AF115MA and MB9AF116MA, ETM is not available.

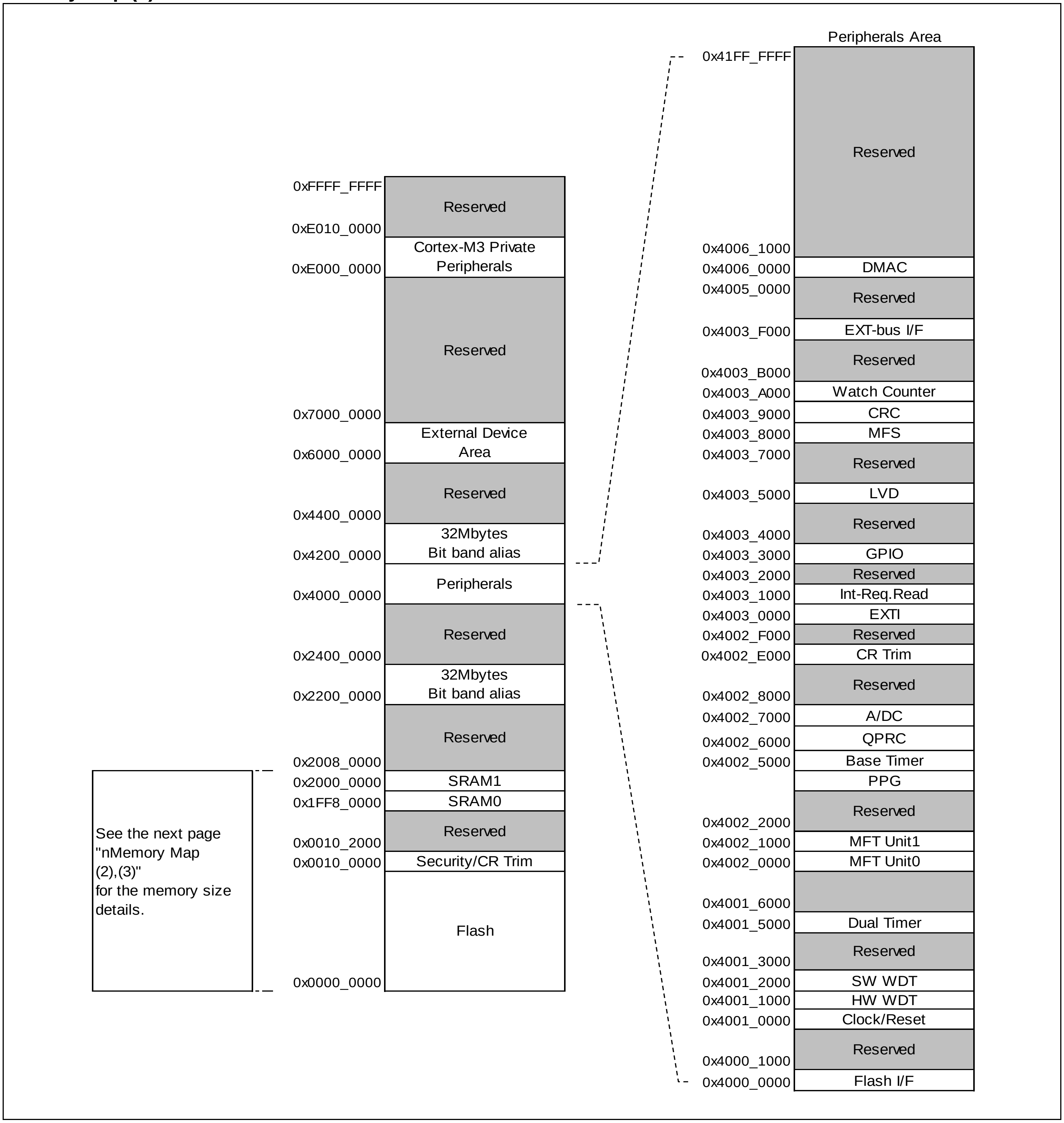
*2: For the MB9AF111LA, F112LA and MB9AF114LA, the External Bus Interface and 12-bit A/D Converter (unit 2) are not available. And the Multi-function Serial Interface does not support hardware flow control in these products.

9. Memory Size

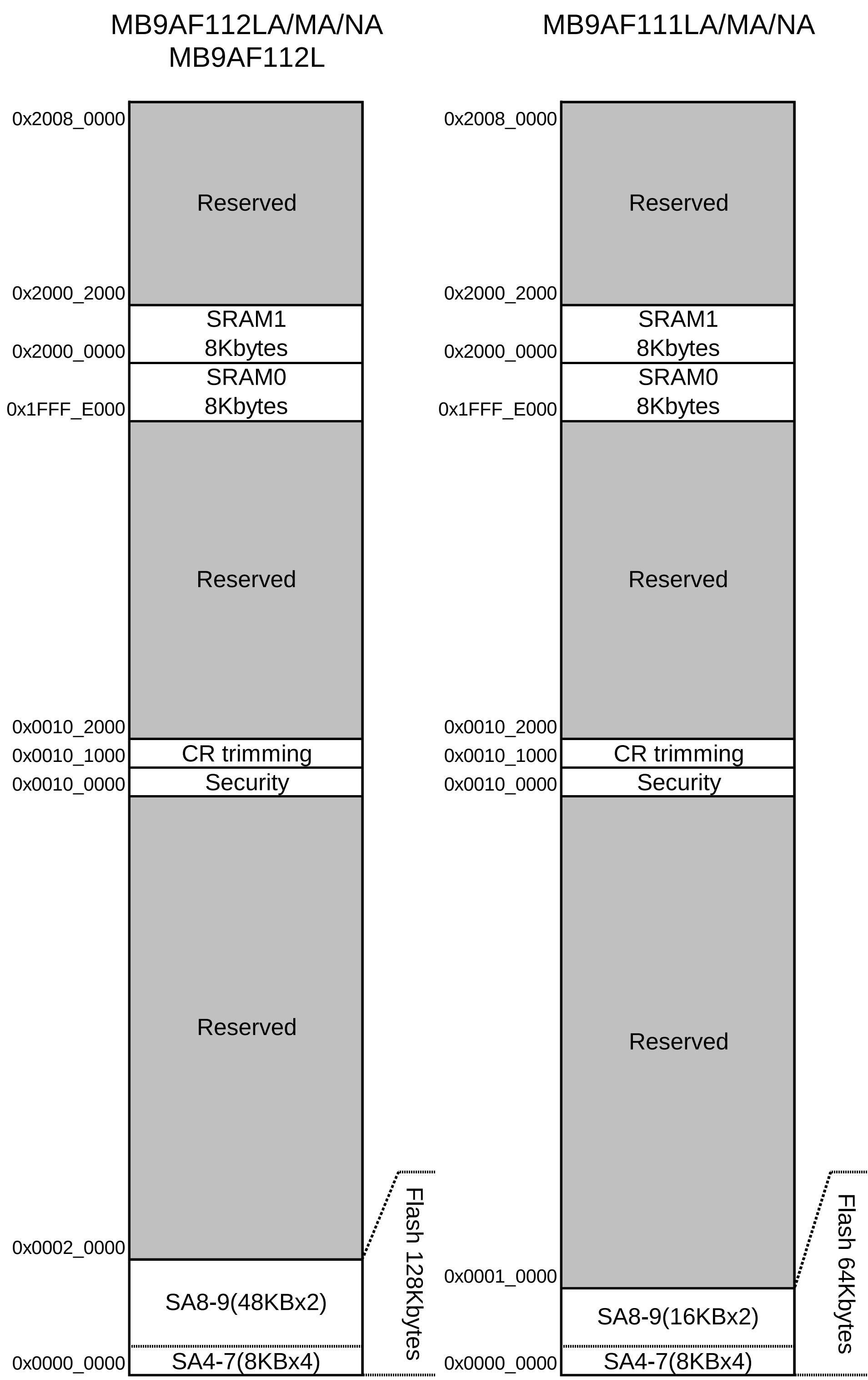
See “Memory Size” in “1. Product Lineup” to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (3)



*: See "MB9A310A/110A Series Flash programming Manual" for sector structure of Flash.

12.4.6 Reset Input Characteristics

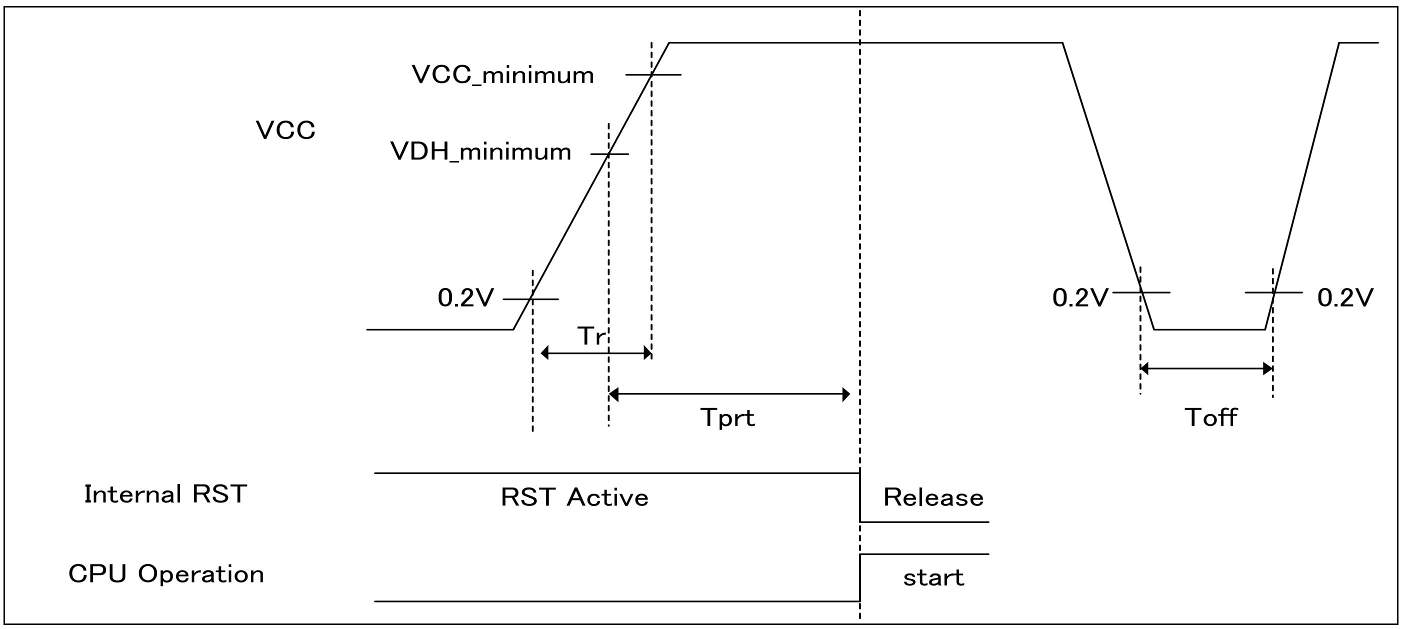
(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	V_{CC}	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.446	0.744	ms	

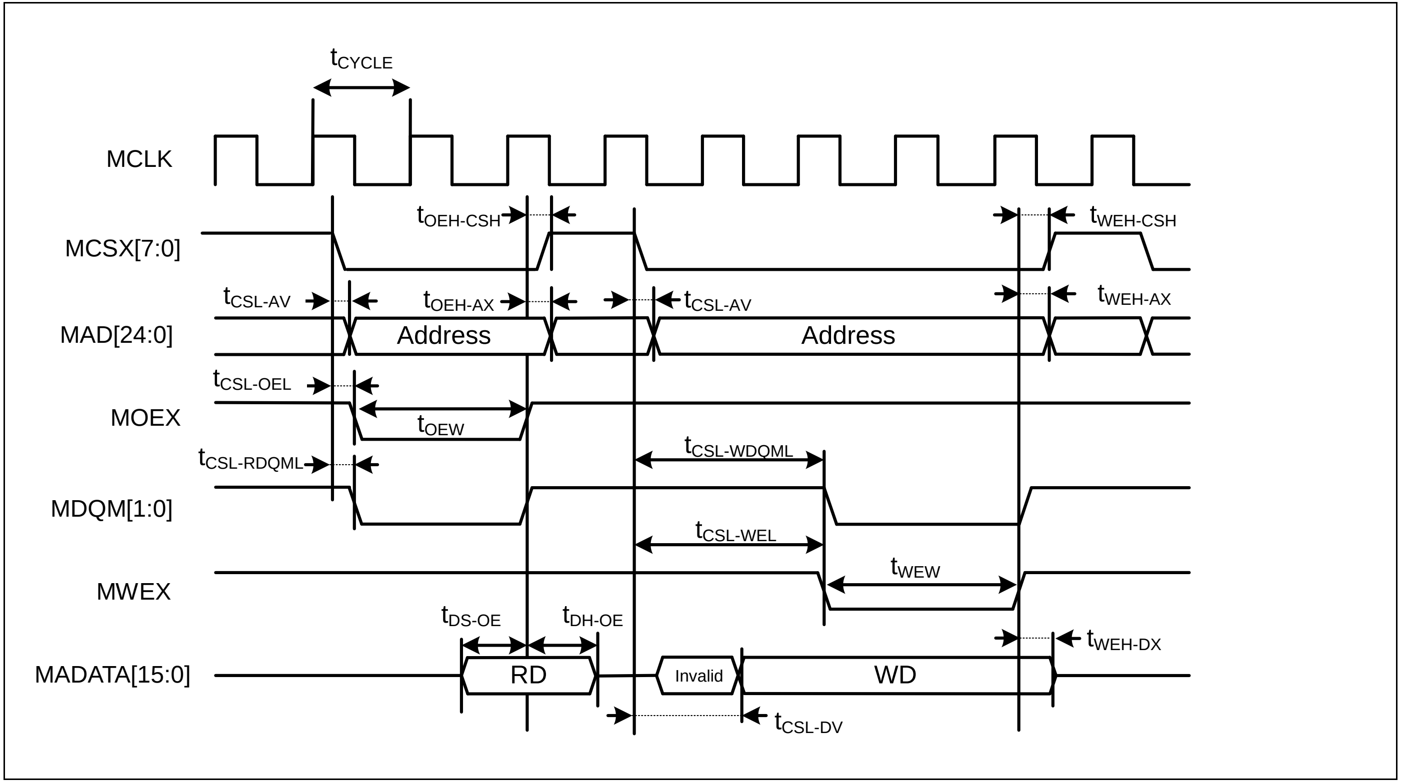


Glossary

VCC_minimum : Minimum V_{CC} of recommended operating conditions

VDH_minimum : Minimum release voltage of Low-Voltage detection reset

See "12.6. Low-voltage detection characteristics"


tCYCLE
MCLK
MCSX[7:0]
tOEH-CSH
tWEH-CSH
MAD[24:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MOEX
tCSL-OEL
tOEW
MDQM[1:0]
tCSL-RDQML
tCSL-WDQML
MWEX
tCSL-WEL
tWEW
MADATA[15:0]
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5V		$V_{CC} \geq$ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑→SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑→ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

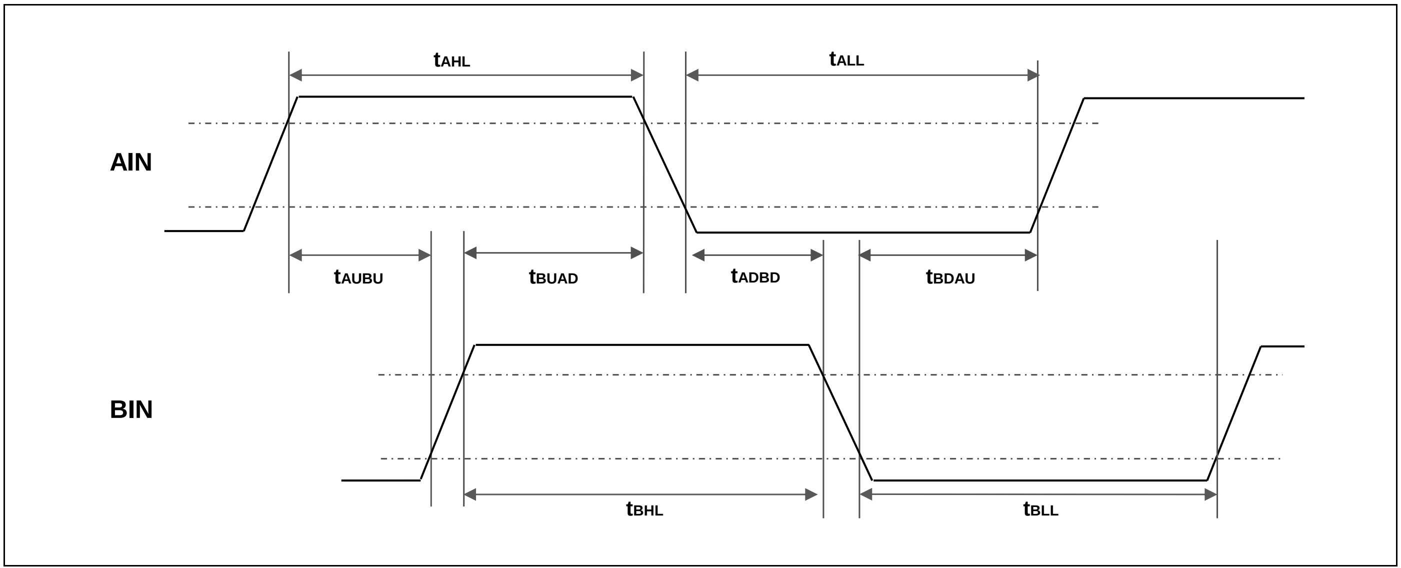
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L= 30pF.

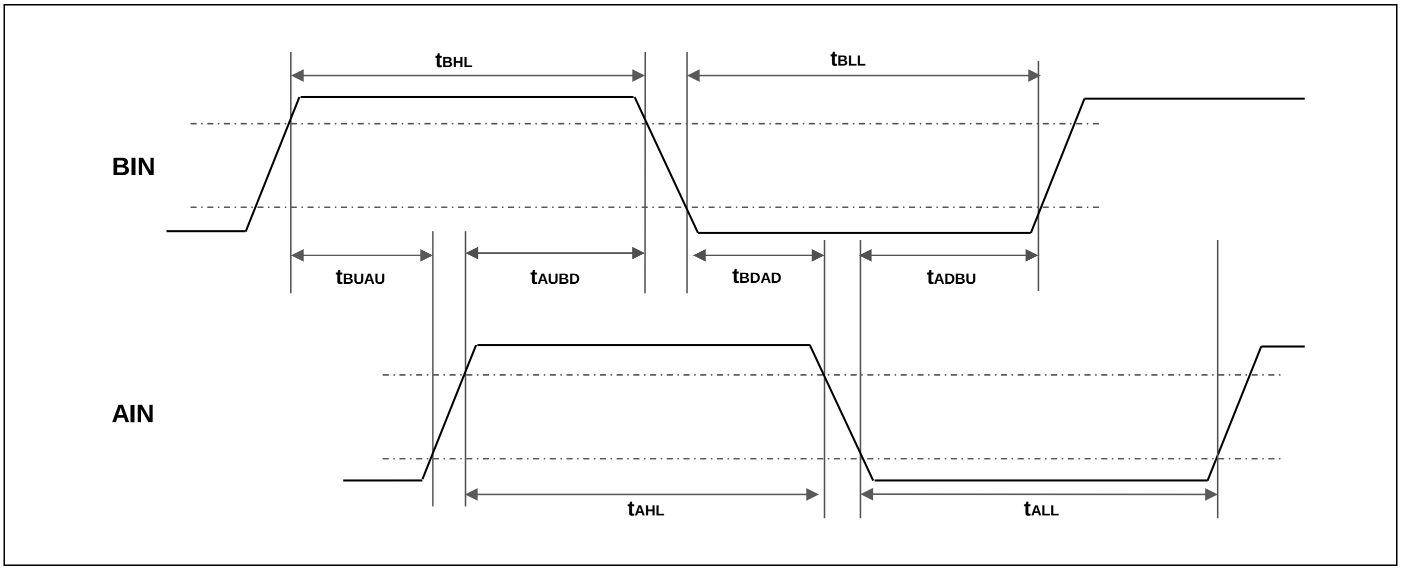
12.4.12 Quadrature Position/Revolution Counter timing

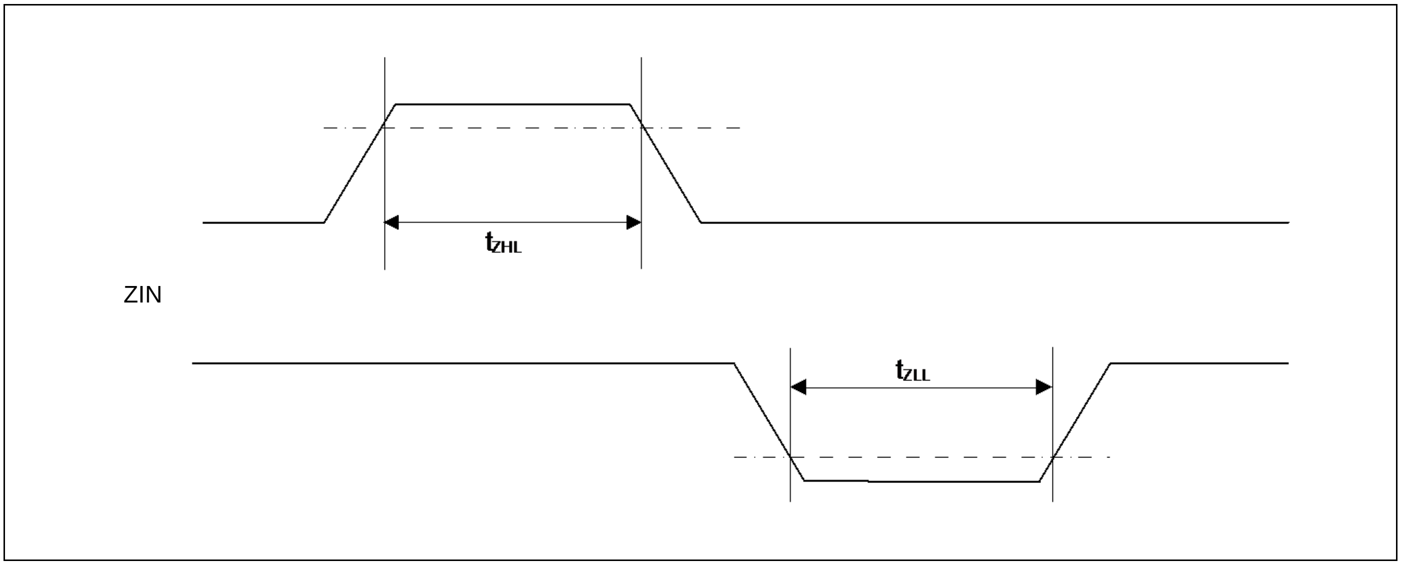
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

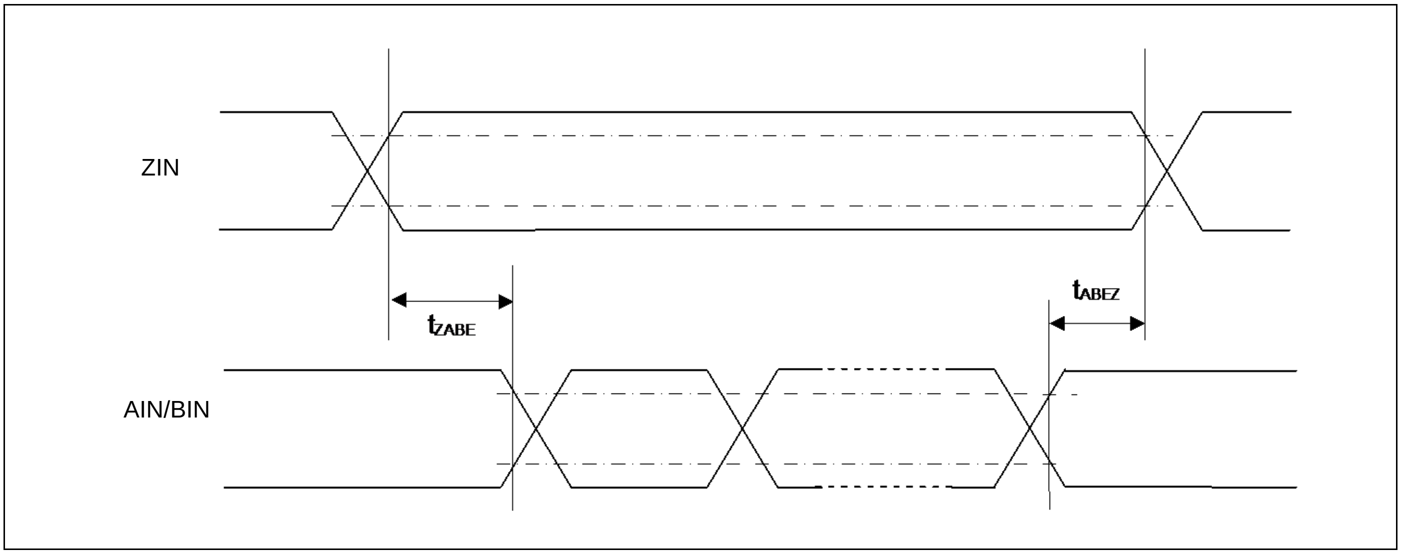
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	2t_{CYCP} *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC = "1"			

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL

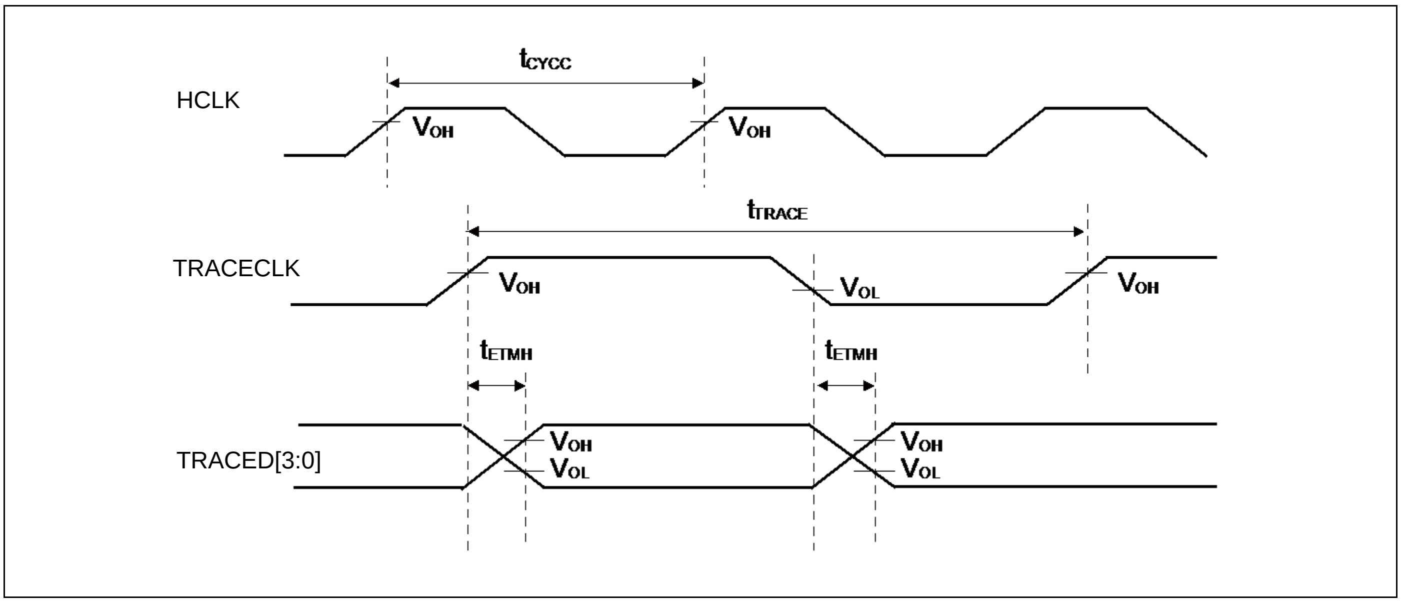

ZIN
tZABE
tABEZ
AIN/BIN

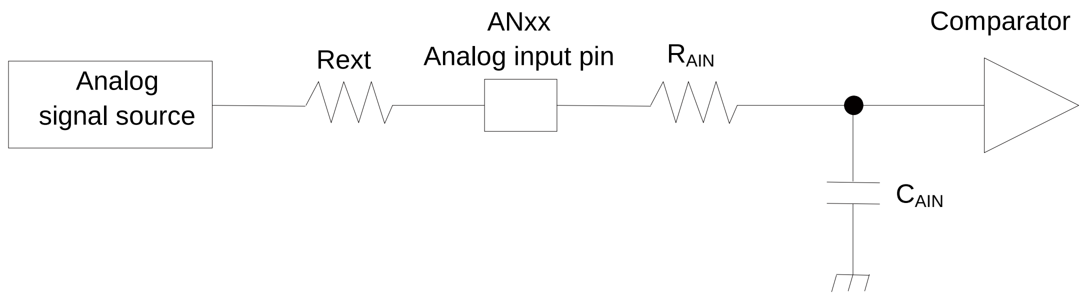
12.4.14 ETM timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED[3:0]	V_{CC}≥ 4.5V	2	9	ns	
			V_{CC}< 4.5V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	V_{CC}≥ 4.5V	-	40	MHz	
			V_{CC} < 4.5V	-	32	MHz	
TRACECLK Clock cycle time	t_{TRACE}		V_{CC}≥ 4.5V	25	-	ns	
			V_{CC} < 4.5V	31.25	-	ns	

Note: When the external load capacitance C_L = 30pF.





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

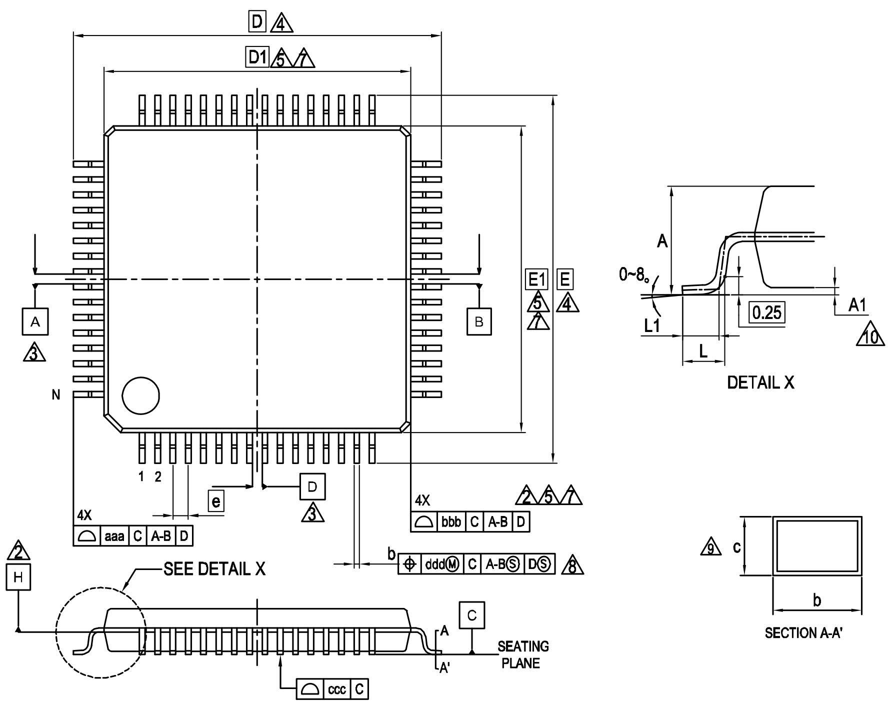
Ts	: Sampling time	
R_{AIN}	: input resistor of A/D = 2kΩ	$4.5 \leq AV_{CC} \leq 5.5$
	input resistor of A/D = 3.8kΩ	$2.7 \leq AV_{CC} < 4.5$
C_{AIN}	:input capacity of A/D = 12.9pF	$2.7 \leq AV_{CC} \leq 5.5$
Rext	: Output impedance of external circuit	

(Equation 2) $Tc = Tcck \times 14$

Tc	: Compare time
Tcck	: Compare clock cycle

Package Type	Package Code
LQFP 64	LQG064

LQG064 , 64 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQG064		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.65 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.13
N	48		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A