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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9af114laqn-g-ave2

Contents

1. Product Lineup

Memory Size

Product name	MB9AF111LA/MA/NA	MB9AF112LA/MA/NA MB9AF112L	MB9AF114LA/MA/NA MB9AF114L
On-chip Flash memory	64Kbytes	128Kbytes	256Kbytes
On-chip SRAM	16Kbytes	16Kbytes	32Kbytes

Product name	MB9AF115MA/NA	MB9AF116MA/NA
On-chip Flash memory	384Kbytes	512Kbytes
On-chip SRAM	32Kbytes	32Kbytes

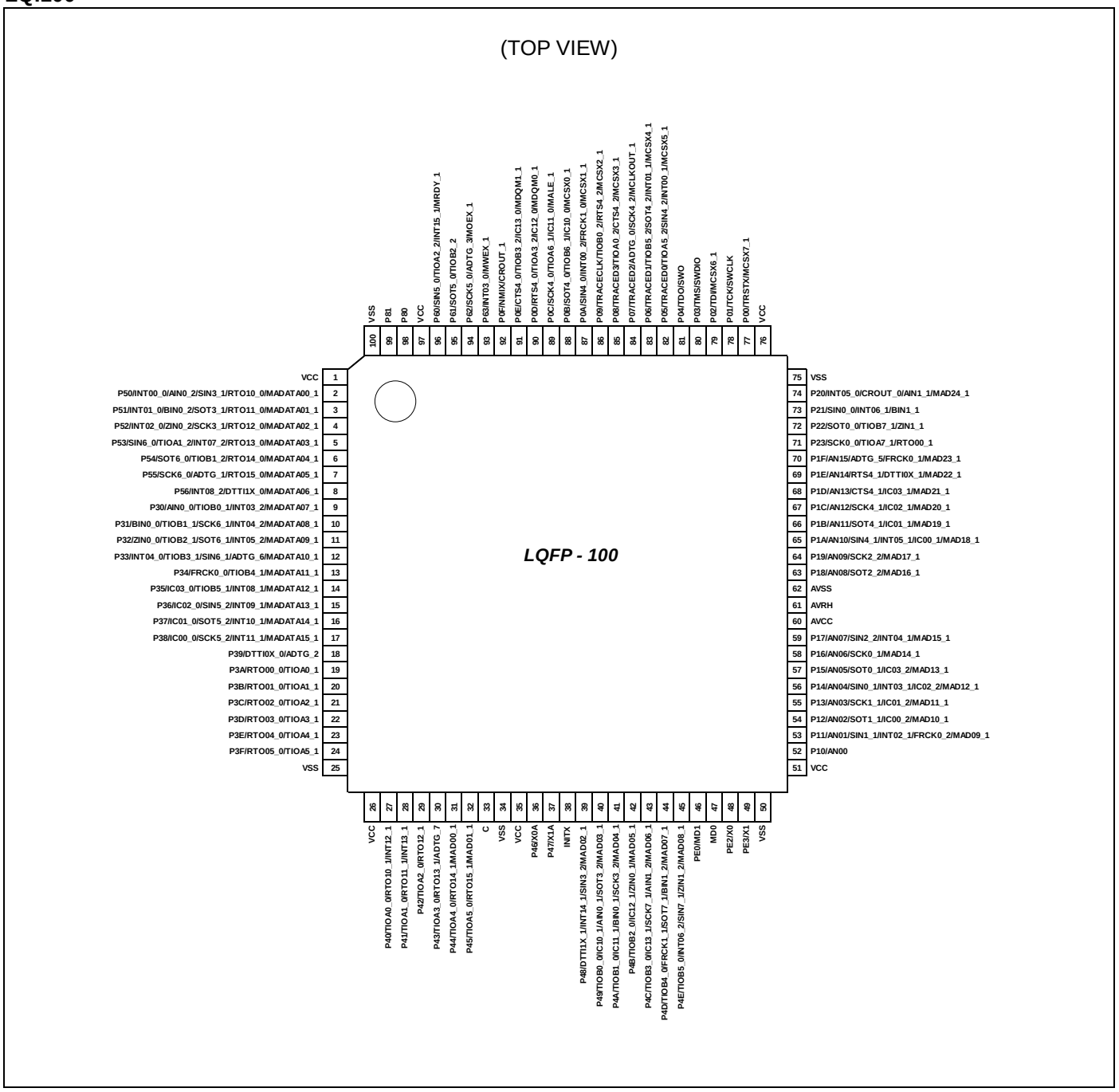
Function

Product name			MB9AF111LA MB9AF112LA MB9AF114LA MB9AF112L MB9AF114L	MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA	MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA
Pin count			64	80	100
CPU			Cortex-M3		
	Freq.		40MHz		
Power supply voltage range			2.7V to 5.5V		
DMAC			8ch.		
External Bus Interface			-	Addr:21-bit (Max) Data:8-bit CS:4 (Max) Support: SRAM, NOR Flash	Addr:25-bit (Max) Data:8/16-bit CS:8 (Max) Support: SRAM, NOR Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max) ch.4 to ch.7: FIFO (16steps x 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF-Timer	A/D activation compare	3ch.	1 unit	2 units (Max)	
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
QPRC			2ch. (Max)		
Dual Timer			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			8 pins (Max) + NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O ports			51 pins (Max)	66 pins (Max)	83 pins (Max)
12-bit A/D converter			9ch. (2 units)	12ch. (3 units)	16ch. (3 units)
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP		SWJ-DP/ETM

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
See “12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics” for accuracy of built-in CR.

3. Pin Assignment

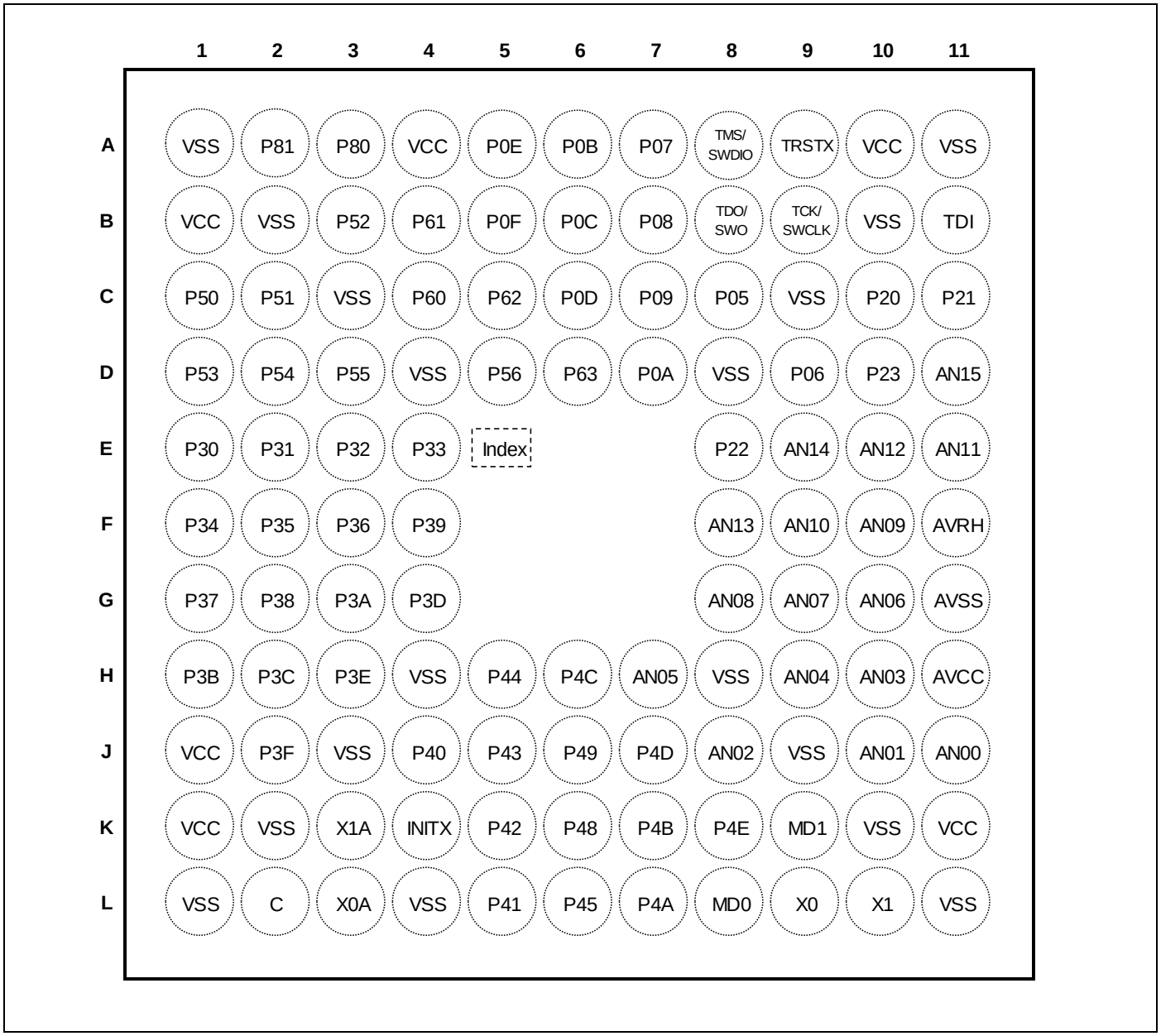
LQI100



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

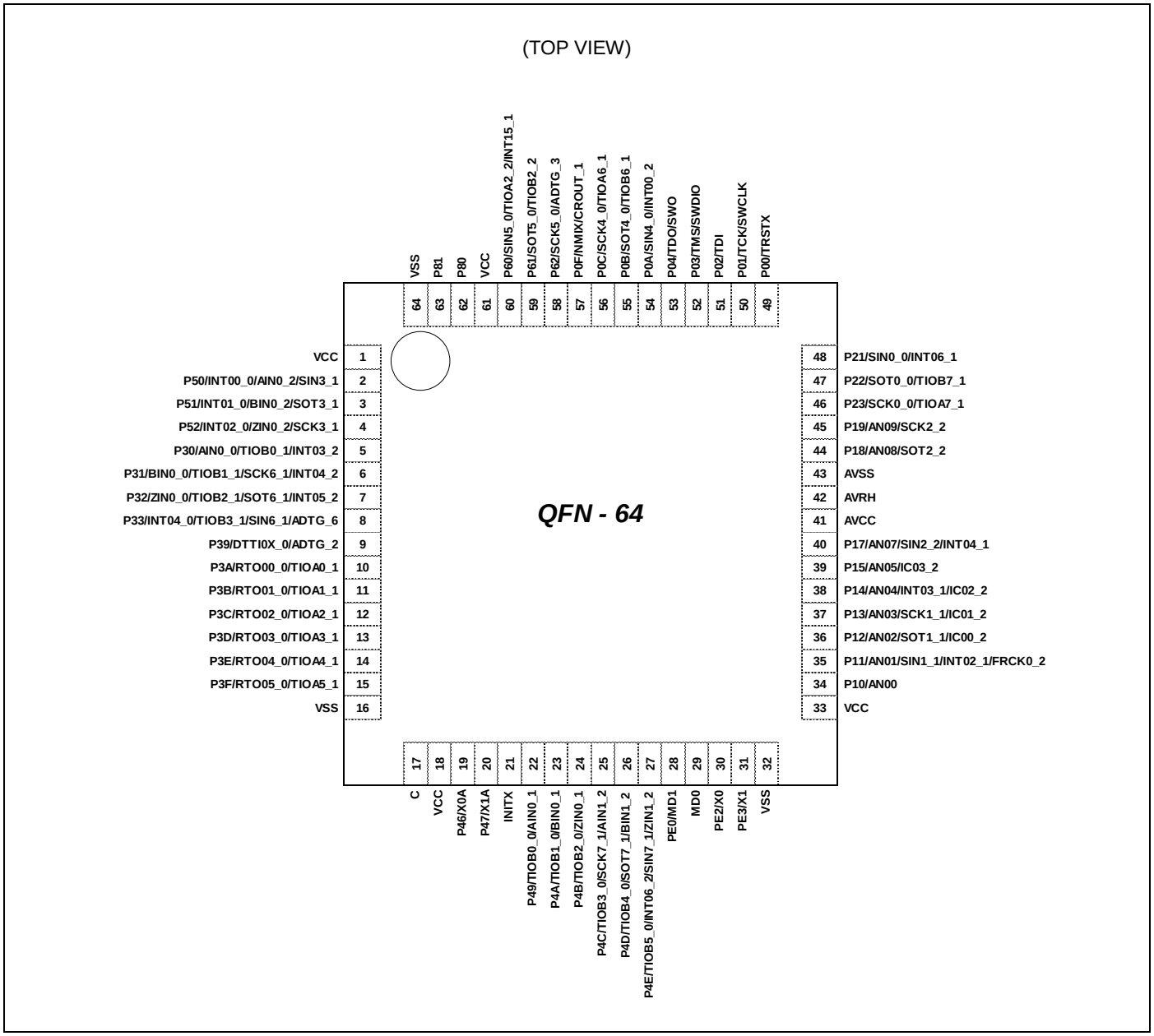
LBC112



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

VNC064

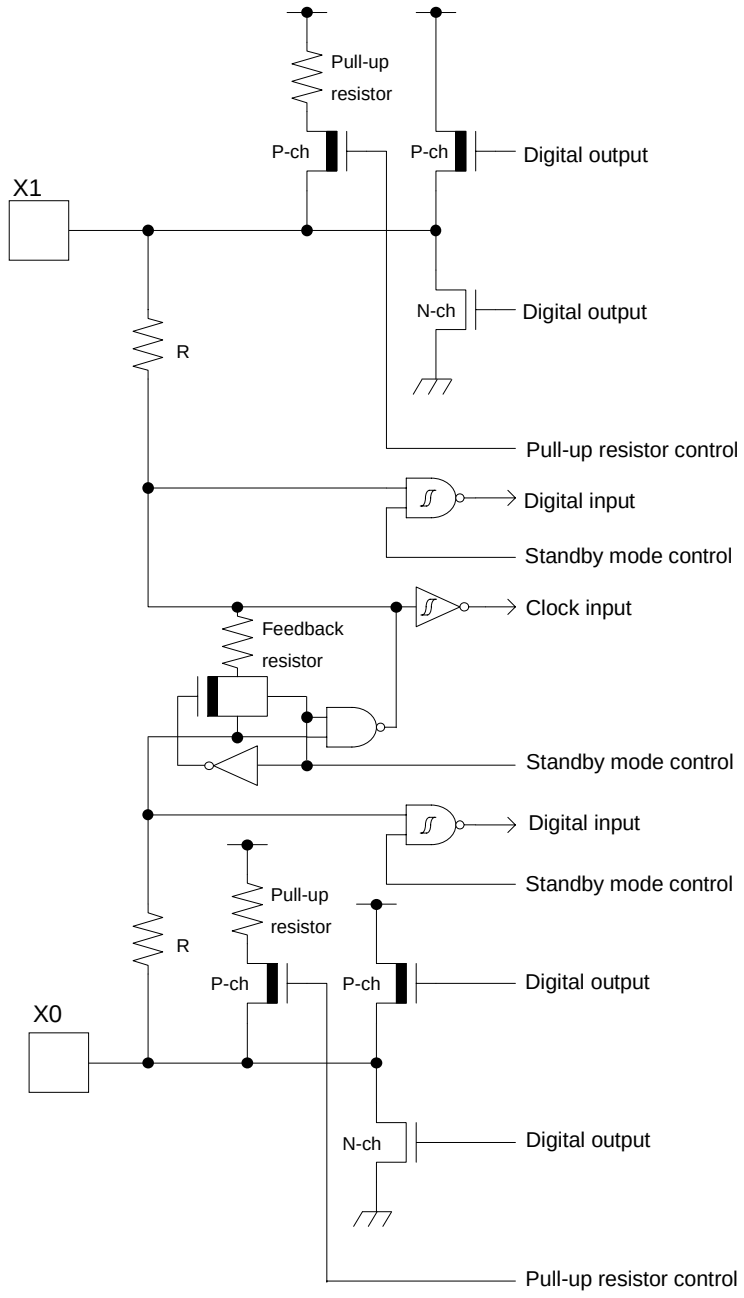
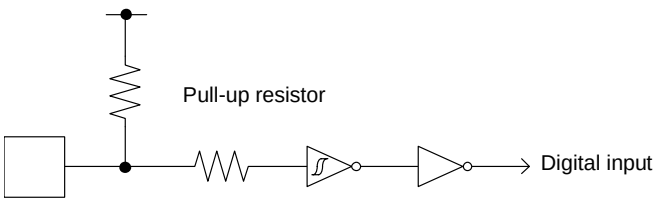


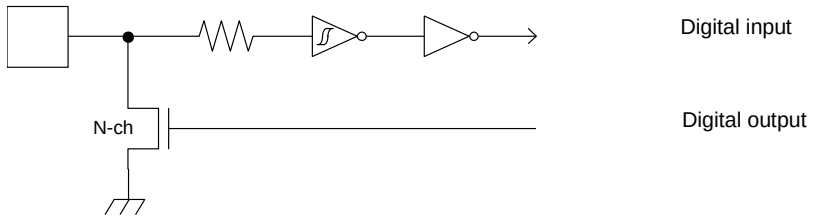
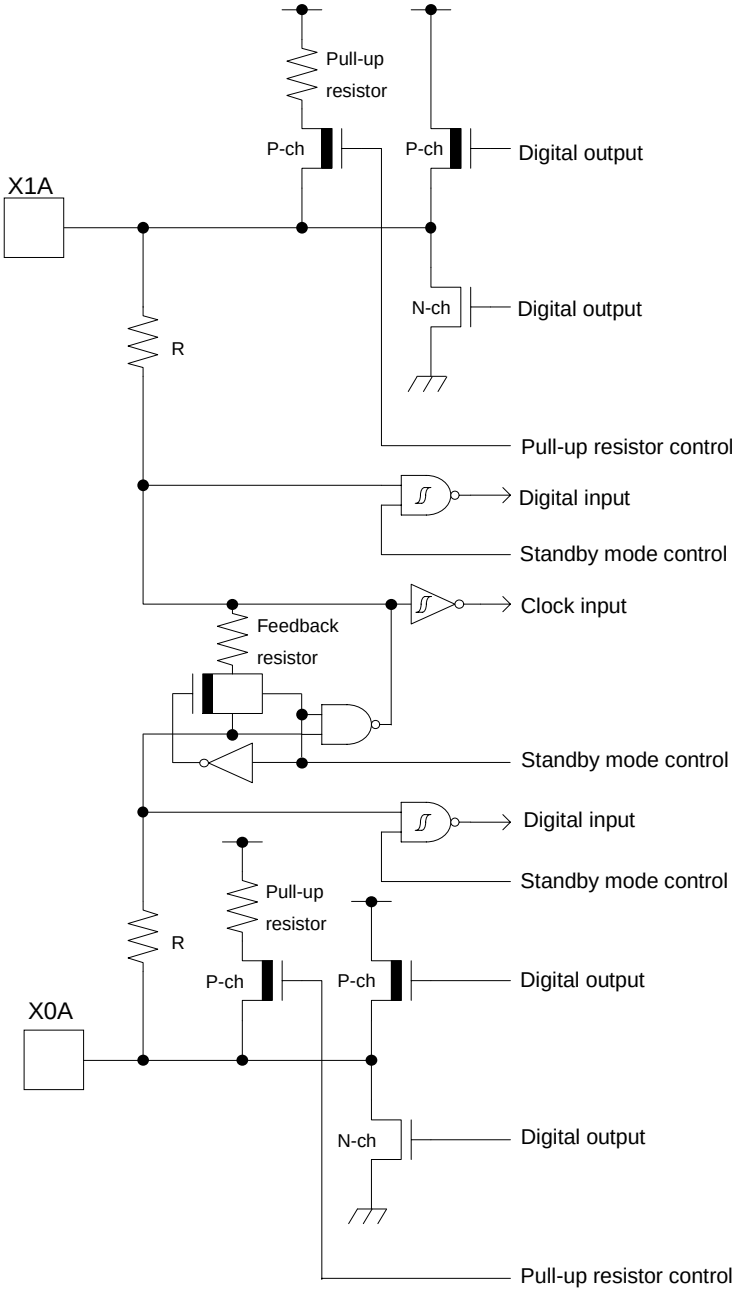
Note:

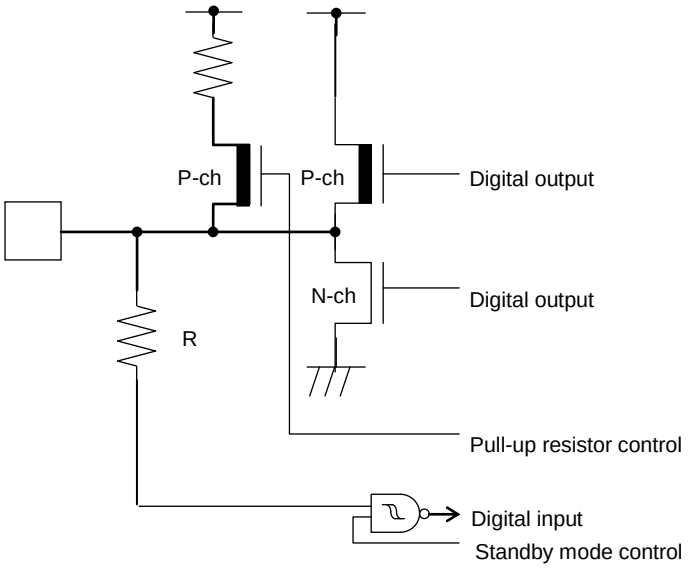
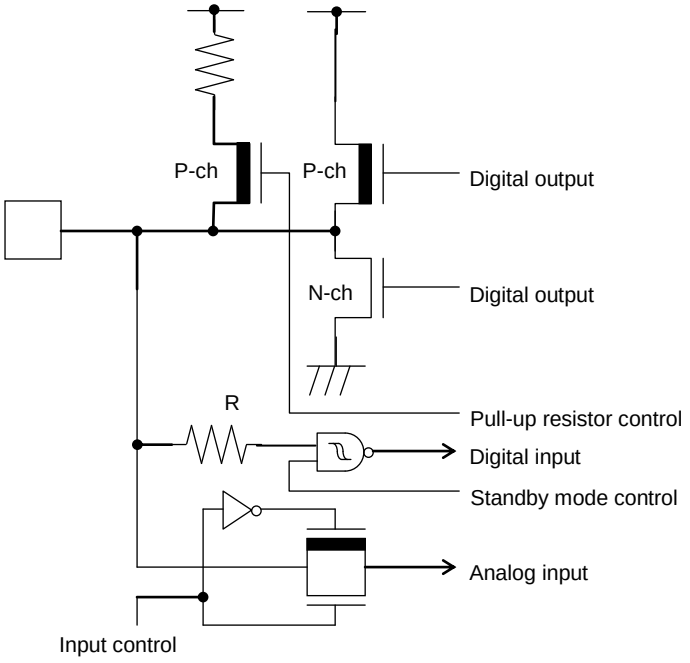
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50kΩ

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}=-4mA, I_{OL}=4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}=-4mA, I_{OL}=4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

12.4 AC Characteristics

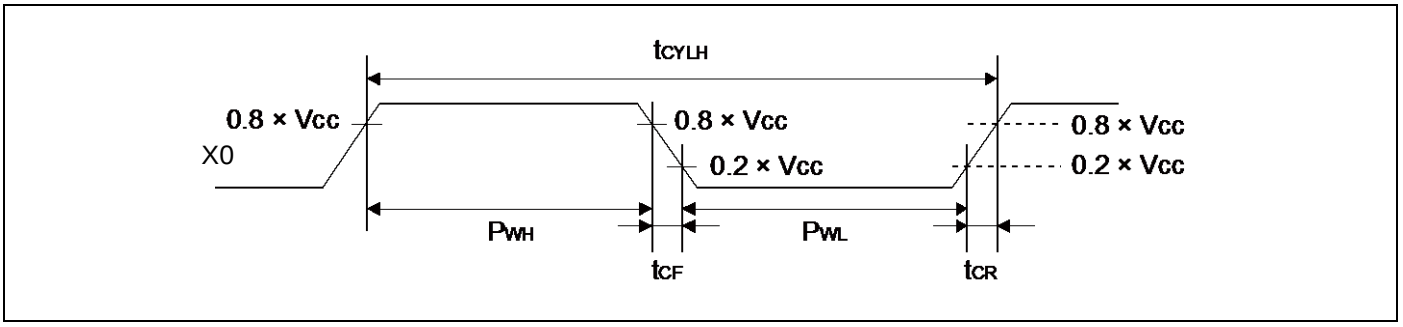
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0 X1	V_{CC}≥ 4.5V	4	48	MHz	When crystal oscillator is connected
			V_{CC}<4.5V	4	20		
			V_{CC}≥ 4.5V	4	48	MHz	When using external clock
			V_{CC}<4.5V	4	20		
Input clock cycle	t_{CYLH}		V_{CC}≥ 4.5V	20.83	250	ns	When using external clock
			V_{CC}<4.5V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF} t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	40	MHz	Master clock
	F_{CC}	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this datasheet.



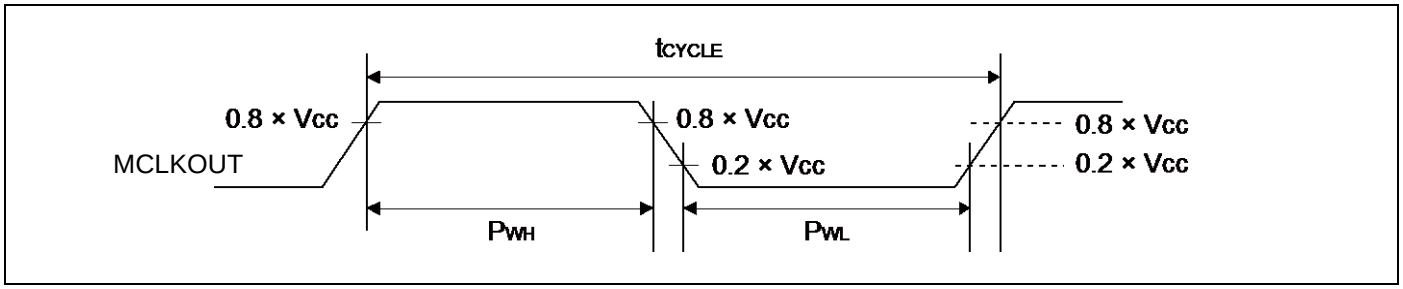
12.4.8 External Bus Timing

External bus clock output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT	$V_{CC} \geq 4.5$ V	-	40	MHz
			$V_{CC} < 4.5$ V	-	32	MHz
Minimum clock cycle time	-		$V_{CC} \geq 4.5$ V	25	-	ns
			$V_{CC} < 4.5$ V	31.25	-	ns

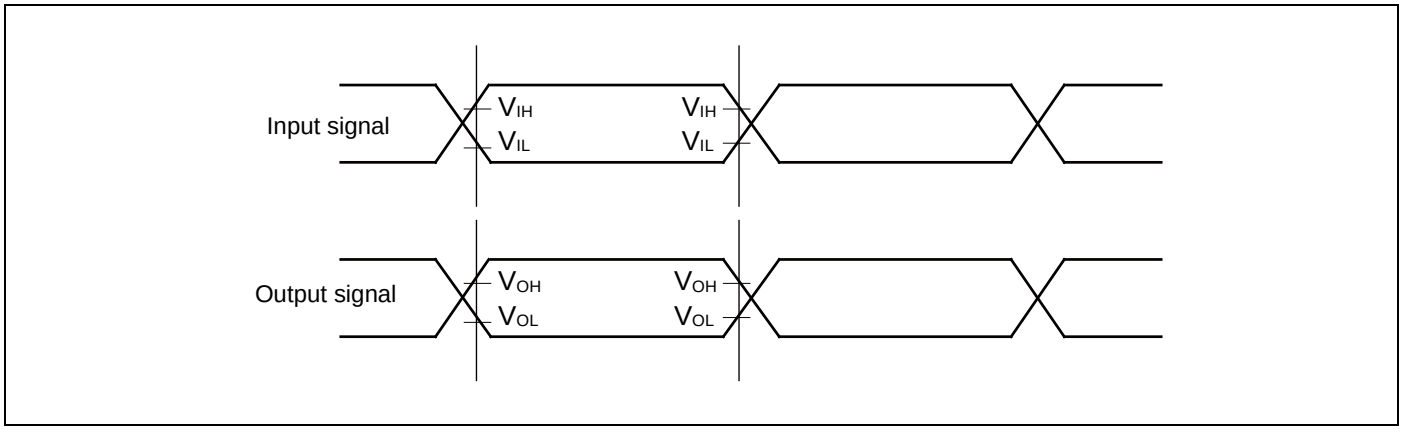
Note: The external bus clock output is a divided clock of HCLK. For more information about setting of clock divider, see "Chapter 12: External Bus Interface" in "FM3 Family Peripheral Manual"
When external bus clock is not output, this characteristic does not give any effect on external bus operation.

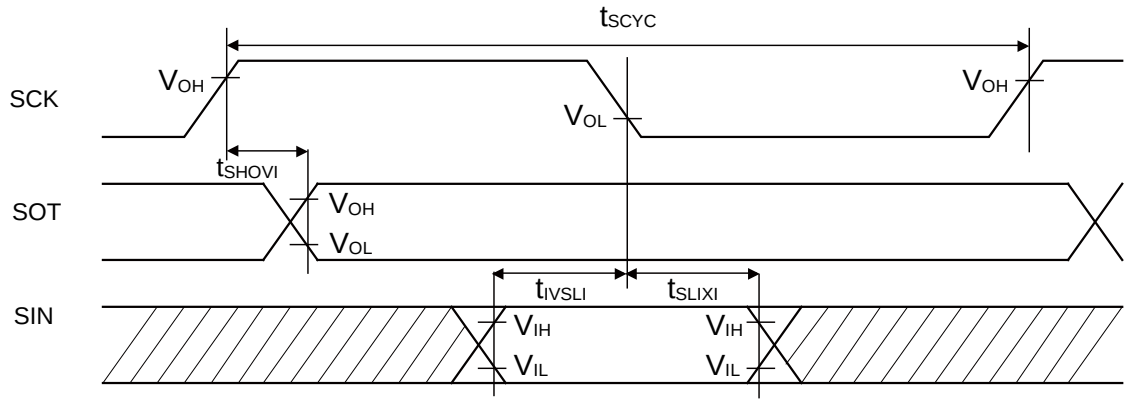


External bus signal input/output characteristics

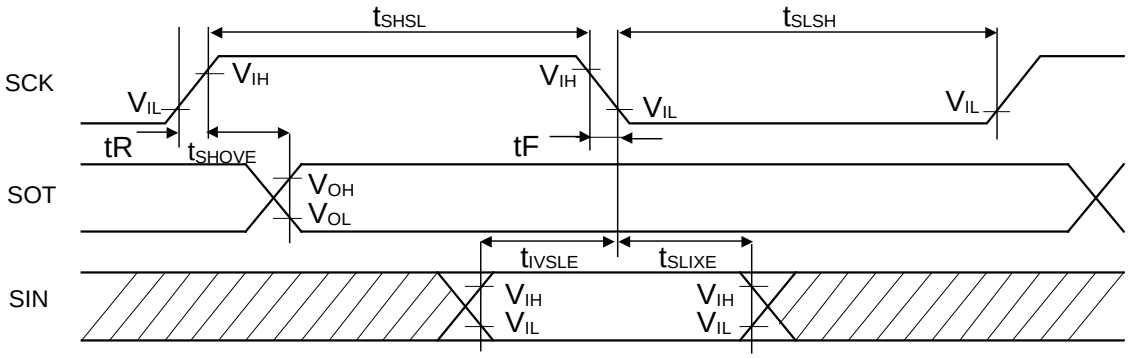
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	

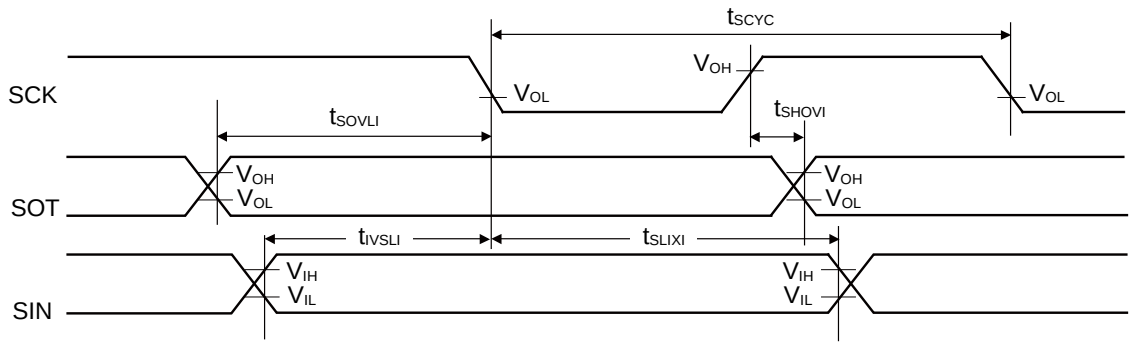




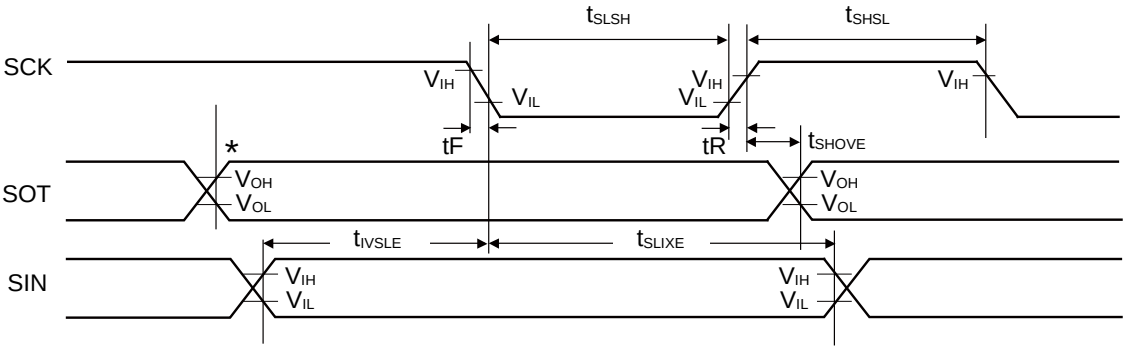
Master mode



Slave mode



Master mode



Slave mode

*: Changes when writing to TDR register

CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS}= 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC}<4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓⟶ SOT delay time	t_{SLOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑⟶SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT ⟶ SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ ⟶ SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN ⟶ SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑⟶ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

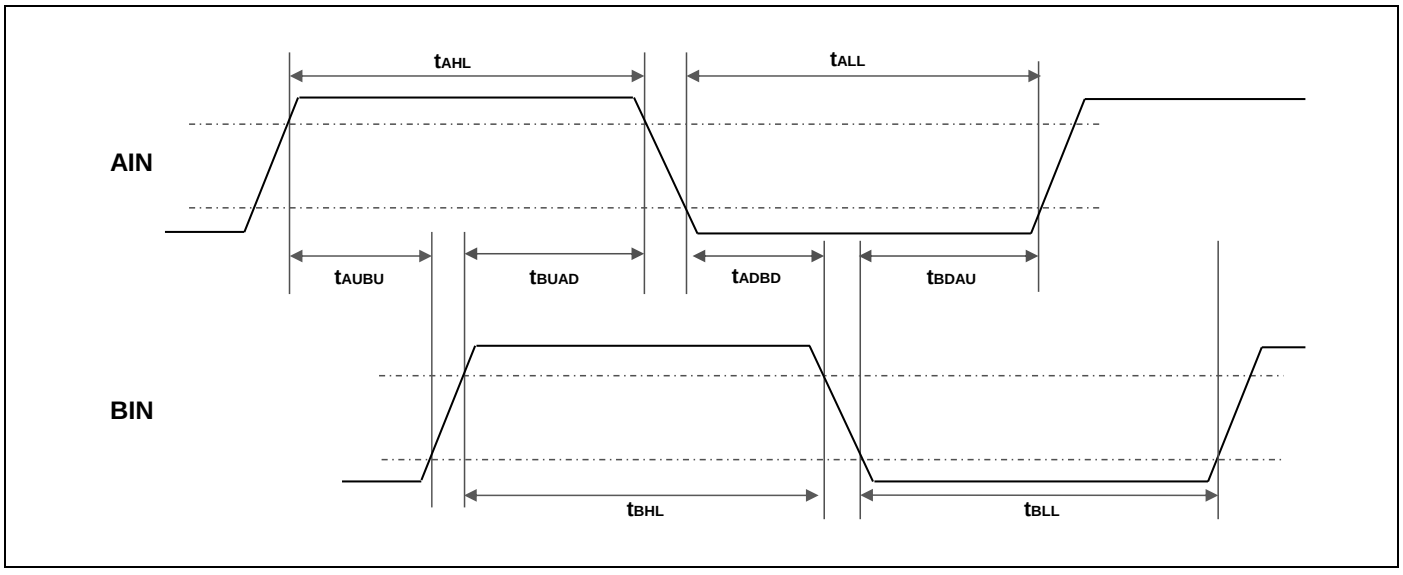
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L= 30pF.

12.4.12 Quadrature Position/Revolution Counter timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

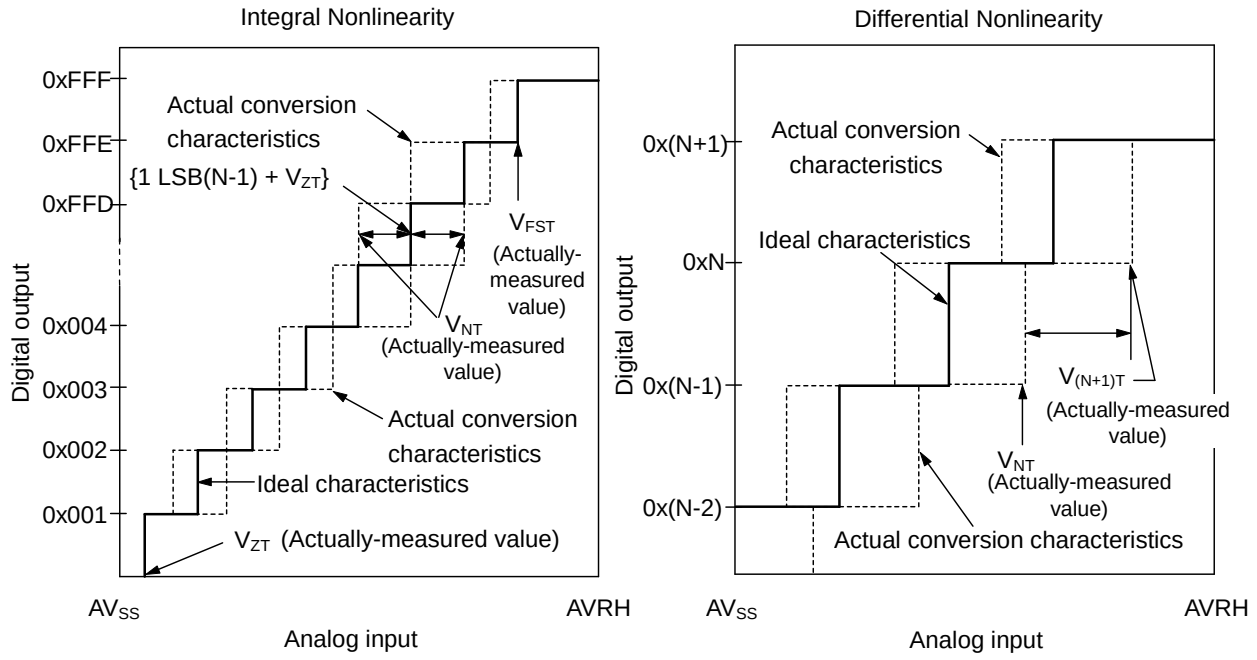
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$ *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC = "1"			

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.



Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

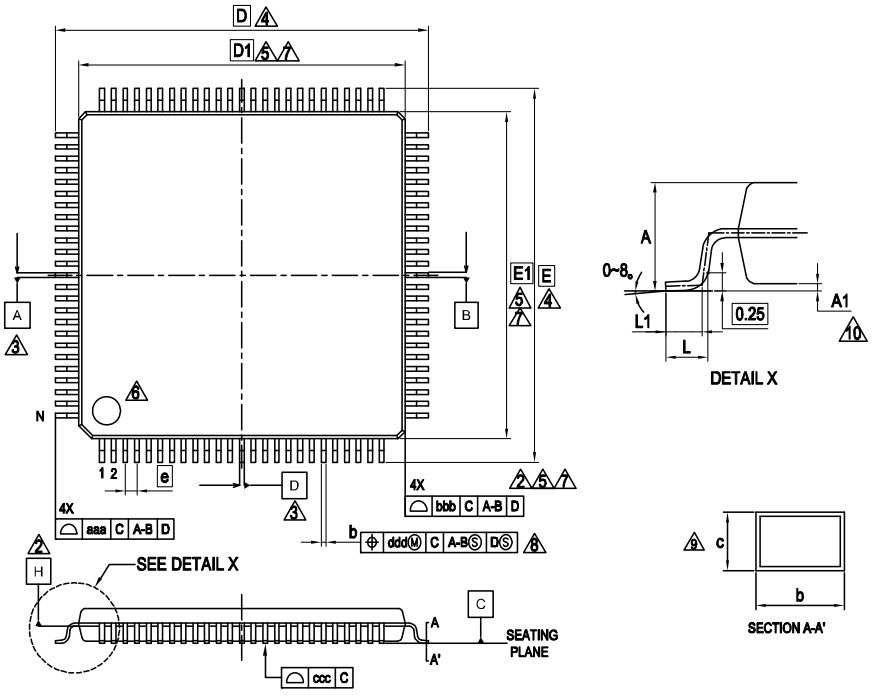
$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100

LQI100-02 , 100 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQI100-02		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	100		

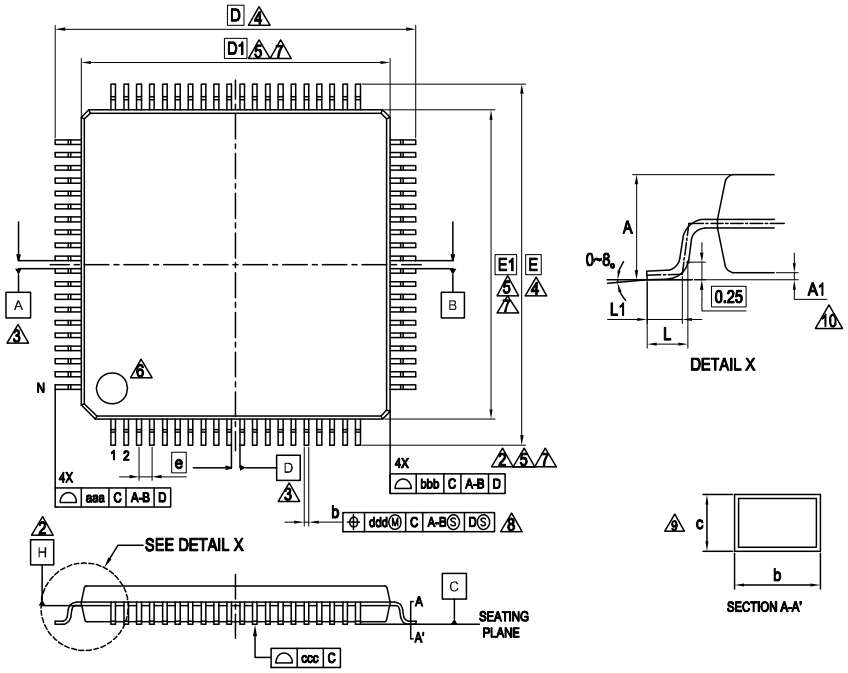
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
LQFP 80	LQH080

LQH080-02 , 80 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQH080-02		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	80		

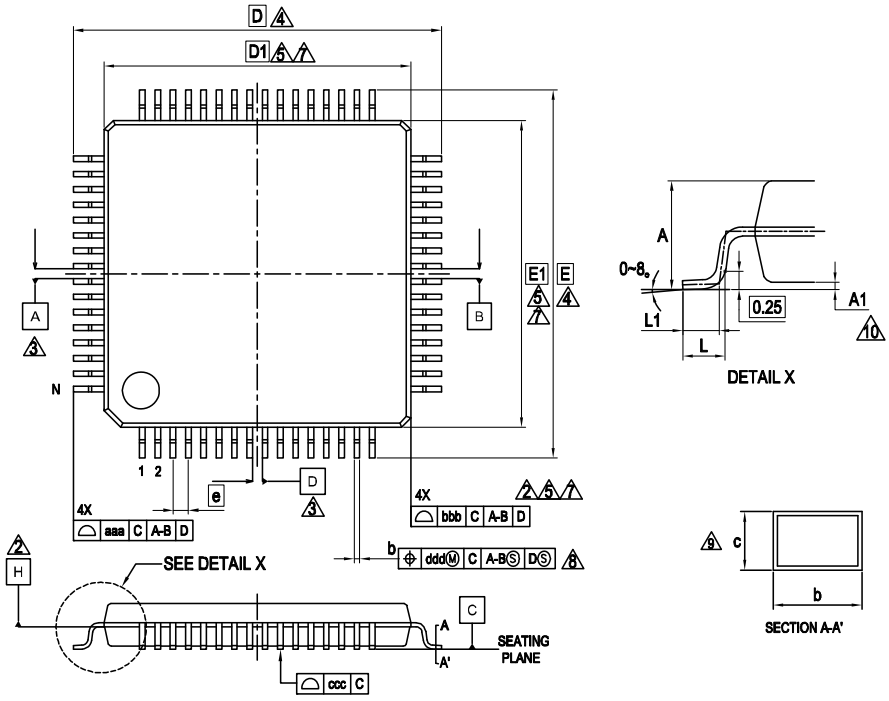
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
LQFP 64	LQG064

LQG064 , 64 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQG064		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.65 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.13
N	48		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
9	PACKAGES	Deleted FPT-64P-M24, FPT-64P-M23, FPT-80P-M21, FPT-100P-M20
44, 46	I/O CIRCUIT TYPE	Added the description of I^2C to the type of E, F and I
44, 45	I/O CIRCUIT TYPE	Added about +B input
51	HANDLING DEVICES	Added "Stabilizing power supply voltage"
51	HANDLING DEVICES Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
52	HANDLING DEVICES C Pin	Changed the description
53	BLOCK DIAGRAM	Modified the block diagram
54	MEMORY SIZE	Changed to the following description See "Memory size" in "PRODUCT LINEUP" to confirm the memory size.
55	MEMORY MAP Memory map(1)	Modified the area of "External Device Area"
56, 57	MEMORY MAP Memory map(2)(3)	Added the summary of Flash memory sector and the note
64, 65	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Added the Clamp maximum current Added the output current of P80 and P81 Added about +B input
66	ELECTRICAL CHARACTERISTICS 2. Recommended Operation Conditions	Modified the minimum value of Analog reference voltage Added Smoothing capacitor Added the note about less than the minimum power supply voltage
67, 68	ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Added Flash Memory Current Moved A/D Converter Current
71	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR
72	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1)(4-2) Operating Conditions of Main PLL	Added Main PLL clock frequency Added the figure of Main PLL connection
73	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (6) Power-on Reset Timing	Added Time until releasing Power-on reset Changed the figure of timing
75-77	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) External Bus Timing	Modified Data output time
82-89	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (8) CSIO/UART Timing	Modified from UART Timing to CSIO/UART Timing Changed from Internal shift clock operation to Master mode Changed from External shift clock operation to Slave mode
96	ELECTRICAL CHARACTERISTICS 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage Modified Stage transition time to operation permission Modified the minimum value of Reference voltage
101	ELECTRICAL CHARACTERISTICS 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
105	ORDERING INFORMATION	Change to full part number
106	PACKAGE DIMENSIONS	Deleted FPT-64P-M24, FPT-64P-M23, FPT-80P-M21, FPT-100P-M20

Note: Please see “Document History” about later revised information.