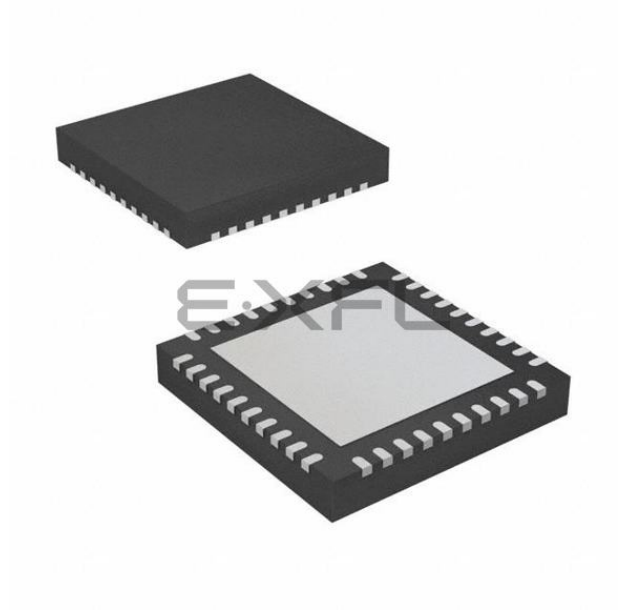

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Product Status	Active
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Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1934-e-mv

TABLE 1: 28-PIN SUMMARY (PIC16(L)F1936)

I/O	28-Pin SPDIP	28-Pin QFN/UQFN	ANSEL	A/D	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	LCD	Interrupt	Pull-up	Basic
RA0	2	27	Y	AN0	—	C12IN0-/ C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG12	—	—	VCAP(2)
RA1	3	28	Y	AN1	—	C12IN1-	—	—	—	—	—	SEG7	—	—	—
RA2	4	1	Y	AN2/ VREF-	—	C2IN+/ DACOUT	—	—	—	—	—	COM2	—	—	—
RA3	5	2	Y	AN3/ VREF+	—	C1IN+	—	—	—	—	—	SEG15/ COM3	—	—	—
RA4	6	3	Y	—	CPS6	C1OUT	SRQ	T0CKI	CCP5	—	—	SEG4	—	—	—
RA5	7	4	Y	AN4	CPS7	C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG5	—	—	VCAP(2)
RA6	10	7	—	—	—	—	—	—	—	—	—	SEG1	—	—	OSC2/ CLKOUT VCAP(2)
RA7	9	6	—	—	—	—	—	—	—	—	—	SEG2	—	—	OSC1/ CLKIN
RB0	21	18	Y	AN12	CPS0	—	SRI	—	CCP4	—	—	SEG0	INT/ IOC	Y	—
RB1	22	19	Y	AN10	CPS1	C12IN3-	—	—	P1C	—	—	VLCD1	IOC	Y	—
RB2	23	20	Y	AN8	CPS2	—	—	—	P1B	—	—	VLCD2	IOC	Y	—
RB3	24	21	Y	AN9	CPS3	C12IN2-	—	—	CCP2(1)/ P2A(1)	—	—	VLCD3	IOC	Y	—
RB4	25	22	Y	AN11	CPS4	—	—	—	P1D	—	—	COM0	IOC	Y	—
RB5	26	23	Y	AN13	CPS5	—	—	T1G(1)	P2B(1) CCP3(1)/ P3A(1)	—	—	COM1	IOC	Y	—
RB6	27	24	—	—	—	—	—	—	—	—	—	SEG14	IOC	Y	ICSPCLK/ ICDCLK
RB7	28	25	—	—	—	—	—	—	—	—	—	SEG13	IOC	Y	ICSPDAT/ ICDDAT
RC0	11	8	—	—	—	—	—	T1OSO/ T1CKI	P2B(1)	—	—	—	—	—	—
RC1	12	9	—	—	—	—	—	T1OSI	CCP2(1)/ P2A(1)	—	—	—	—	—	—
RC2	13	10	—	—	—	—	—	—	CCP1/ P1A	—	—	SEG3	—	—	—
RC3	14	11	—	—	—	—	—	—	—	—	SCK/SCL	SEG6	—	—	—
RC4	15	12	—	—	—	—	—	T1G(1)	—	—	SDI/SDA	SEG11	—	—	—
RC5	16	13	—	—	—	—	—	—	—	—	SDO	SEG10	—	—	—
RC6	17	14	—	—	—	—	—	—	CCP3(1) P3A(1)	TX/CK	—	SEG9	—	—	—
RC7	18	15	—	—	—	—	—	—	P3B	RX/DT	—	SEG8	—	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	8, 19	5, 16	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be moved using the APFCON register.
2: PIC16F1936 devices only.

TABLE 3-11: PIC16(L)F1934/6/7 MEMORY MAP, BANK 31

Bank 31	
F8Ch	Unimplemented Read as '0'
FE3h	
FE4h	STATUS_SHAD
FE5h	WREG_SHAD
FE6h	BSR_SHAD
FE7h	PCLATH_SHAD
FE8h	FSR0L_SHAD
FE9h	FSR0H_SHAD
FEAh	FSR1L_SHAD
FEBh	FSR1H_SHAD
FECh	—
FEDh	STKPTR
FEEh	TOSL
FEFh	TOSH

Legend: = Unimplemented data memory locations, read as '0'.

3.2.6 SPECIAL FUNCTION REGISTERS SUMMARY

The Special Function Register Summary for the device family are as follows:

Device	Bank(s)	Page No.
PIC16(L)F1934/6/7	0	39
	1	40
	2	41
	3	42
	4	43
	5	44
	6	45
	7	46
	8	47
	9-14	48
	15	49
	16-30	51
	31	52

7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

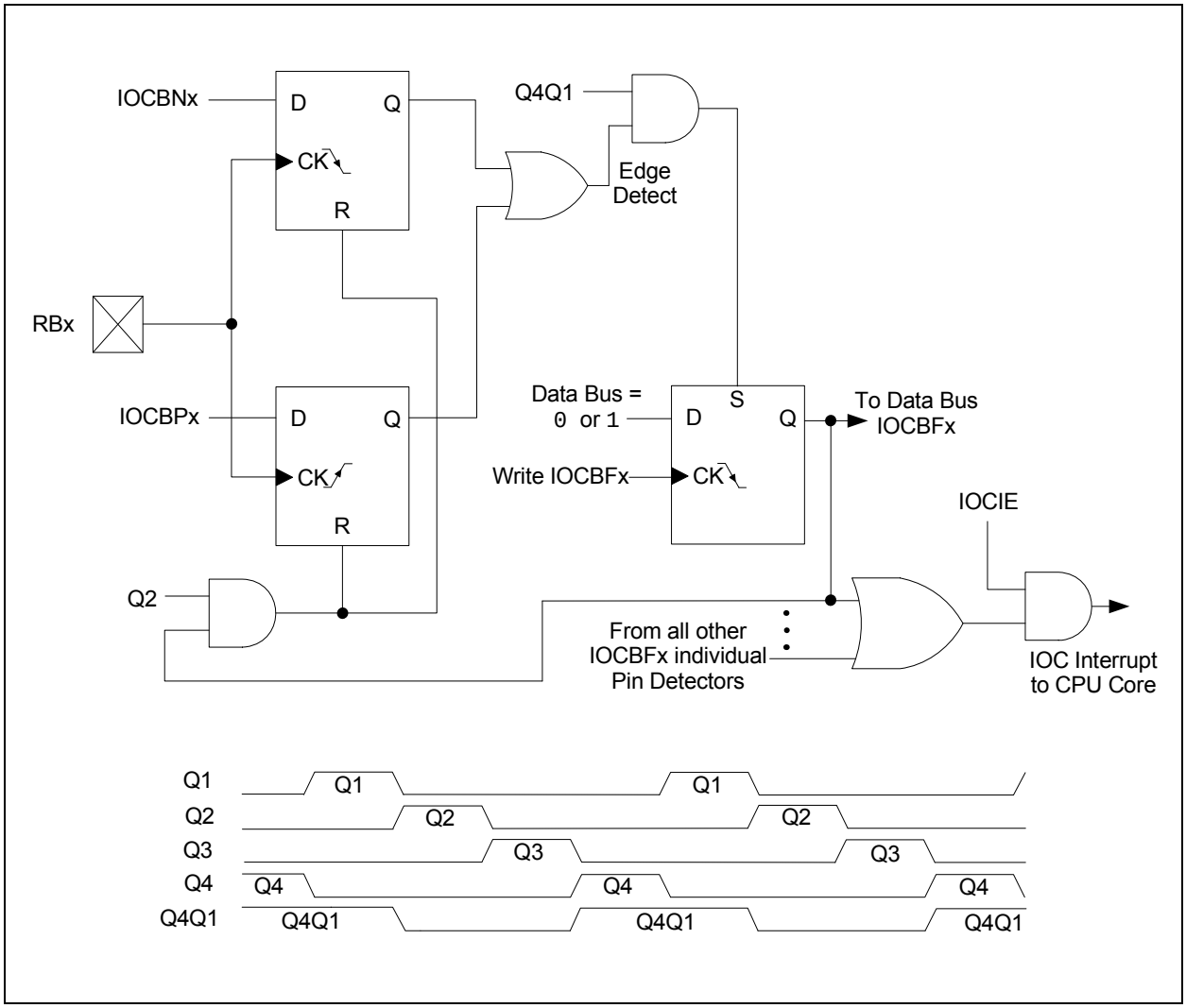
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce Interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: INTERRUPT LOGIC



7.6.3 PIE2 REGISTER

The PIE2 register contains the interrupt enable bits, as shown in Register 7-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 7-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	—	CCP2IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail interrupt
0 = Disables the Oscillator Fail interrupt

bit 6 **C2IE:** Comparator C2 Interrupt Enable bit
1 = Enables the Comparator C2 interrupt
0 = Disables the Comparator C2 interrupt

bit 5 **C1IE:** Comparator C1 Interrupt Enable bit
1 = Enables the Comparator C1 interrupt
0 = Disables the Comparator C1 interrupt

bit 4 **EEIE:** EEPROM Write Completion Interrupt Enable bit
1 = Enables the EEPROM Write Completion interrupt
0 = Disables the EEPROM Write Completion interrupt

bit 3 **BCLIE:** MSSP Bus Collision Interrupt Enable bit
1 = Enables the MSSP Bus Collision Interrupt
0 = Disables the MSSP Bus Collision Interrupt

bit 2 **LCDIE:** LCD Module Interrupt Enable bit
1 = Enables the LCD module interrupt
0 = Disables the LCD module interrupt

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

7.6.6 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 7-6.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 7-6: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	—	CCP2IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **OSFIF:** Oscillator Fail Interrupt Flag
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **C2IF:** Comparator C2 Interrupt Flag
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **C1IF:** Comparator C1 Interrupt Flag
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **EEIF:** EEPROM Write Completion Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **BCLIF:** MSSP Bus Collision Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **LCDIF:** LCD Module Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

12.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 12-1. For this device family, the following functions can be moved between different pins.

- $\overline{SS}$ (Slave Select)
- P2B output
- CCP2/P2A output
- CCP3/P3A output
- Timer1 Gate
- SR Latch SRNQ output
- Comparator C2 output

These bits have no effect on the values of any TRIS register. PORT and TRIS overrides will be routed to the correct pin. The unselected pin will be unaffected.

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	163
ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		164
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	134
APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	131
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	183
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	183
CM1CON1	C1NTP	C1INTN	C1PCH<1:0>		—	—	C1NCH<1:0>		184
CM2CON1	C2NTP	C2INTN	C2PCH<1:0>		—	—	C2NCH<1:0>		184
CPSCON0	CPSON	—	—	—	CPSRNG<1:0>		CPSOUT	T0XCS	323
CPSCON1	—	—	—	—	CPSCH<3:0>				324
DACCON0	DACEN	DACLPS	DACOE	---	DACPSS<1:0>		---	DACNSS	176
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	133
LCDCON	LCDEN	SLPEN	WERR	—	CS<1:0>		LMUX<1:0>		329
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	333
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	333
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			193
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	133
SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	189
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				287
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	133

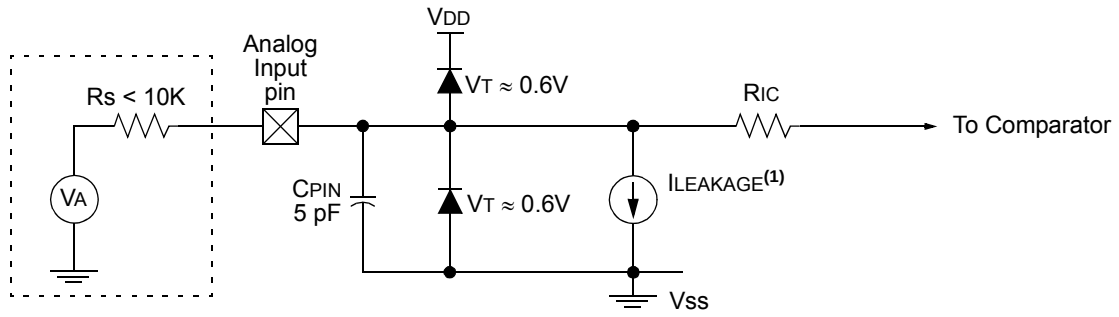
Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

TABLE 12-4: SUMMARY OF CONFIGURATION WORD WITH PORTA

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		$\overline{\text{CPD}}$	62
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			
CONFIG2	13:8	—	—	LVP	$\overline{\text{DEBUG}}$	—	BORV	STVREN	PLLEN	64
	7:0	—	—	VCAPEN<1:0>(1)		—	—	WRT<1:0>		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTA.
Note 1: PIC16F1934/6/7 only.

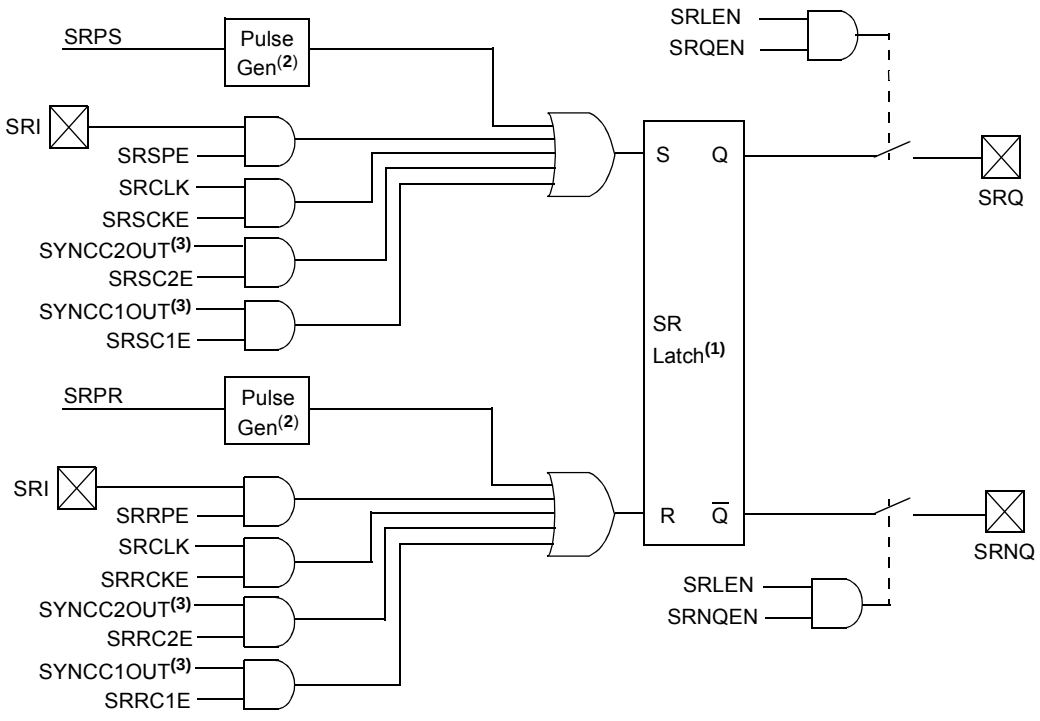
FIGURE 18-3: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

Note 1: See the applicable Electrical Specifications Chapter.

FIGURE 19-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM



Note 1: If R = 1 and S = 1 simultaneously, Q = 0, $\overline{Q}$ = 1
2: Pulse generator causes a 1 Q-state pulse width.
3: Name denotes the connection point at the comparator output.

FIGURE 21-5: TIMER1 GATE SINGLE-PULSE MODE

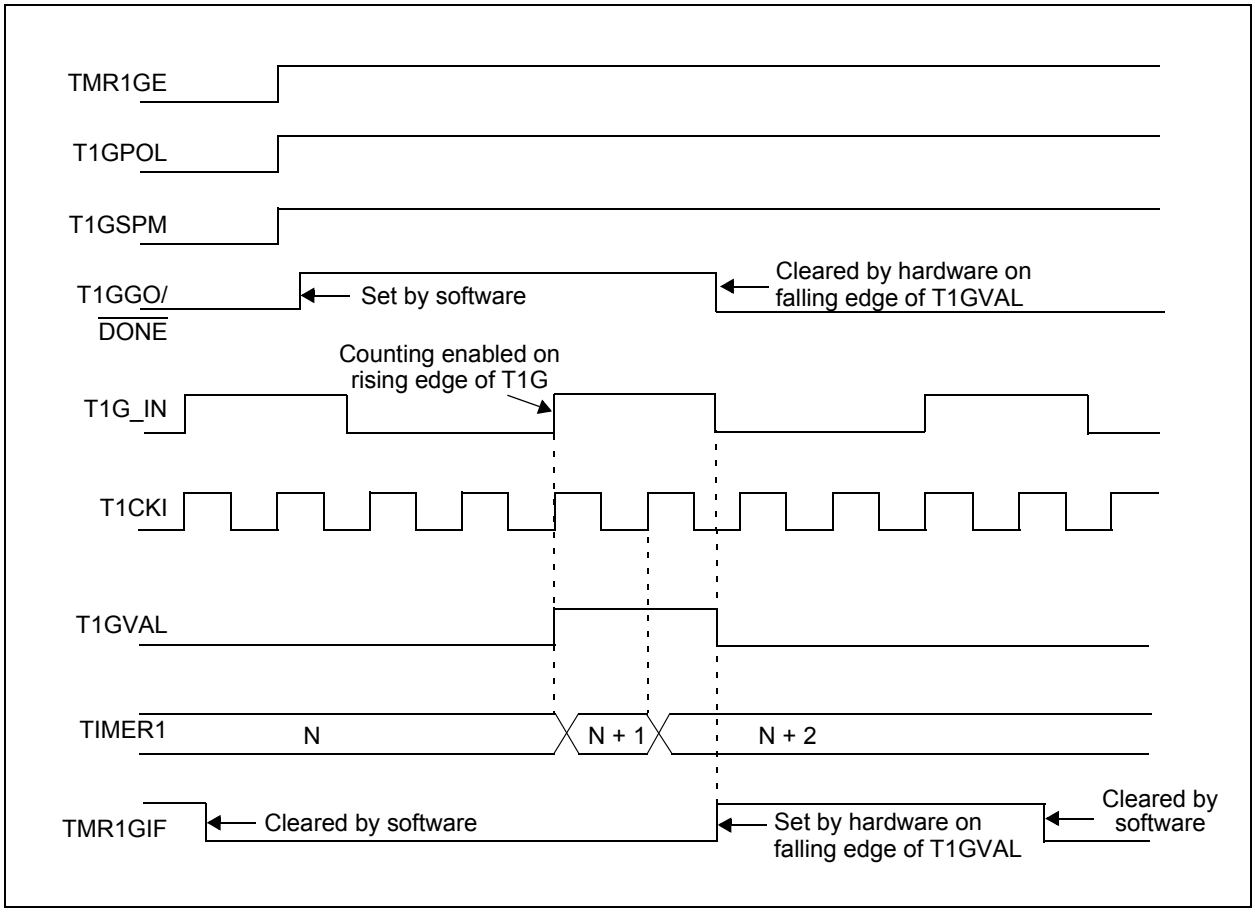
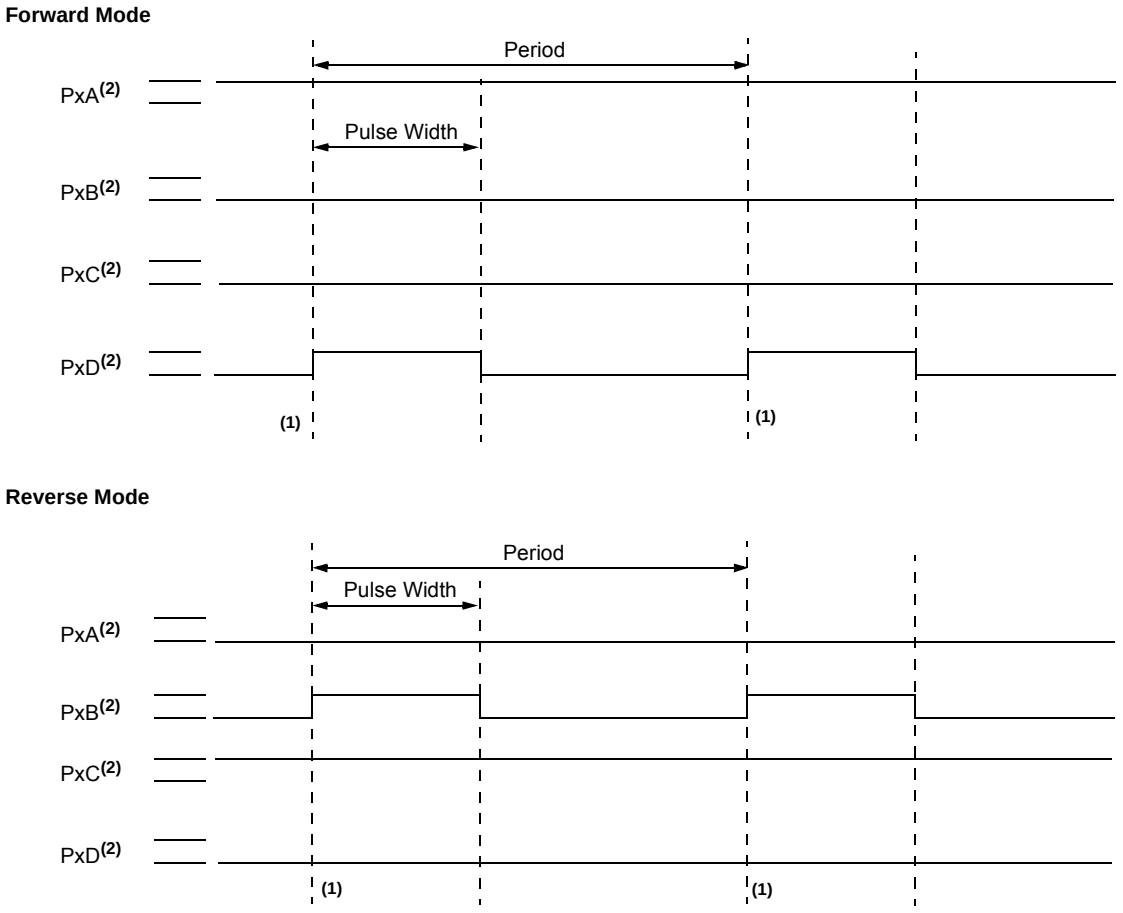


FIGURE 23-11: EXAMPLE OF FULL-BRIDGE PWM OUTPUT



Note 1: At this time, the TMRx register is equal to the PRx register.

2: Output signal is shown as active-high.

FIGURE 24-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

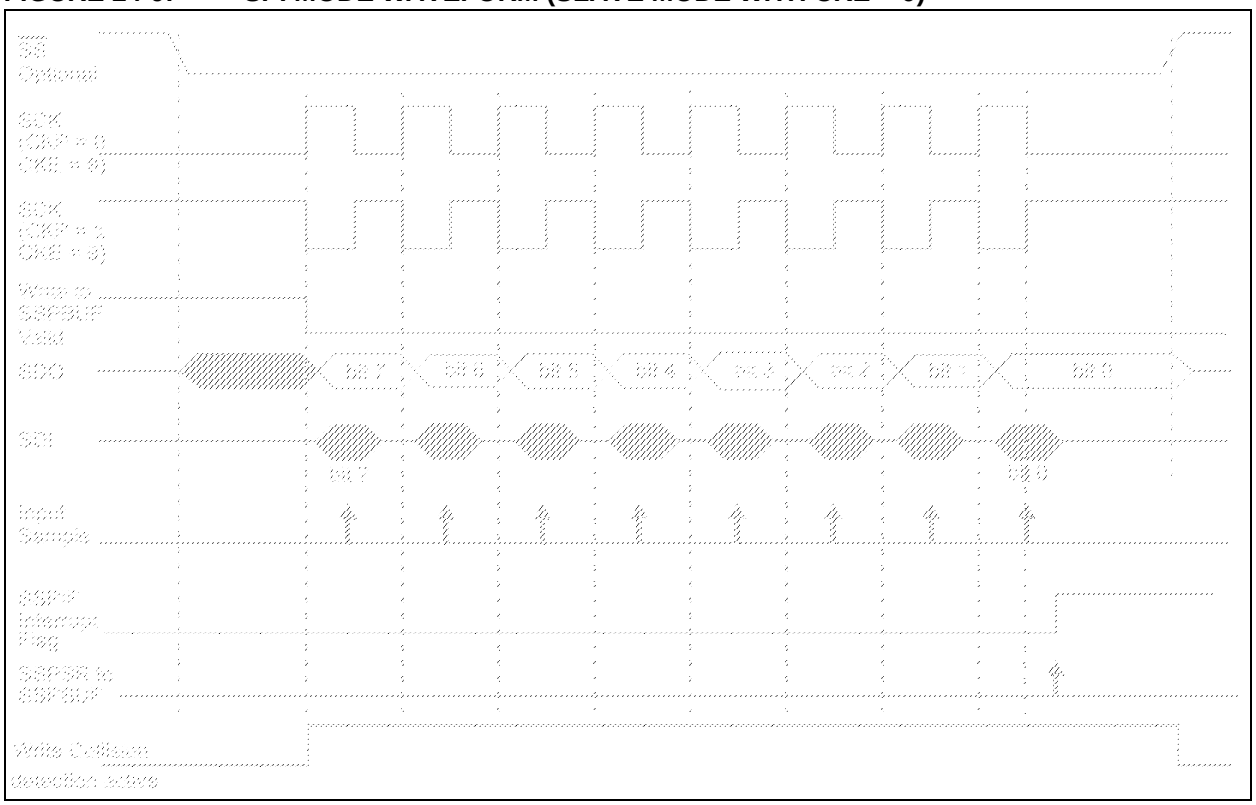
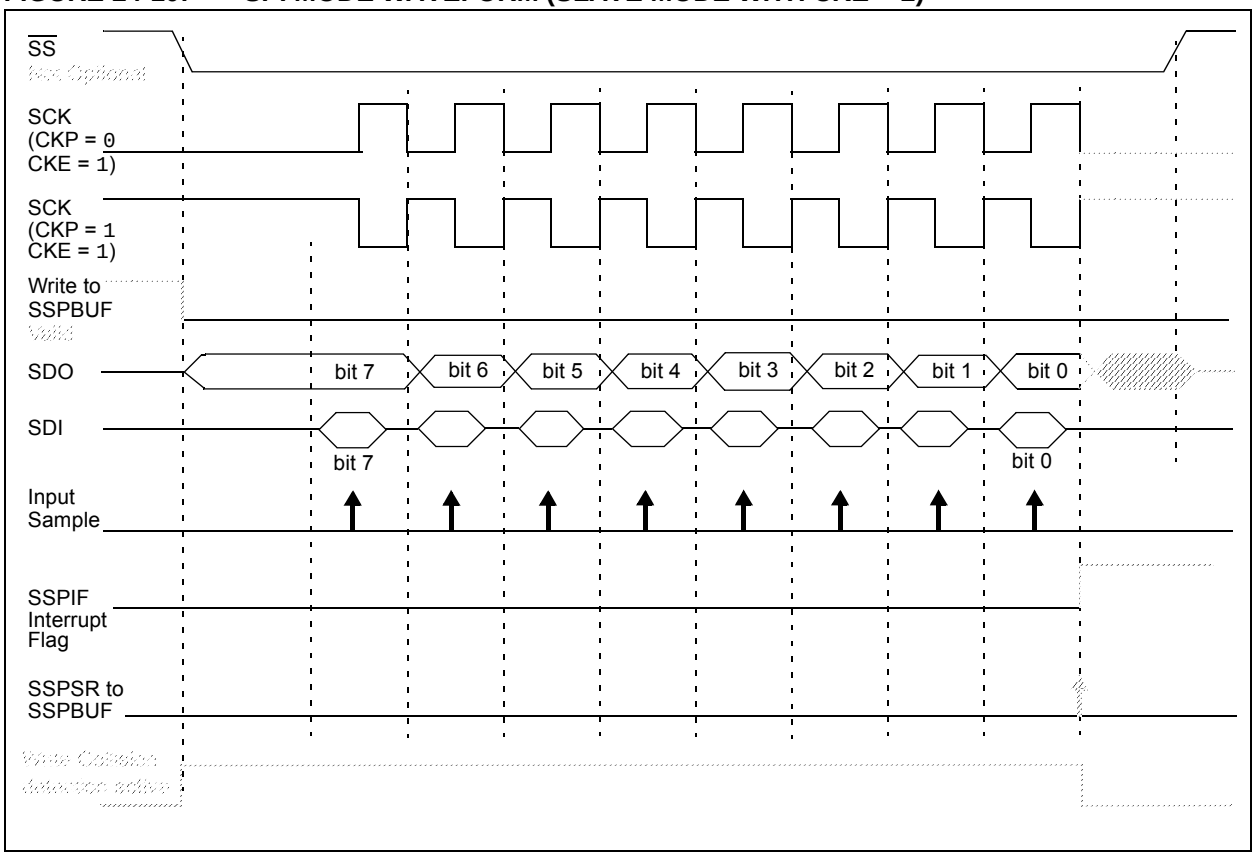


FIGURE 24-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



24.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

24.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit of SSPCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready, CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on whether the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPBUF was read before the 9th falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

24.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

24.5.6.3 Byte NACKing

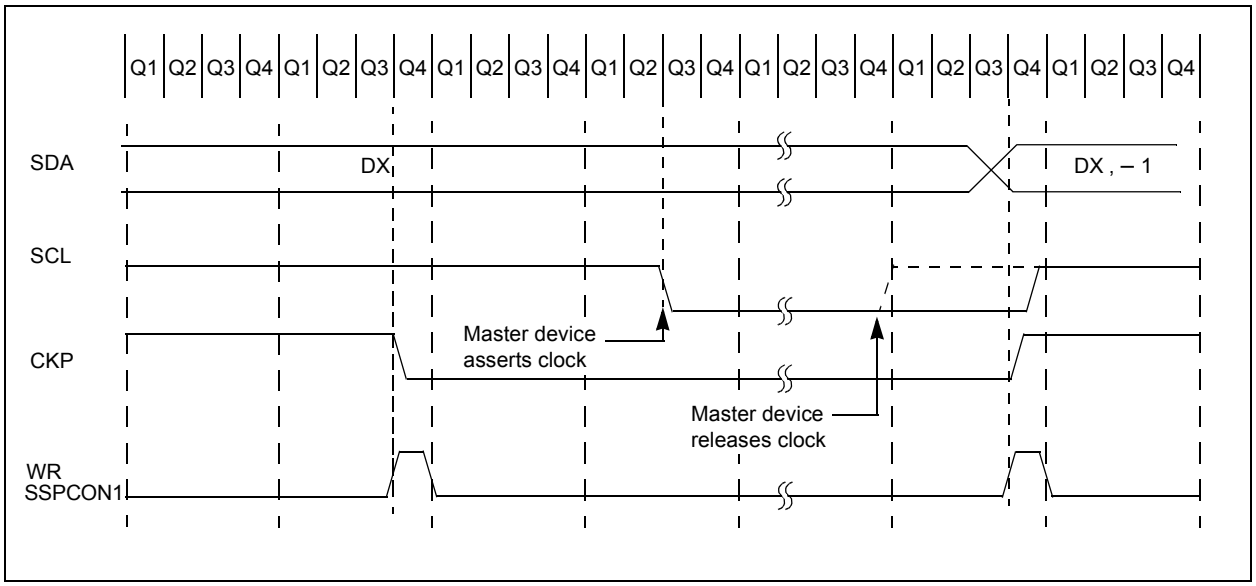
When the AHEN bit of SSPCON3 is set; CKP is cleared by hardware after the 8th falling edge of SCL for a received matching address byte. When the DHEN bit of SSPCON3 is set; CKP is cleared after the 8th falling edge of SCL for received data.

Stretching after the 8th falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

24.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 24-22).

FIGURE 24-23: CLOCK SYNCHRONIZATION TIMING



REGISTER 24-3: SSPCON2: SSP CONTROL REGISTER 2

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

bit 7 **GCEN:** General Call Enable bit (in I^2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 **ACKDT:** Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence Idle

bit 3 **RCEN:** Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive Idle

bit 2 **PEN:** Stop Condition Enable bit (in I^2C Master mode only)
SCKMSSP Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enabled bit (in I^2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enabled bit (in I^2C Master mode only)
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

25.3.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXSTA register. The Break character transmission is then initiated by a write to the TXREG. The value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXSTA register indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 25-9 for the timing of the Break character sequence.

25.3.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

25.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCSTA register and the Received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

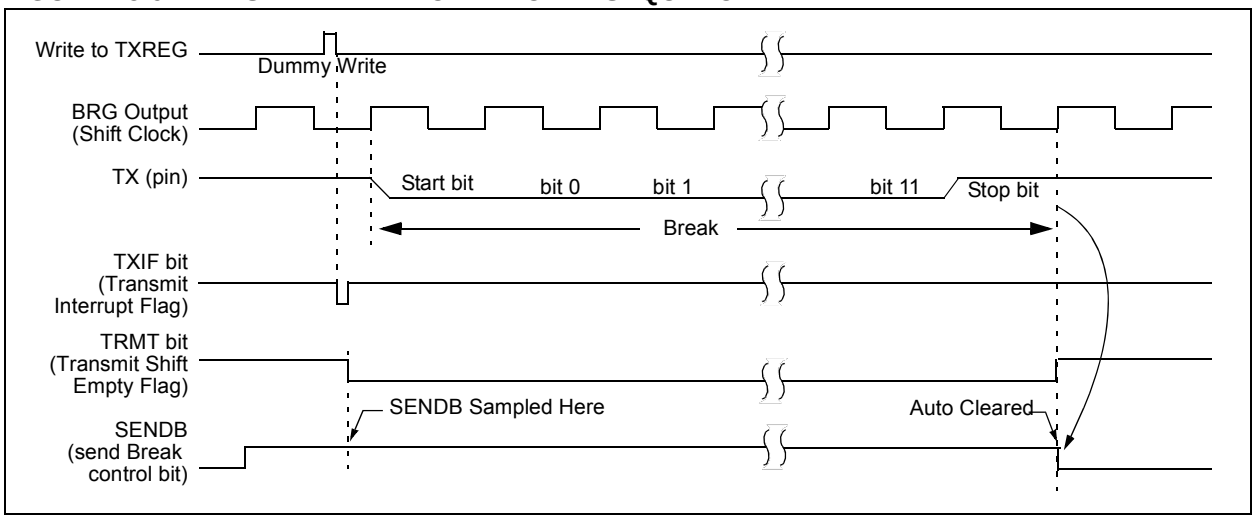
A Break character has been received when;

- RCIF bit is set
- FERR bit is set
- RCREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 25.3.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDCON register before placing the EUSART in Sleep mode.

FIGURE 25-9: SEND BREAK CHARACTER SEQUENCE



BCF **Bit Clear f**

Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BRA **Relative Branch**

Syntax:	[*label*] BRA label [*label*] BRA $+k
Operands:	-256 ≤ label - PC + 1 ≤ 255 -256 ≤ k ≤ 255
Operation:	(PC) + 1 + k → PC
Status Affected:	None
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + k. This instruction is a two-cycle instruction. This branch has a limited range.

BRW **Relative Branch with W**

Syntax:	[*label*] BRW
Operands:	None
Operation:	(PC) + (W) → PC
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + (W). This instruction is a two-cycle instruction.

BSF **Bit Set f**

Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC **Bit Test f, Skip if Clear**

Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS **Bit Test f, Skip if Set**

Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

30.2 DC Characteristics: PIC16(L)F1934/6/7-I/E (Industrial, Extended) (Continued)

PIC16LF1934/36/37			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16F1934/36/37			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Device Characteristics**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**	
						VDD	**Note**
D017	**Supply Current (IDD)(1, 2)**						
		—	110	180	µA	1.8	FOSC = 500 kHz MFINTOSC mode
		—	140	250	µA	3.0	
D017		—	150	250	µA	1.8	FOSC = 500 kHz MFINTOSC mode **(Note 5)**
		—	210	330	µA	3.0	
		—	270	430	µA	5.0	
D018		—	1.0	1.4	mA	1.8	FOSC = 8 MHz HFINTOSC mode
		—	1.8	2.3	mA	3.0	
D018		—	1.0	1.5	mA	1.8	FOSC = 8 MHz HFINTOSC mode **(Note 5)**
		—	1.8	2.3	mA	3.0	
		—	2.0	2.8	mA	5.0	
D019		—	1.5	2.2	mA	1.8	FOSC = 16 MHz HFINTOSC mode
		—	2.8	3.7	mA	3.0	
D019		—	1.7	2.3	mA	1.8	FOSC = 16 MHz HFINTOSC mode **(Note 5)**
		—	2.9	3.9	mA	3.0	
		—	3.1	4.1	mA	5.0	
D020		—	4.8	6.2	mA	3.0	FOSC = 32 MHz HFINTOSC mode
		—	5.0	7.5	mA	3.6	
D020		—	4.8	6.5	mA	3.0	FOSC = 32 MHz HFINTOSC mode
		—	5.0	7.5	mA	5.0	
D021		—	410	550	µA	1.8	FOSC = 4 MHz EXTRC mode **(Note 3)**
		—	710	990	µA	3.0	
D021		—	430	700	µA	1.8	FOSC = 4 MHz EXTRC mode **(Note 3, Note 5)**
		—	730	1100	µA	3.0	
		—	860	1400	µA	5.0	
D022		—	5.0	6.2	mA	3.0	FOSC = 32 MHz HS Oscillator mode **(Note 6)**
		—	6.0	7.5	mA	3.6	
D022		—	5.0	6.5	mA	3.0	FOSC = 32 MHz HS Oscillator mode **(Note 5, Note 6)**
		—	5.2	7.5	mA	5.0	

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: 0.1 µF capacitor on VCAP (RA0).

6: 8 MHz crystal oscillator with 4x PLL enabled.

FIGURE 31-67: PIC16F1937 FVR_ADC

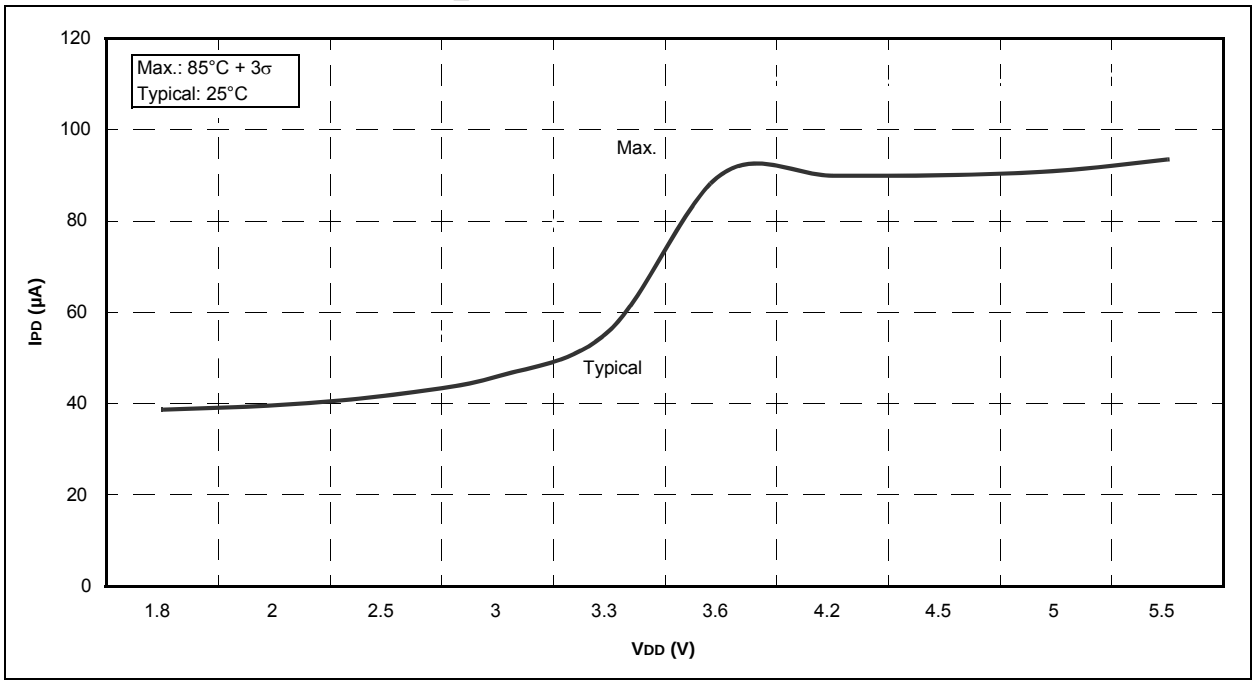
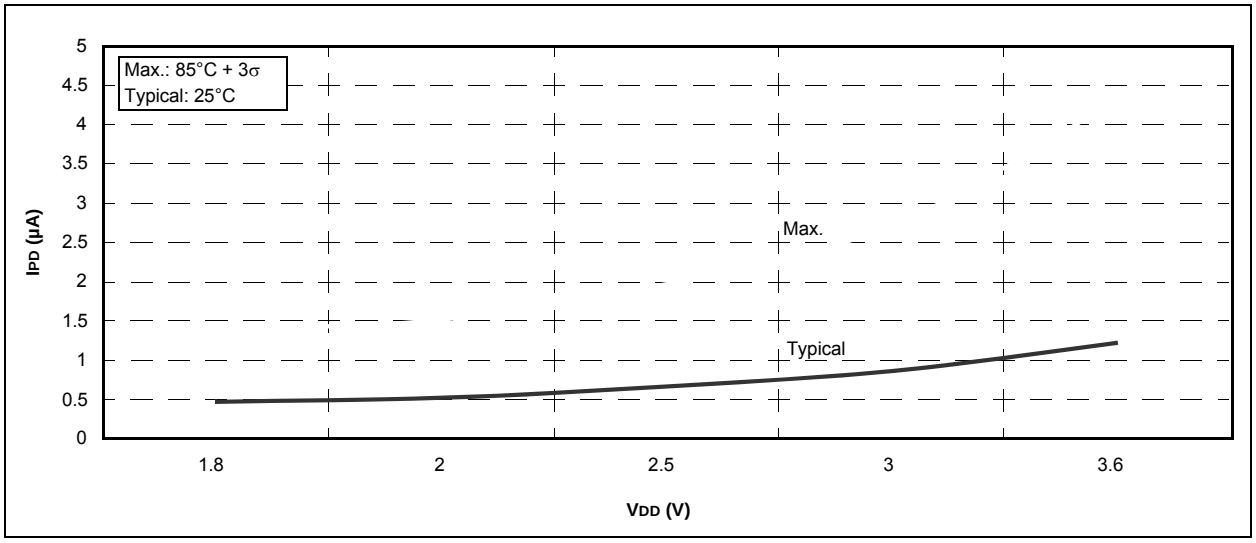
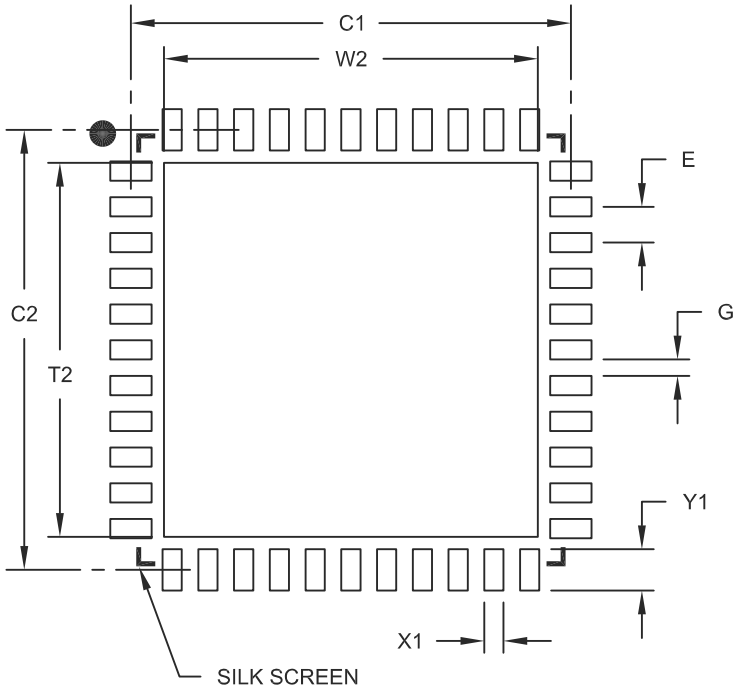


FIGURE 31-68: PIC16LF1937 WDT



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

NOTES: