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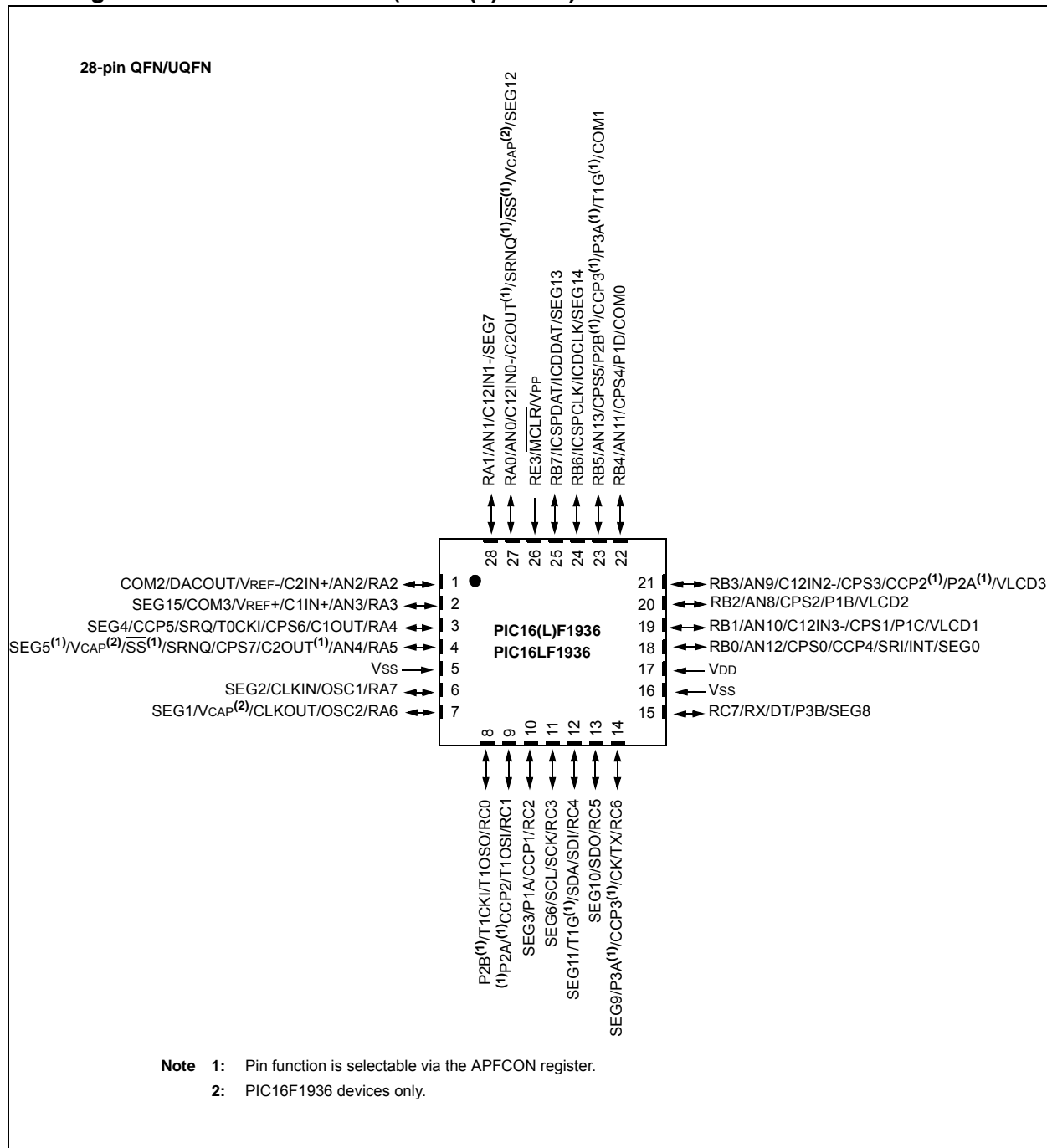
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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f1934t-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16f1934t-i-pt</a>

# PIC16(L)F1934/6/7

## Pin Diagram – 28-Pin QFN/UQFN (PIC16(L)F1936)



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**TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RD6 <sup>(4)</sup> /CPS14/P1C/SEG19	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
	P1C	—	CMOS	PWM output.
	SEG19	—	AN	LCD analog output.
RD7 <sup>(4)</sup> /CPS15/P1D/SEG20	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
	P1D	—	CMOS	PWM output.
	SEG20	—	AN	LCD analog output.
RE0 <sup>(5)</sup> /AN5/P3A <sup>(1)</sup> /CCP3 <sup>(1)</sup> /SEG21	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	P3A	—	CMOS	PWM output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SEG21	—	AN	LCD analog output.
RE1 <sup>(5)</sup> /AN6/P3B/SEG22	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	P3B	—	CMOS	PWM output.
	SEG22	—	AN	LCD analog output.
RE2 <sup>(5)</sup> /AN7/CCP5/SEG23	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG23	—	AN	LCD analog output.
RE3/MCLR/VPP	RE3	TTL	—	General purpose input.
	MCLR	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C™ = Schmitt Trigger input with I<sup>2</sup>C levels  
HV = High Voltage    XTAL = Crystal

- Note** 1: Pin function is selectable via the APFCON register.  
2: PIC16F1934/6/7 devices only.  
3: PIC16(L)F1936 devices only.  
4: PORTD is available on PIC16(L)F1934/7 devices only.  
5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

# PIC16(L)F1934/6/7

## 4.5 Device ID and Revision ID

The memory location 8006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See **Section 11.5 “User ID, Device ID and Configuration Word Access”** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

### REGISTER 4-3: DEVICEID: DEVICE ID REGISTER<sup>(1)</sup>

R	R	R	R	R	R	R
DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2
bit 13						bit 7

R	R	R	R	R	R	R
DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 6						bit 0

<b>Legend:</b>			U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit		'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set		x = Bit is unknown

bit 13-5      **DEV<8:0>:** Device ID bits  
100011010 = PIC16F1934  
100011011 = PIC16F1936  
100011100 = PIC16F1937  
100100010 = PIC16LF1934  
100100011 = PIC16LF1936  
100100100 = PIC16LF1937

bit 4-0      **REV<4:0>:** Revision ID bits  
These bits are used to identify the revision.

**Note 1:** This location cannot be written.

**REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER**

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<4:0>:** Frequency Tuning bits

011111 = Maximum frequency

011110 =

•

•

•

000001 =

000000 = Oscillator module is running at the factory-calibrated frequency.

111111 =

•

•

•

100000 = Minimum frequency

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		81
OSCSTAT	T1OSCR	PLLRL	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	82
OSCTUNE	—	—	TUN<5:0>						83
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	—	CCP2IE <sup>(1)</sup>	100
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	—	CCP2IF <sup>(1)</sup>	103
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR1ON	203

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

**Note 1:** PIC16F1934 only.

**TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES**

Name	Bits	Bit -7	Bit -6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD	62
	7:0	CP	MCLRE	PWRTÉ	WDTE<1:0>		FOSC<2:0>			
CONFIG2	13:8	—	—	LVP	DEBUG	—	BORV	STVREN	PLLEN	64
	7:0	—	—	VCAPEN<1:0> <sup>(1)</sup>		—	—	WRT<1:0>		

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

**Note 1:** PIC16F1934/6/7 only.

## 12.0 I/O PORTS

Depending on the device selected and peripherals enabled, there are up to five ports available. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

Each port has three standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)
- INLVx (input level control)

**TABLE 12-1: PORT AVAILABILITY PER DEVICE**

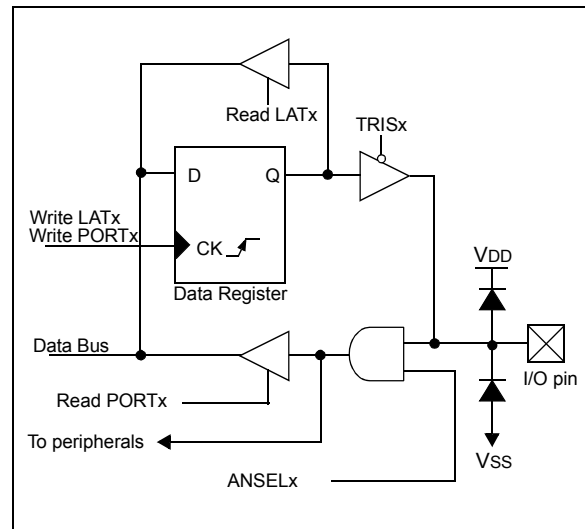
Device	PORTA	PORTB	PORTC	PORTD	PORTE
PIC16(L)F1934	•	•	•	•	•
PIC16(L)F1936	•	•	•		•
PIC16(L)F1937	•	•	•	•	•

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 12-1.

**FIGURE 12-1: GENERIC I/O PORT OPERATION**



**EXAMPLE 12-1: INITIALIZING PORTA**

```

; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL PORTA      ;
CLRF PORTA         ;Init PORTA
BANKSEL LATA        ;Data Latch
CLRF LATA          ;
BANKSEL ANSELA      ;
CLRF ANSELA        ;digital I/O
BANKSEL TRISA       ;
MOVLW B'00111000'  ;Set RA<5:3> as inputs
MOVWF TRISA         ;and set RA<2:0> as
                   ;outputs

```

## 13.0 INTERRUPT-ON-CHANGE

The PORTB pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual PORT IOC pin, or combination of PORT IOC pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

### 13.1 Enabling the Module

To allow individual PORTB pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

### 13.2 Individual Pin Configuration

For each PORTB pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated IOCBPx bit of the IOCBP register is set. To enable a pin to detect a falling edge, the associated IOCBNx bit of the IOCBN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both the IOCBPx bit and the IOCBNx bit of the IOCBP and IOCBN registers, respectively.

## 13.3 Interrupt Flags

The IOCBFx bits located in the IOCBF register are status flags that correspond to the interrupt-on-change pins of PORTB. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCBFx bits.

### 13.4 Clearing Interrupt Flags

The individual status flags, (IOCBFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

#### EXAMPLE 13-1:

```
MOVLW    0xff
XORWF    IOCBF, W
ANDWF    IOCBF, F
```

### 13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCBF register will be updated prior to the first instruction executed out of Sleep.

**FIGURE 13-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM**

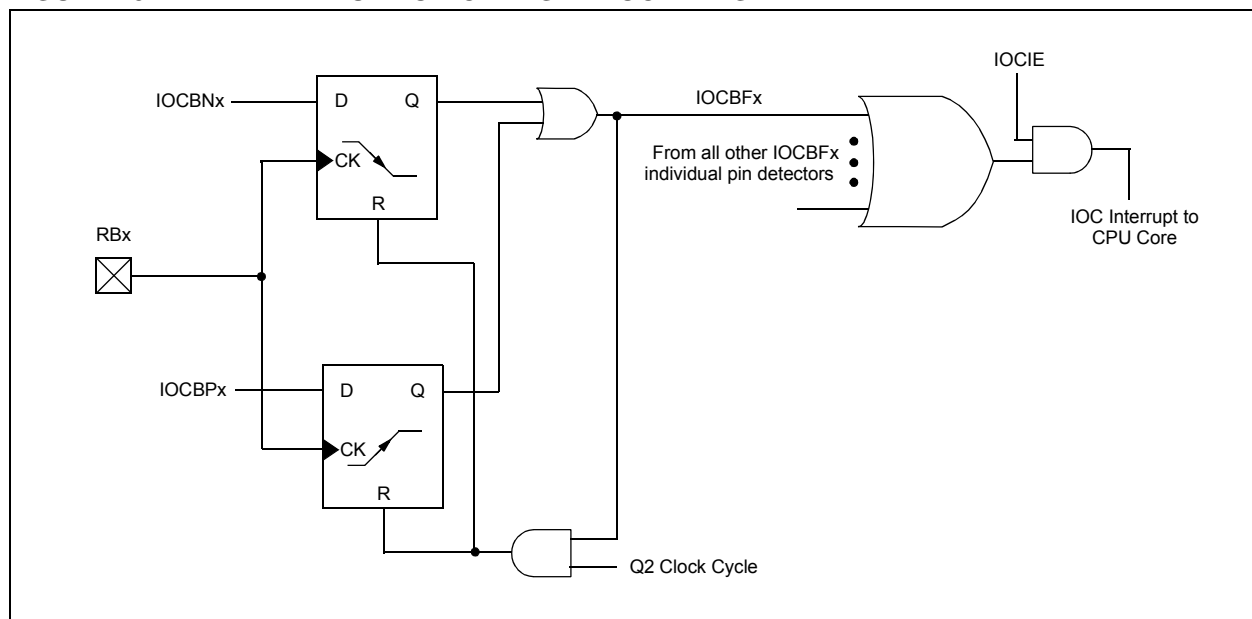




FIGURE 17-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

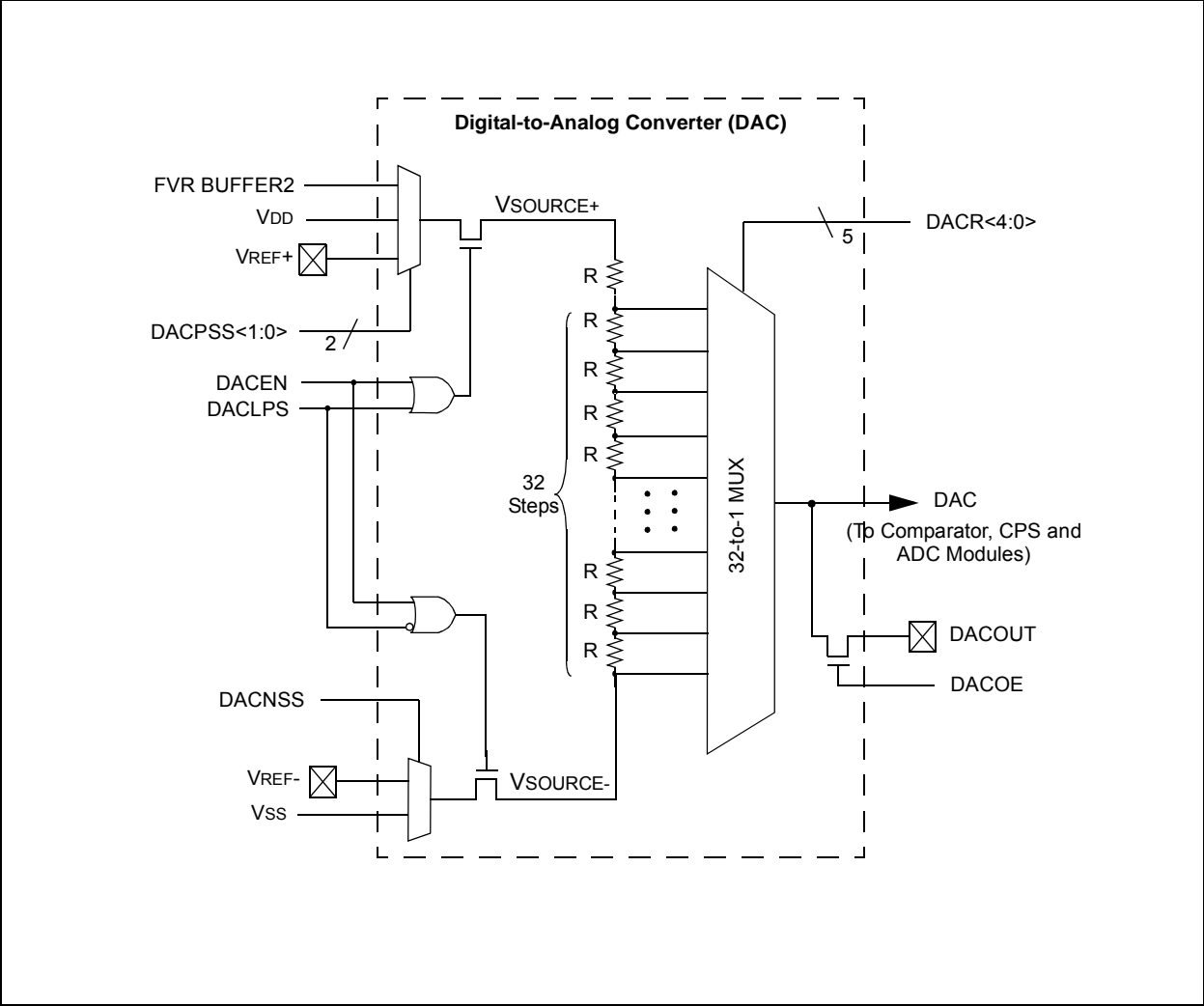
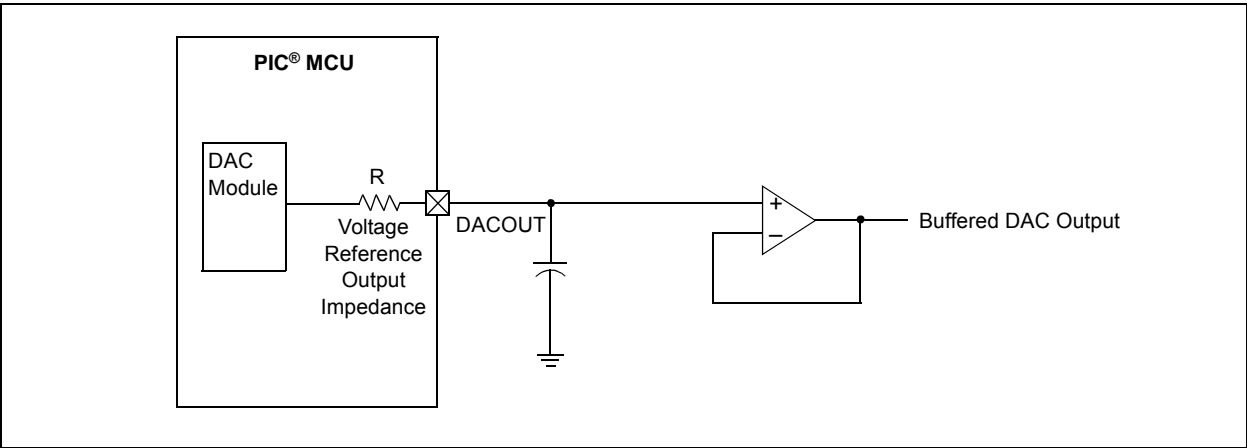
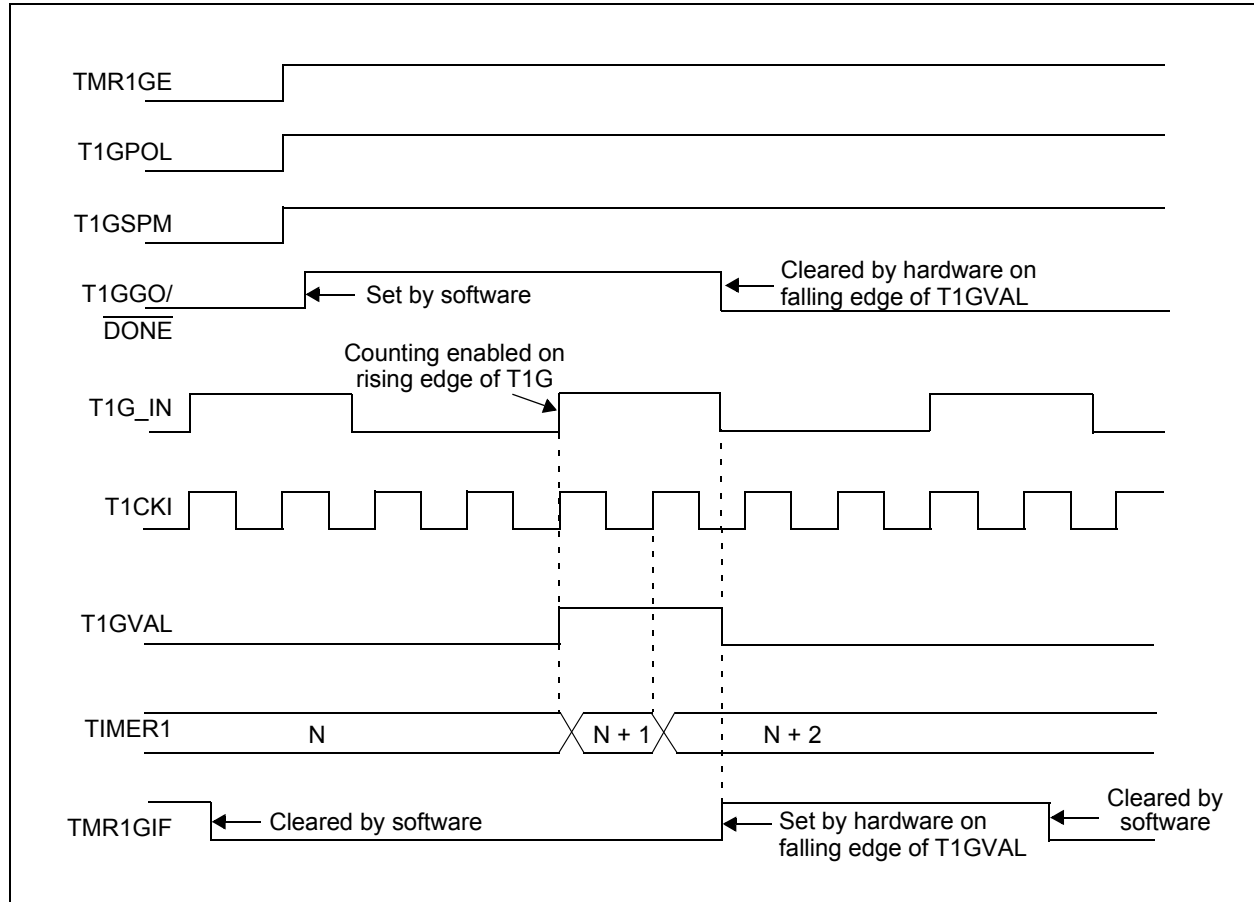


FIGURE 17-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



NOTES:

**FIGURE 21-5: TIMER1 GATE SINGLE-PULSE MODE**



\_\_\_\_\_

**Note:** When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the Off state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

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## 24.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 24-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and Status bits appropriately set).

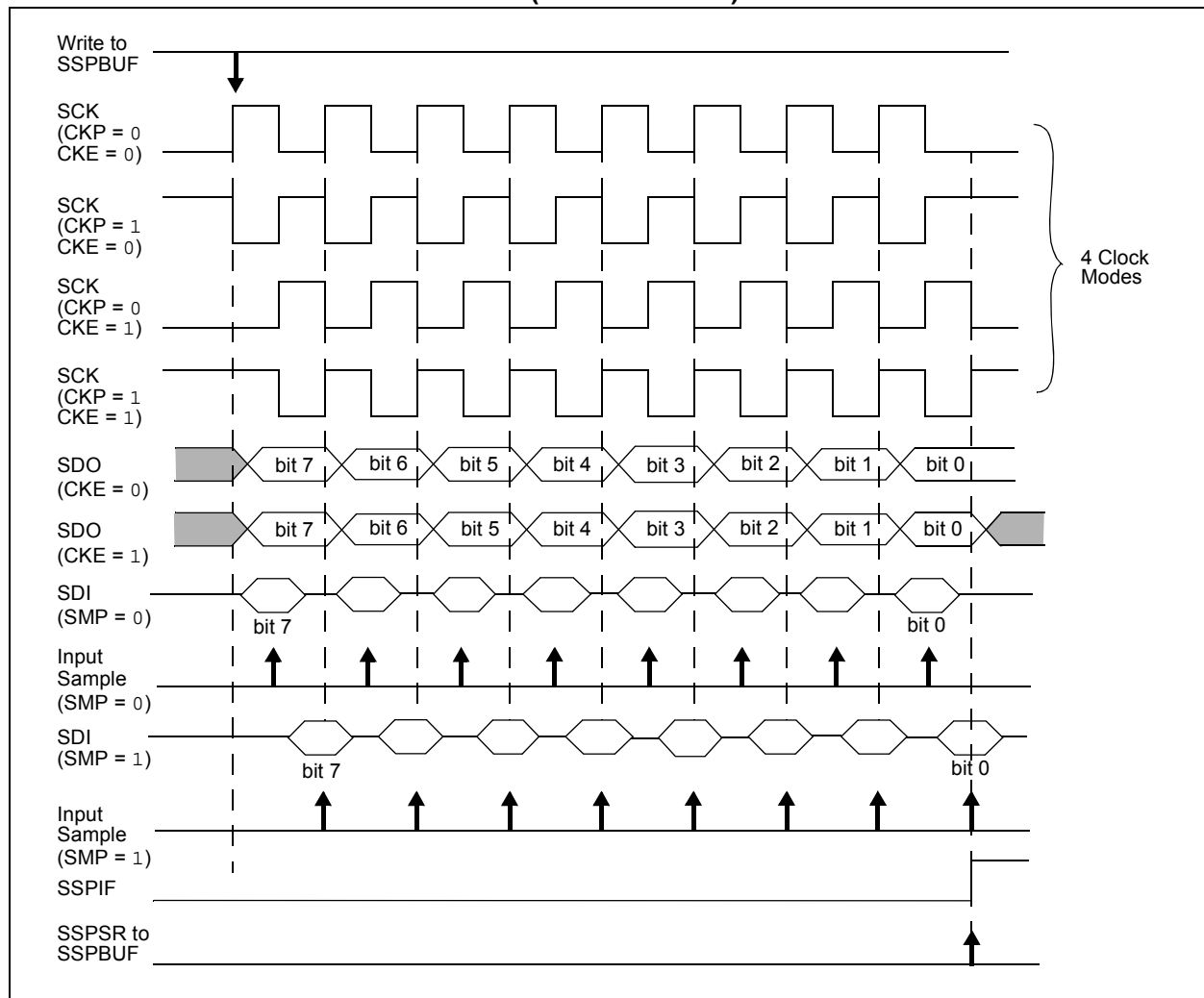
The clock polarity is selected by appropriately programming the CKP bit of the SSPCON1 register and the CKE bit of the SSPSTAT register. This then, would give waveforms for SPI communication as shown in Figure 24-6, Figure 24-8 and Figure 24-9, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- $F_{osc}/4$  (or  $T_{cy}$ )
- $F_{osc}/16$  (or  $4 * T_{cy}$ )
- $F_{osc}/64$  (or  $16 * T_{cy}$ )
- Timer2 output/2
- $F_{osc}/(4 * (SSPADD + 1))$

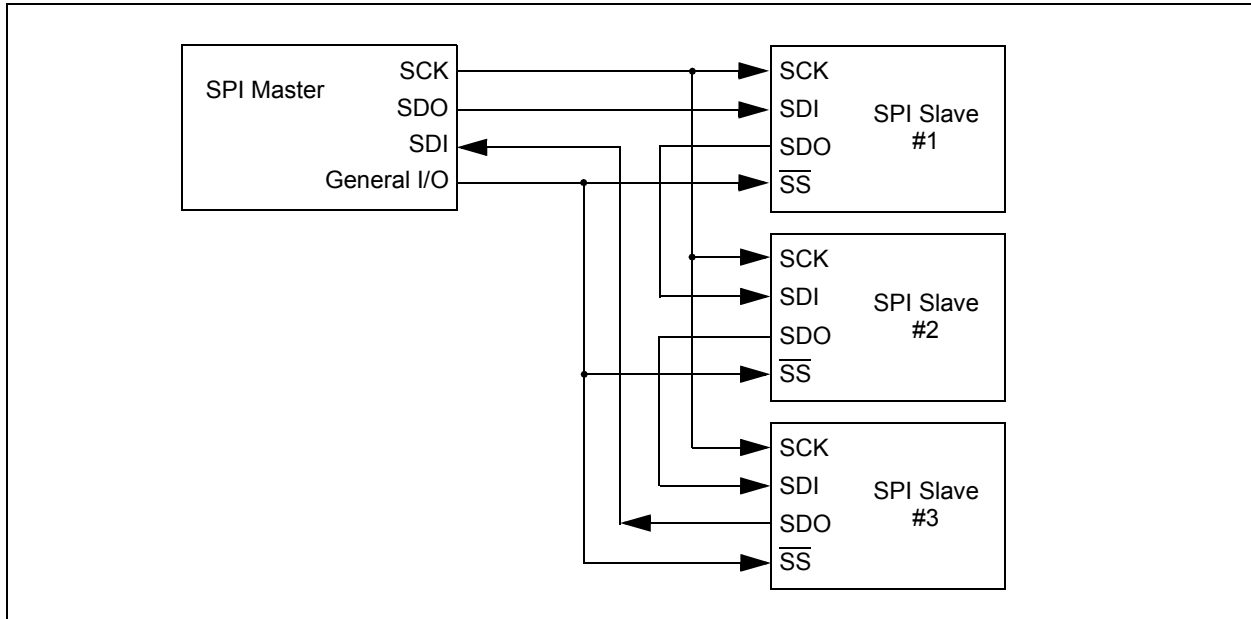
Figure 24-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

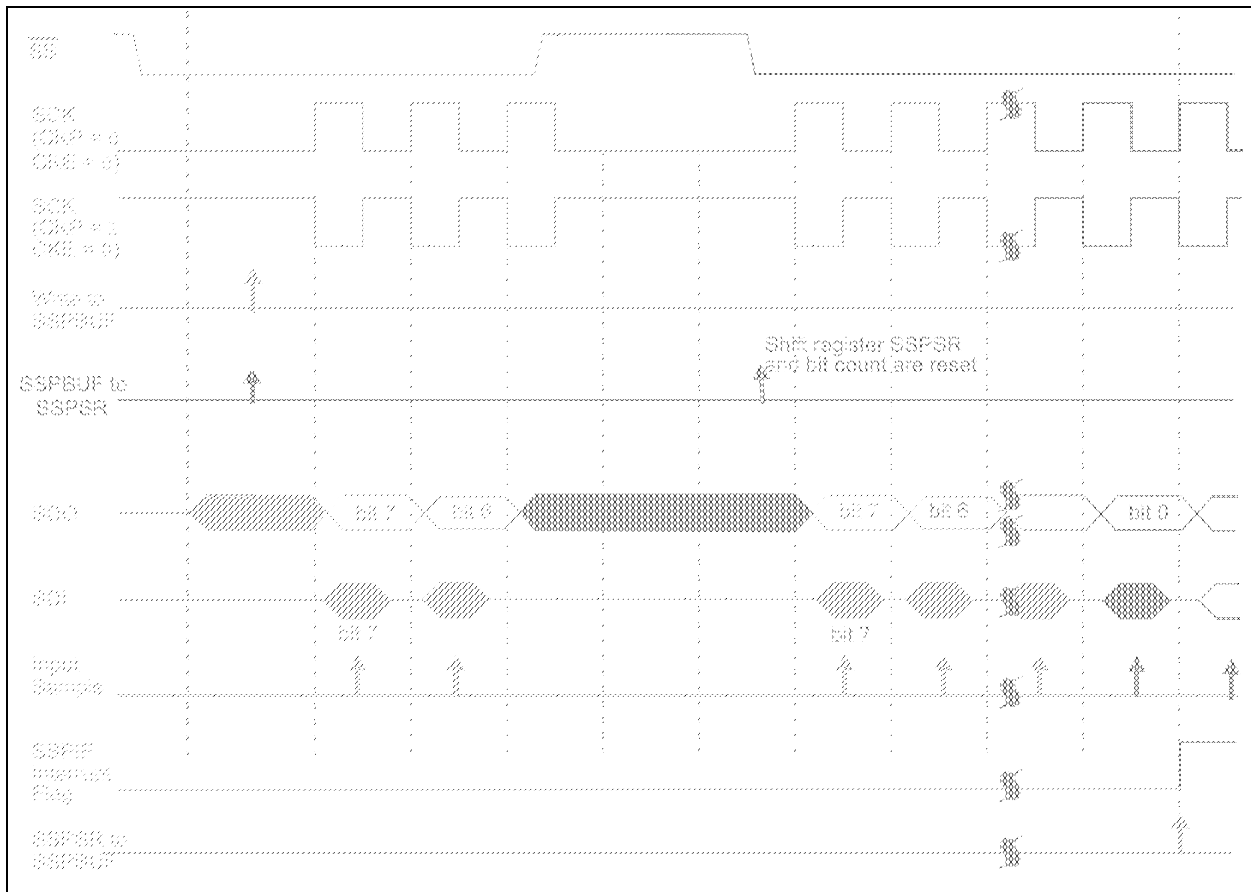
**FIGURE 24-6: SPI MODE WAVEFORM (MASTER MODE)**



**FIGURE 24-7: SPI DAISY-CHAIN CONNECTION**



**FIGURE 24-8: SLAVE SELECT SYNCHRONOUS WAVEFORM**



**TABLE 25-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)**

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

## 27.3 LCD Bias Voltage Generation

The LCD module can be configured for one of three bias types:

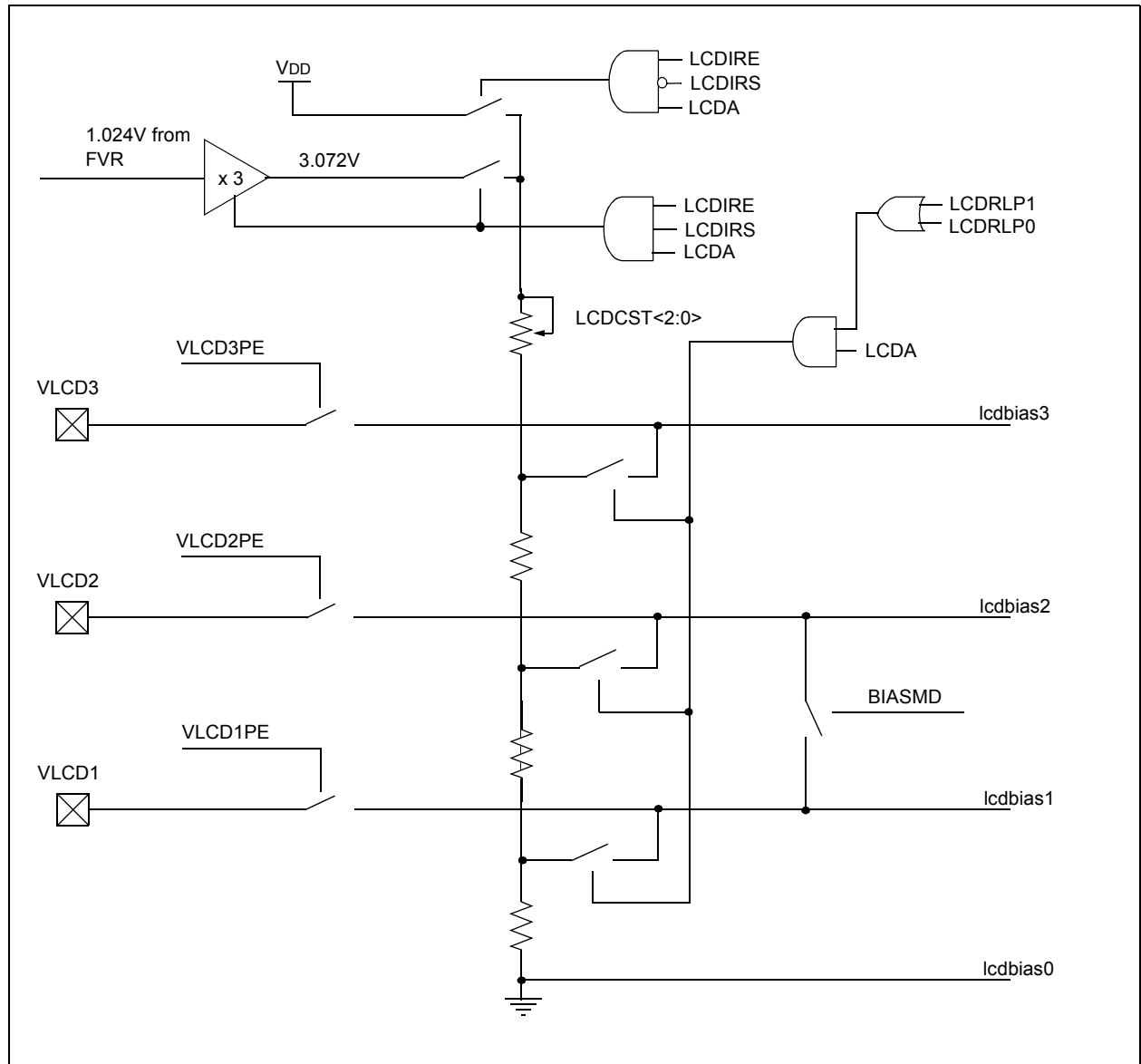
- Static Bias (2 voltage levels: VSS and VLCD)
- 1/2 Bias (3 voltage levels: VSS, 1/2 VLCD and VLCD)
- 1/3 Bias (4 voltage levels: VSS, 1/3 VLCD, 2/3 VLCD and VLCD)

**TABLE 27-2: LCD BIAS VOLTAGES**

	Static Bias	1/2 Bias	1/3 Bias
LCD Bias 0	VSS	VSS	VSS
LCD Bias 1	—	1/2 VDD	1/3 VDD
LCD Bias 2	—	1/2 VDD	2/3 VDD
LCD Bias 3	VLCD3	VLCD3	VLCD3

So that the user is not forced to place external components and use up to three pins for bias voltage generation, internal contrast control and an internal reference ladder are provided internally. Both of these features may be used in conjunction with the external VLCD<3:1> pins, to provide maximum flexibility. Refer to Figure 27-3.

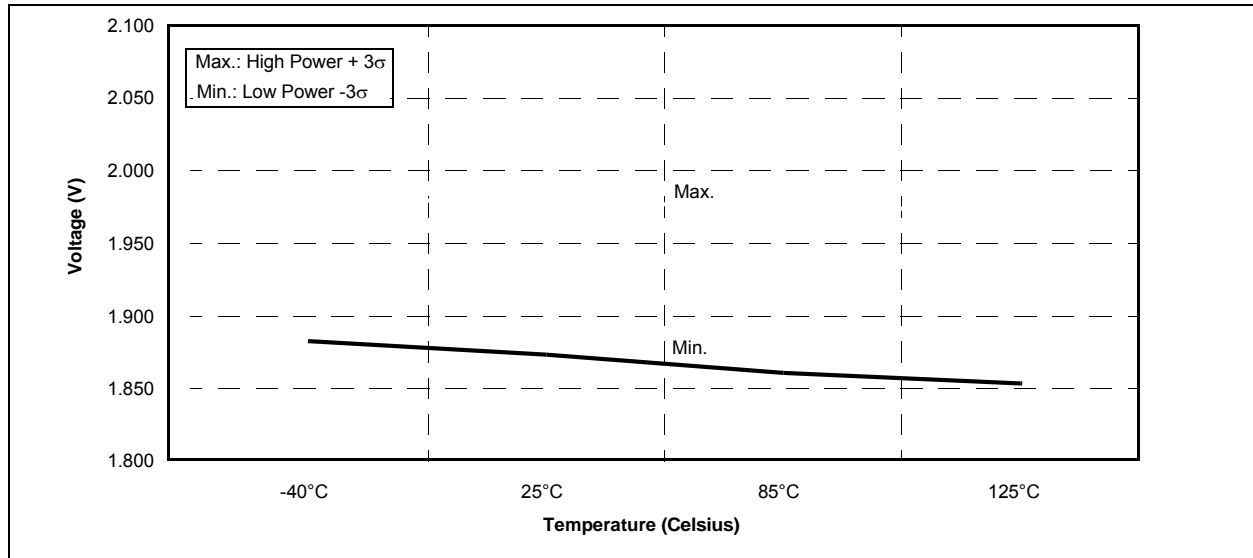
**FIGURE 27-3: LCD BIAS VOLTAGE GENERATION BLOCK DIAGRAM**



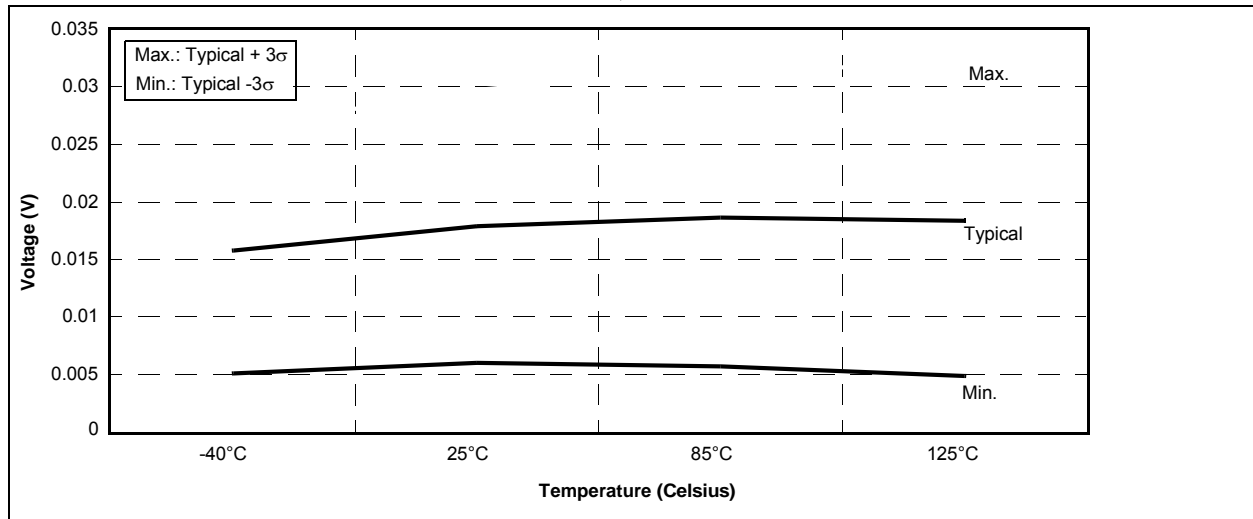


## 31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

**FIGURE 31-1: PIC16F1934/6/7 RESET VOLTAGE, BOR = 1.9V**



**FIGURE 31-2: PIC16F1934/6/7 HYSTERESIS, BOR = 1.9V**



# PIC16(L)F1934/6/7

FIGURE 31-3: PIC16F1934/6/7 RESET VOLTAGE, BOR = 2.5V

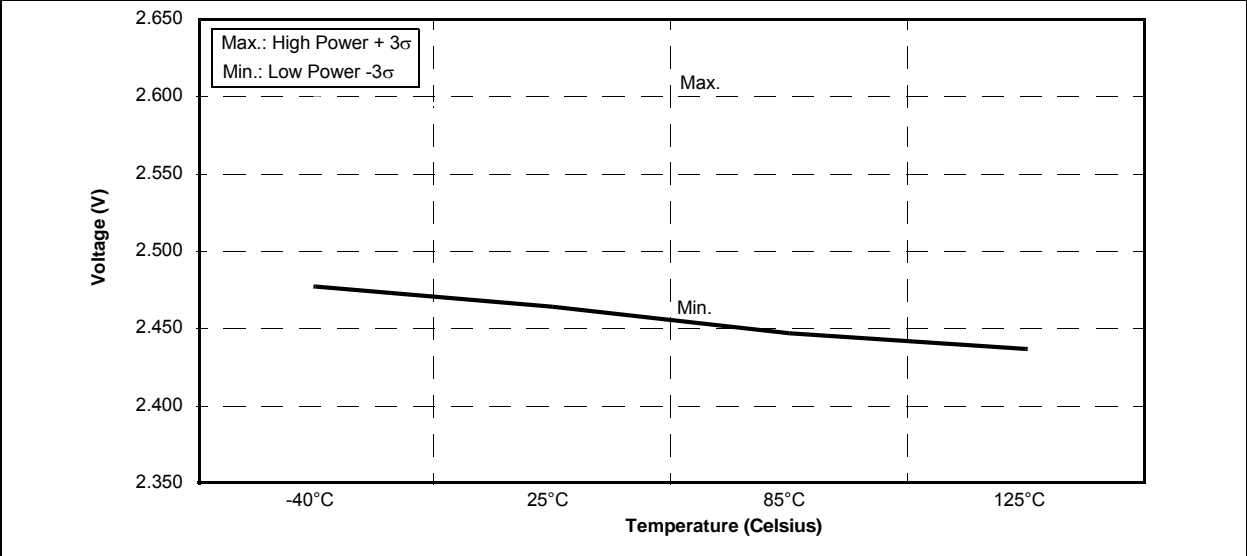
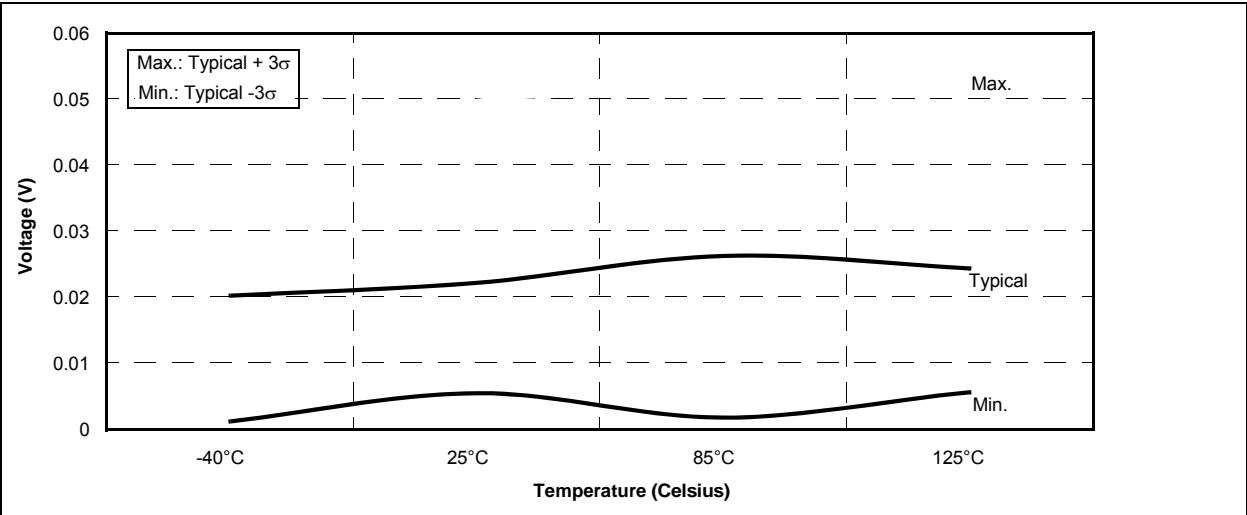


FIGURE 31-4: PIC16F1934/6/7 HYSTERESIS, BOR = 2.5V



# PIC16(L)F1934/6/7

FIGURE 31-17: PIC16LF1937 HF INTOSC MODE, Fosc = 8 MHz

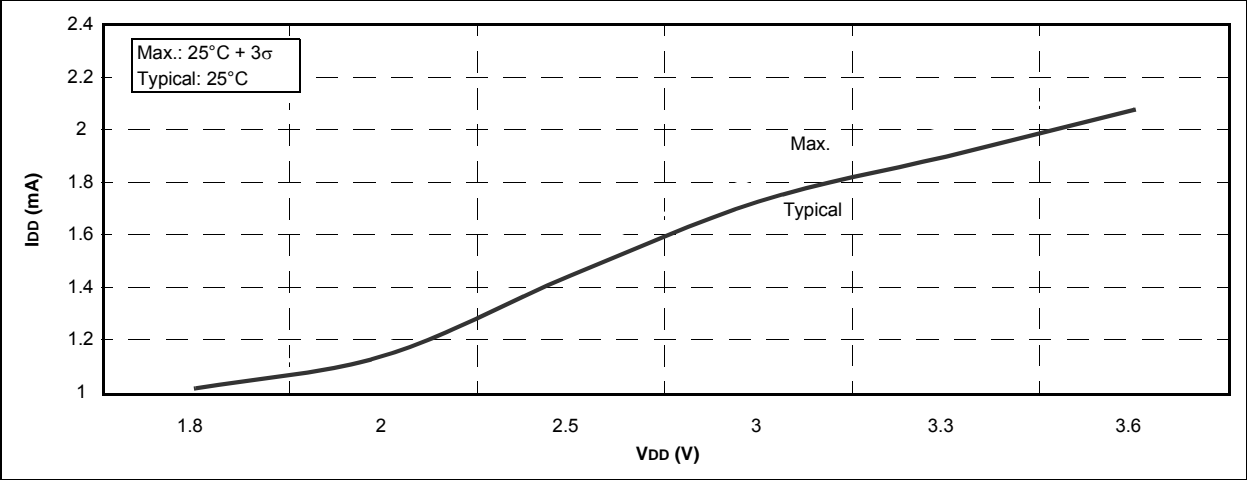


FIGURE 31-18: PIC16F1937 MF INTOSC MODE, Fosc = 500 kHz

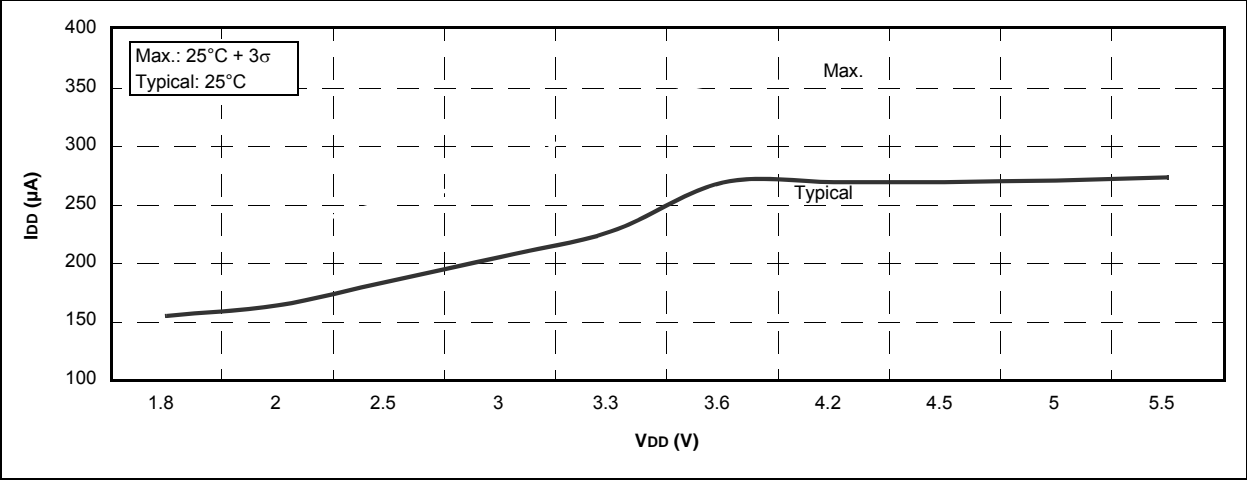
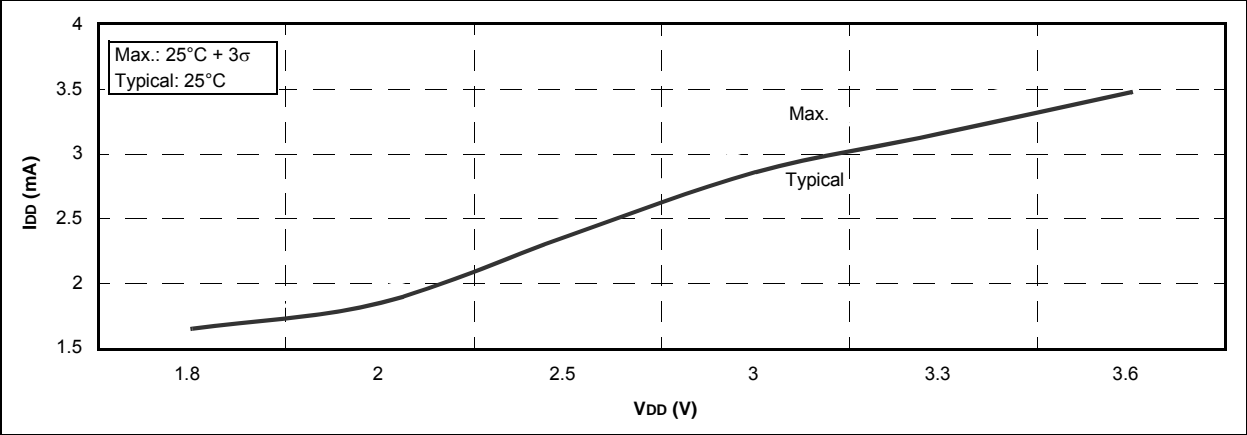
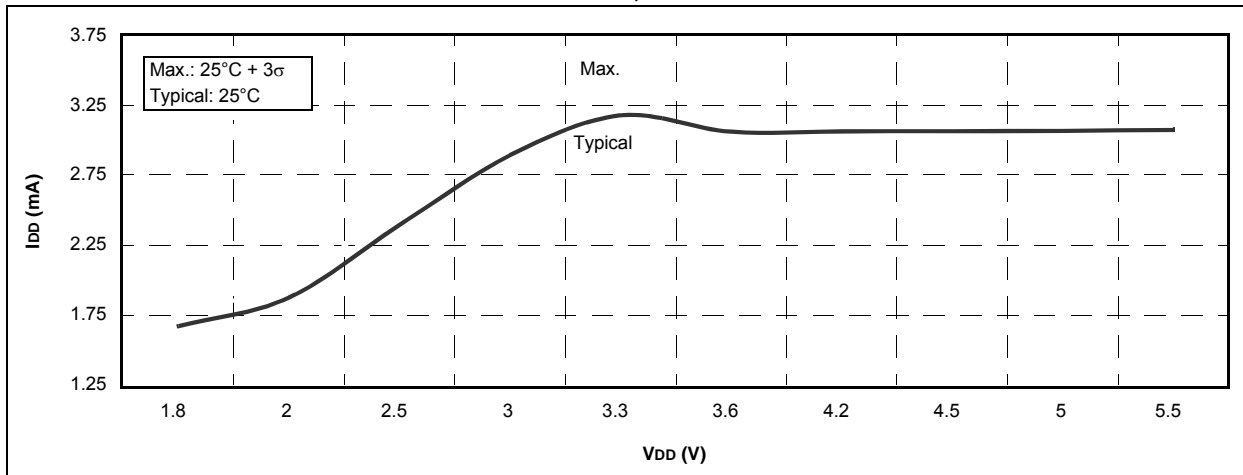


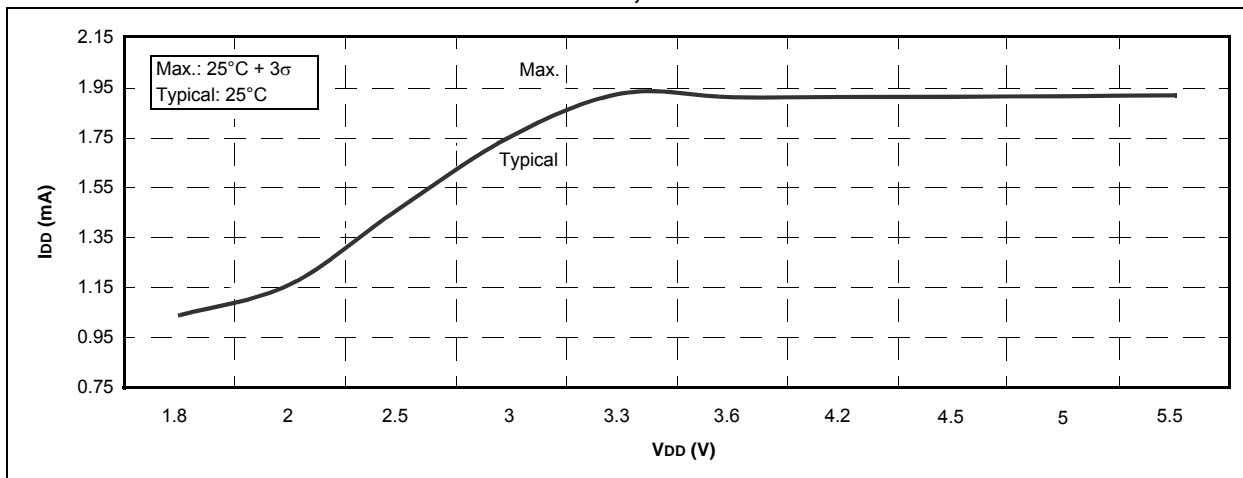
FIGURE 31-19: PIC16LF1937 HF INTOSC MODE, Fosc = 16 MHz



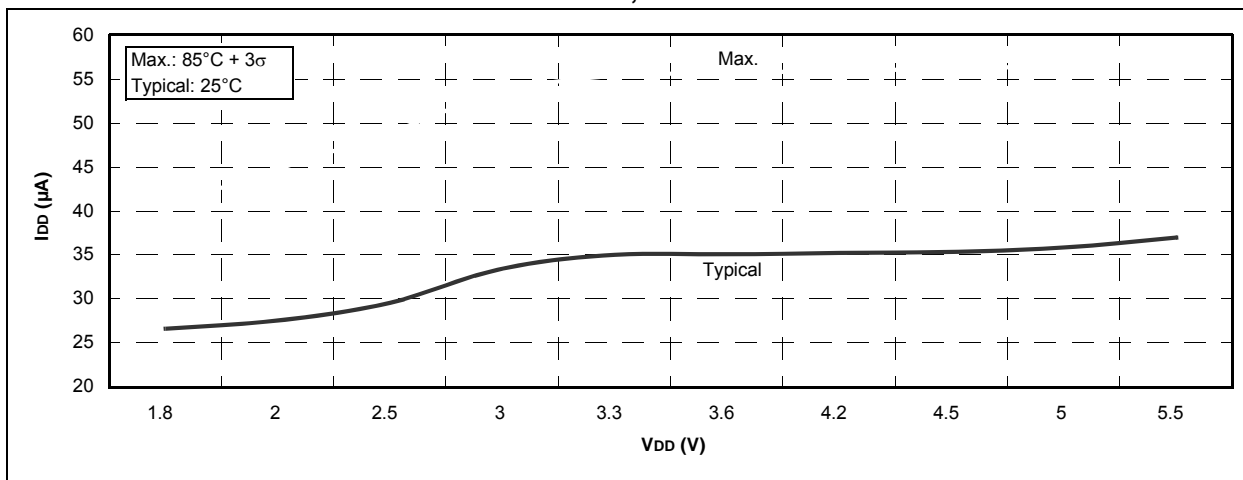
**FIGURE 31-20: PIC16F1937 HF INTOSC MODE,  $F_{osc} = 16\text{ MHz}$**



**FIGURE 31-21: PIC16F1937 HF INTOSC MODE,  $F_{osc} = 8\text{ MHz}$**



**FIGURE 31-22: PIC16F1937 LF INTOSC MODE,  $F_{osc} = 32\text{ kHz}$**



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NOTES: