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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1936-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagram – 28-Pin SPDIP/SOIC/SSOP (PIC16(L)F1936)



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2											
100h ⁽²⁾	INDF0	Addressing (not a physi	Addressing this location uses contents of FSR0H/FSR0L to address data memory not a physical register)							XXXX XXXX	xxxx xxxx
101h ⁽²⁾	INDF1	Addressing (not a physi	Addressing this location uses contents of FSR1H/FSR1L to address data memory not a physical register)								xxxx xxxx
102h ⁽²⁾	PCL	Program Co	ounter (PC) Le	ast Significant	t Byte					0000 0000	0000 0000
103h ⁽²⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
104h ⁽²⁾	FSR0L	Indirect Data	a Memory Ado	Iress 0 Low P	ointer					0000 0000	uuuu uuuu
105h ⁽²⁾	FSR0H	Indirect Data	a Memory Add	lress 0 High P	ointer					0000 0000	0000 0000
106h ⁽²⁾	FSR1L	Indirect Data	a Memory Ado	Iress 1 Low P	ointer					0000 0000	uuuu uuuu
107h ⁽²⁾	FSR1H	Indirect Data	a Memory Add	lress 1 High P	ointer					0000 0000	0000 0000
108h ⁽²⁾	BSR	—	-	_		I	BSR<4:0>			0 0000	0 0000
109h ⁽²⁾	WREG	Working Re	gister							0000 0000	uuuu uuuu
10Ah ^(1, 2)	PCLATH	—	Write Buffer f	or the upper 7	bits of the Pro	ogram Counter	r			-000 0000	-000 0000
10Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
10Ch	LATA	PORTA Dat	a Latch							xxxx xxxx	uuuu uuuu
10Dh	LATB	PORTB Dat	a Latch							xxxx xxxx	uuuu uuuu
10Eh	LATC	PORTC Dat	a Latch							xxxx xxxx	uuuu uuuu
10Fh ⁽³⁾	LATD	PORTD Dat	a Latch							xxxx xxxx	uuuu uuuu
110h	LATE	—	—	—	—	—	LATE2 ⁽³⁾	LATE1 ⁽³⁾	LATE0 ⁽³⁾	xxx	uuu
111h	CM1CON0	C10N	C10UT	C10E	C1POL	—	C1SP	C1HYS	C1SYNC	0000 -100	0000 -100
112h	CM1CON1	C1INTP	C1INTN	C1PCH1	C1PCH0	—	—	C1NC	H<1:0>	000000	000000
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	0000 -100	0000 -100
114h	CM2CON1	C2INTP	C2INTN	C2PCH1	C2PCH0	—	_	C2NCI	H<1:0>	000000	000000
115h	CMOUT	—	_	_	_	_		MC2OUT	MC1OUT	00	00
116h	BORCON	SBOREN	_	_	—	—		—	BORRDY	1q	u u
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFV	R<1:0>	0000 00p0	0q00 0000
118h	DACCON0	DACEN	DACLPS	DACOE		DACPS	S<1:0>		DACNSS	000- 00-0	000- 00-0
119h	DACCON1					D	ACR<4:0>	-	-	0 0000	0 0000
11Ah	SRCON0	SRLEN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR	0000 0000	0000 0000
11Bh	SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	0000 0000	0000 0000
11Ch	—	Unimpleme	nted							—	_
11Dh	APFCON	-	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	-000 0000	-000 0000
11Eh	—	Unimpleme	Unimplemented						—	—	
11Fh	—	Unimpleme	nted							—	—

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.

These registers can be addressed from any bank. 2:

These registers/bits are not implemented on PIC16(L)F1936 devices, read as '0'. 3:

4: Unimplemented, read as '1'.





2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT not available in all Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in the applicable Electrical Specifications Chapter.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	
ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	
bit 7	•						bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'		
u = Bit is unchanged		x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared					

REGISTER 12-17: ANSELD: PORTD ANALOG SELECT REGISTER⁽²⁾

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

- 2: ANSELD register is not implemented on the PIC16(L)F1936. Read as '0'.
- 3: PORTD implemented on PIC16(L)F1934/7 devices only.

TABLE 12-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD ⁽¹

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	146
CCPxCON	PxM∙	<1:0>	DCxB	<1:0>		CCPxI	vl<3:0>		234
CPSCON0	CPSON	_	—	—	CPSRN	IG<1:0>	CPSOUT	T0XCS	323
CPSCON1	—	_	—	—	CPSCH		CH<3:0>		324
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	145
LCDCON	LCDEN	SLPEN	WERR	—	CS<	:1:0>	LMUX	(<1:0>	329
LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	333
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	145
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	145

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

Note 1: These registers are not implemented on the PIC16(L)F1936 devices, read as '0'.

bit 7-0 **ANSD<7:0>**: Analog Select between Analog or Digital Function on Pins RD<7:0>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

15.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 15-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—			CHS<4:0>			GO/DONE	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7		Unimplemented: Read as '0'
bit 6-2	2	CHS<4:0>: Analog Channel Select bits
		00000 = ANO
		00001 = AN1
		00010 = AN2
		00011 = AN3
		00100 = AN4
		$00101 = AN5^{(4)}$
		$00110 = AN6^{(4)}$
		$00111 = AN7^{(4)}$
		01000 = AN8
		01001 = AN9
		01010 = AN10
		01011 = AN11
		01100 = AN12
		01110 - Reserved No channel connected
		•
		•
		•
		11100 = Reserved. No channel connected.
		11101 = Temperature Indicator ⁽³⁾
		11110 = DAC output ⁽¹⁾
		11111 = FVR (Fixed Voltage Reference) Buffer 1 Output ⁽²⁾
bit 1		GO/DONE: A/D Conversion Status bit
		1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
		This bit is automatically cleared by hardware when the A/D conversion has completed.
		0 = A/D conversion completed/not in progress
bit 0		ADON: ADC Enable bit
		1 = ADC is enabled
		0 = ADC is disabled and consumes no operating current
Note	1:	See Section 17.0 "Digital-to-Analog Converter (DAC) Module" for more information
	2.	See Section 14.0 "Fixed Voltage Reference (EVR)" for more information
	2. 2.	See Section 16.0 "Temperature Indicator Medule" for more information
	J:	See Section 16.0 remperature indicator module for more information.

4: Not available on the PIC16(L)F1936.

20.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION_REG register.

Note:	The Watchdog Timer (WDT) uses its own
	independent prescaler.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

20.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the
	processor from Sleep since the timer is
	frozen during Sleep.

20.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in the applicable Electrical Specifications Chapter.

20.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.

23.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains three Enhanced Capture/Compare/PWM modules (ECCP1, ECCP2, and ECCP3) and two standard Capture/Compare/PWM modules (CCP4 and CCP5).

The Capture and Compare functions are identical for all five CCP modules (ECCP1, ECCP2, ECCP3, CCP4, and CCP5). The only differences between CCP modules are in the Pulse-Width Modulation (PWM) function. The standard PWM function is identical in modules, CCP4 and CCP5. In CCP modules ECCP1, ECCP2, and ECCP3, the Enhanced PWM function has slight variations from one another. Full-Bridge ECCP modules have four available I/O pins while Half-Bridge ECCP modules only have two available I/O pins. See Table 23-1 for more information.

- Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
 - 2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to ECCP1, ECCP2, ECCP3, CCP4 and CCP5. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

TABLE 23-1:PWM RESOURCES

Device Name	ECCP1	ECCP2	ECCP3	CCP4	CCP5
PIC16(L)F1936	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM
PIC16(L)F1934/7	Enhanced PWM Full-Bridge	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM





24.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is a reserved address in the I²C protocol, defined as address 0x00. When the GCEN bit of the SSPCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave read SSPBUF software can and respond. Figure 24-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.





24.5.9 SSP MASK REGISTER

An SSP Mask (SSPMSK) register (Register 24-5) is available in I²C Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero ('0') bit in the SSPMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

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24.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 24-37). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 24-38).

FIGURE 24-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)



FIGURE 24-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



25.3.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

25.3.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 25-7), and asynchronously if the device is in Sleep mode (Figure 25-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

25.3.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be 10 or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

<u>WUE Bit</u>

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

25.4 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

25.4.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for Synchronous Master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

25.4.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

25.4.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

25.4.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data
	memory, so it is not available to the user.

- 25.4.1.4 Synchronous Master Transmission Set-up:
- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 25.3 "EUSART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Disable Receive mode by clearing bits SREN and CREN.
- 4. Enable Transmit mode by setting the TXEN bit.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
- 8. Start transmission by loading data to the TXREG register.

27.4.3 AUTOMATIC POWER MODE SWITCHING

As an LCD segment is electrically only a capacitor, current is drawn only during the interval where the voltage is switching. To minimize total device current, the LCD internal reference ladder can be operated in a different power mode for the transition portion of the duration. This is controlled by the LCDRL register (Register 27-7). The LCDRL register allows switching between two power modes, designated 'A' and 'B'. 'A' Power mode is active for a programmable time, beginning at the time when the LCD segments transition. 'B' Power mode is the remaining time before the segments or commons change again. The LRLAT<2:0> bits select how long, if any, that the 'A' Power mode is active. Refer to Figure 27-4.

To implement this, the 5-bit prescaler used to divide the 32 kHz clock down to the LCD controller's 1 kHz base rate is used to select the power mode.

FIGURE 27-4: LCD INTERNAL REFERENCE LADDER POWER MODE SWITCHING DIAGRAM – TYPE A



R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	
LRLAP<1:0>		LRLBP	P<1:0>	—		LRLAT<2:0>		
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable b	it	U = Unimplem	nented bit, read	as '0'		
u = Bit is unchanged		x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets						
1' = Bit is set	t	'0' = Bit is clea	red					
bit 7-6	LRLAP<1:0>: During Time ir 00 = Internal 01 = Internal 10 = Internal 11 = Internal	: LCD Reference nterval A (Refer LCD Reference LCD Reference LCD Reference LCD Reference	e Ladder A Tin to Figure 27-4 Ladder is pow Ladder is pow Ladder is pow Ladder is pow	ne Power Contr): vered down and vered in Low-Po vered in Mediun vered in High-Po	ol bits unconnected ower mode n-Power mode ower mode			
bit 5-4	 LRLBP<1:0>: LCD Reference Ladder B Time Power Control bits During Time interval B (Refer to Figure 27-4): 00 = Internal LCD Reference Ladder is powered down and unconnected 01 = Internal LCD Reference Ladder is powered in Low-Power mode 10 = Internal LCD Reference Ladder is powered in Medium-Power mode 11 = Internal LCD Reference Ladder is powered in High-Power mode 							
bit 3	Unimplement	ted: Read as '0'						
bit 2-0	LRLAT<2:0>: LCD Reference Ladder A Time Interval Control bits Sets the number of 32 kHz clocks that the A Time Interval Power mode is active							
	For type A war	veforms (WFT =	0):					
	000 = Interna 001 = Interna 010 = Interna 011 = Interna 100 = Interna 110 = Interna 111 = Interna	I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference	e Ladder is alv e Ladder is in ' e Ladder is in '	vays in 'B' Powe A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode	er mode for 1 clock and for 2 clocks and for 3 clocks and for 4 clocks and for 5 clocks and for 6 clocks and for 7 clocks and	I 'B' Power mod d 'B' Power mod	e for 15 clocks e for 14 clocks e for 13 clocks e for 12 clocks e for 11 clocks e for 10 clocks de for 9 clocks	
	For type B waveforms (WFT = 1):							
	000 = Internal 001 = Interna 010 = Interna 011 = Interna 100 = Interna 110 = Interna 111 = Interna	I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference I LCD Reference	e Ladder is alw e Ladder is in ' e Ladder is in '	vays in 'B' Powe A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode A' Power mode	er mode. for 1 clock and for 2 clocks and for 3 clocks and for 4 clocks and for 5 clocks and for 6 clocks and for 7 clocks and	I 'B' Power mode d 'B' Power mod d 'B' Power mod	e for 31 clocks e for 30 clocks e for 29 clocks e for 28 clocks e for 27 clocks e for 26 clocks e for 25 clocks	

REGISTER 27-7: LCDRL: LCD REFERENCE LADDER CONTROL REGISTERS



TABLE 30-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽²⁾	±2% ±3%		16.0 16.0	—	MHz MHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq +60^{\circ}C, \ VDD \geq 2.5V \\ 60^{\circ}C \leq TA \leq 85^{\circ}C, \ VDD \geq 2.5V \end{array}$
			±5%	_	16.0	—	MHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OS08A	MFosc	Internal Calibrated MFINTOSC Frequency ⁽²⁾	±2% ±3%	_	500 500	_	kHz kHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq +60^{\circ}C, \ VDD \geq 2.5V \\ 60^{\circ}C \leq TA \leq 85^{\circ}C, \ VDD \geq 2.5V \end{array}$
			±5%	_	500	—	kHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OS09	LFosc	Internal LFINTOSC Frequency	—	_	31	-	kHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	_	_	3.2	8	μS	
		MEINTOSC Wake-up from Sleep Start-up Time	—	—	24	35	μS	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

3: By design.

TABLE 30-3: PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.7V TO 5.5V)

Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4	_	8	MHz	
F11	Fsys	On-Chip VCO System Frequency	16		32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	_		2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	_	+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES			
Dimensio	n Limits	MIN	NOM	MAX		
Number of Pins	Ν		40			
Pitch	е	.100 BSC				
Top to Seating Plane	А	-	-	.250		
Molded Package Thickness	A2	.125	-	.195		
Base to Seating Plane	A1	.015	-	-		
Shoulder to Shoulder Width	E	.590	-	.625		
Molded Package Width	E1	.485	-	.580		
Overall Length	D	1.980	-	2.095		
Tip to Seating Plane	L	.115	-	.200		
Lead Thickness	с	.008	-	.015		
Upper Lead Width	b1	.030	-	.070		
Lower Lead Width	b	.014	-	.023		
Overall Row Spacing §	eB	-	-	.700		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B



For the most current package drawings, please see the Microchip Packaging Specification located at

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

	MILLIMETERS					
Dimensio	n Limits	MIN	NOM	MAX		
Number of Pins	Ν	28				
Pitch	e 0.65 BSC					
Overall Height	А	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint	L1	1.25 REF				
Lead Thickness	с	0.09	-	0.25		
Foot Angle	¢	0°	4°	8°		
Lead Width	b	0.22	_	0.38		

Notes:

Note:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B