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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1936-i-so

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NOTES:

REGISTER 12-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	Unimplemented: Read as '0'.
bit 6	CCP3SEL: CCP3 Input/Output Pin Selection bit <u>For 28-Pin Devices (PIC16F1936):</u> 0 = CCP3/P3A function is on RC6/TX/CK/CCP3/P3A/SEG9 1 = CCP3/P3A function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1 <u>For 40-Pin Devices (PIC16F1934/7):</u> 0 = CCP3/P3A function is on RE0/AN5/CCP3/P3A/SEG21 1 = CCP3/P3A function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1
bit 5	T1GSEL: Timer1 Gate Input Pin Selection bit 0 = T1G function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1 1 = T1G function is on RC4/SDI/SDA/T1G/SEG11
bit 4	P2BSEL: CCP2 PWM B Output Pin Selection bit <u>For 28-Pin Devices (PIC16F1936):</u> 0 = P2B function is on RC0/T1OSO/T1CKI/P2B 1 = P2B function is on RB5/AN13/P2B/CPS5/T1G/COM1 <u>For 40-Pin Devices (PIC16F1934/7):</u> 0 = P2B function is on RC0/T1OSO/T1CKI/P2B 1 = P2B function is on RD2/CPS10/P2B
bit 3	SRNQSEL: SR Latch nQ Output Pin Selection bit 0 = SRnQ function is on RA5/AN4/C2OUT/SRnQ/ \overline{SS} /CPS7/SEG5/VCAP 1 = SRnQ function is on RA0/AN0/C12IN0-/C2OUT/SRnQ/ \overline{SS} /SEG12/VCAP
bit 2	C2OUTSEL: Comparator C2 Output Pin Selection bit 0 = C2OUT function is on RA5/AN4/C2OUT/SRnQ/ \overline{SS} /CPS7/SEG5/VCAP 1 = C2OUT function is on RA0/AN0/C12IN0-/C2OUT/SRnQ/ \overline{SS} /SEG12/VCAP
bit 1	SSSEL: \overline{SS} Input Pin Selection bit 0 = \overline{SS} function is on RA5/AN4/C2OUT/SRnQ/ \overline{SS} /CPS7/SEG5/VCAP 1 = \overline{SS} function is on RA0/AN0/C12IN0-/C2OUT/SRnQ/ \overline{SS} /SEG12/VCAP
bit 0	CCP2SEL: CCP2 Input/Output Pin Selection bit 0 = CCP2/P2A function is on RC1/T1OSI/CCP2/P2A 1 = CCP2/P2A function is on RB3/AN9/C12IN2-/CPS3/CCP2/P2A/VLCD3

REGISTER 12-14: PORTD: PORTD REGISTER⁽¹⁾

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **RD<7:0>**: PORTD General Purpose I/O Pin bits
 1 = Port pin is > V_{IH}
 0 = Port pin is < V_{IL}

Note 1: PORTD is not implemented on PIC16(L)F1936 devices, read as '0'.

REGISTER 12-15: TRISD: PORTD TRI-STATE REGISTER⁽¹⁾

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **TRISD<7:0>**: PORTD Tri-State Control bits
 1 = PORTD pin configured as an input (tri-stated)
 0 = PORTD pin configured as an output

Note 1: TRISD is not implemented on PIC16(L)F1936 devices, read as '0'.

2: PORTD implemented on PIC16(L)F1934/7 devices only.

REGISTER 12-16: LATD: PORTD DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **LATD<7:0>**: PORTD Output Latch Value bits^(1,2)

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

2: PORTD implemented on PIC16(L)F1934/7 devices only.

NOTES:

17.4 Low-Power Voltage State

In order for the DAC module to consume the least amount of power, one of the two voltage reference input sources to the resistor ladder must be disconnected. Either the positive voltage source, (VSOURCE+), or the negative voltage source, (VSOURCE-) can be disabled.

The negative voltage source is disabled by setting the DACLPS bit in the DACCON0 register. Clearing the DACLPS bit in the DACCON0 register disables the positive voltage source.

17.4.1 OUTPUT CLAMPED TO POSITIVE VOLTAGE SOURCE

The DAC output voltage can be set to VSOURCE+ with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the DACCON0 register.
- Setting the DACLPS bit in the DACCON0 register.
- Configuring the DACPSS bits to the proper positive source.
- Configuring the DACR<4:0> bits to '11111' in the DACCON1 register.

This is also the method used to output the voltage level from the FVR to an output pin. See **Section 17.5 “Operation During Sleep”** for more information.

Reference Figure 17-3 for output clamping examples.

17.4.2 OUTPUT CLAMPED TO NEGATIVE VOLTAGE SOURCE

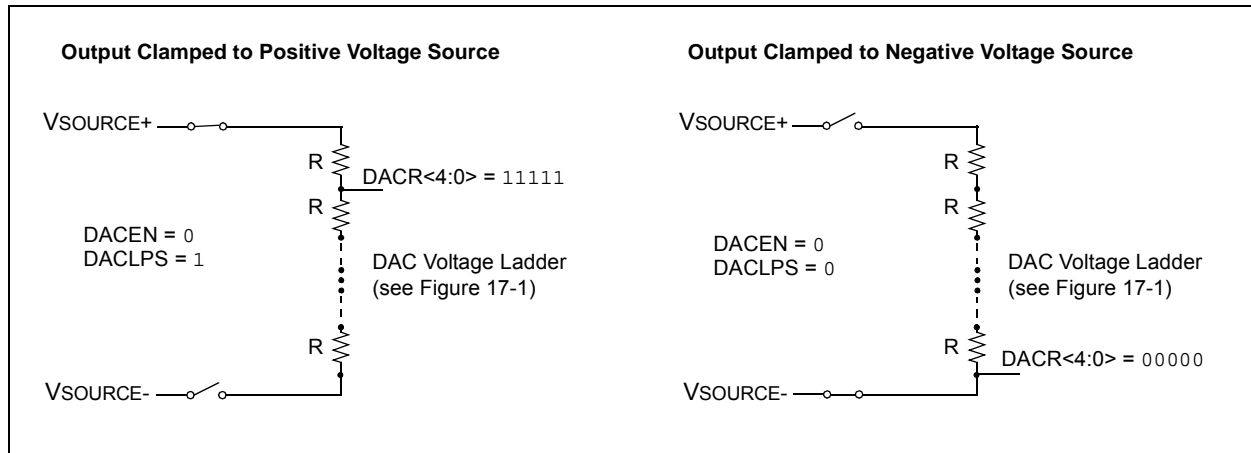
The DAC output voltage can be set to VSOURCE- with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the DACCON0 register.
- Clearing the DACLPS bit in the DACCON0 register.
- Configuring the DACNSS bits to the proper negative source.
- Configuring the DACR<4:0> bits to '00000' in the DACCON1 register.

This allows the comparator to detect a zero-crossing while not consuming additional current through the DAC module.

Reference Figure 17-3 for output clamping examples.

FIGURE 17-3: OUTPUT VOLTAGE CLAMPING EXAMPLES



17.5 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DACCON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

17.6 Effects of a Reset

A device Reset affects the following:

- DAC is disabled.
- DAC output voltage is removed from the DACOUT pin.
- The DACR<4:0> range select bits are cleared.

23.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PRx register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2/4/6:
 - Select the Timer2/4/6 resource to be used for PWM generation by setting the CxTSEL<1:0> bits in the CCPTMRSx register.
 - Clear the TMRxIF interrupt flag bit of the PIRx register. See Note below.
 - Configure the TxCKPS bits of the TxCON register with the Timer prescale value.
 - Enable the Timer by setting the TMRxON bit of the TxCON register.
6. Enable PWM output pin:
 - Wait until the Timer overflows and the TMRxIF bit of the PIRx register is set. See Note below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

23.3.3 TIMER2/4/6 TIMER RESOURCE

The PWM standard mode makes use of one of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

Configuring the CxTSEL<1:0> bits in the CCPTMRSx register selects which Timer2/4/6 timer is used.

23.3.4 PWM PERIOD

The PWM period is specified by the PRx register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 23-1.

EQUATION 23-1: PWM PERIOD

$$PWM\ Period = [(PRx) + 1] \cdot 4 \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

Note 1: $TOSC = 1/FOSC$

When TMRx is equal to PRx, the following three events occur on the next increment cycle:

- TMRx is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see **Section 22.1 “Timer2/4/6 Operation”**) is not used in the determination of the PWM frequency.

23.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSBs and the DCxB<1:0> bits of the CCPxCON register contain the two LSBs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PRx and TMRx registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 23-2 is used to calculate the PWM pulse width.

Equation 23-3 is used to calculate the PWM duty cycle ratio.

EQUATION 23-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

EQUATION 23-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PRx + 1)}$$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMRx register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 23-4).

TABLE 23-9: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	PxM<1:0>	CCPx/PxA	PxB	PxC	PxD
Single	00	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: PWM Steering enables outputs in Single mode.

FIGURE 23-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

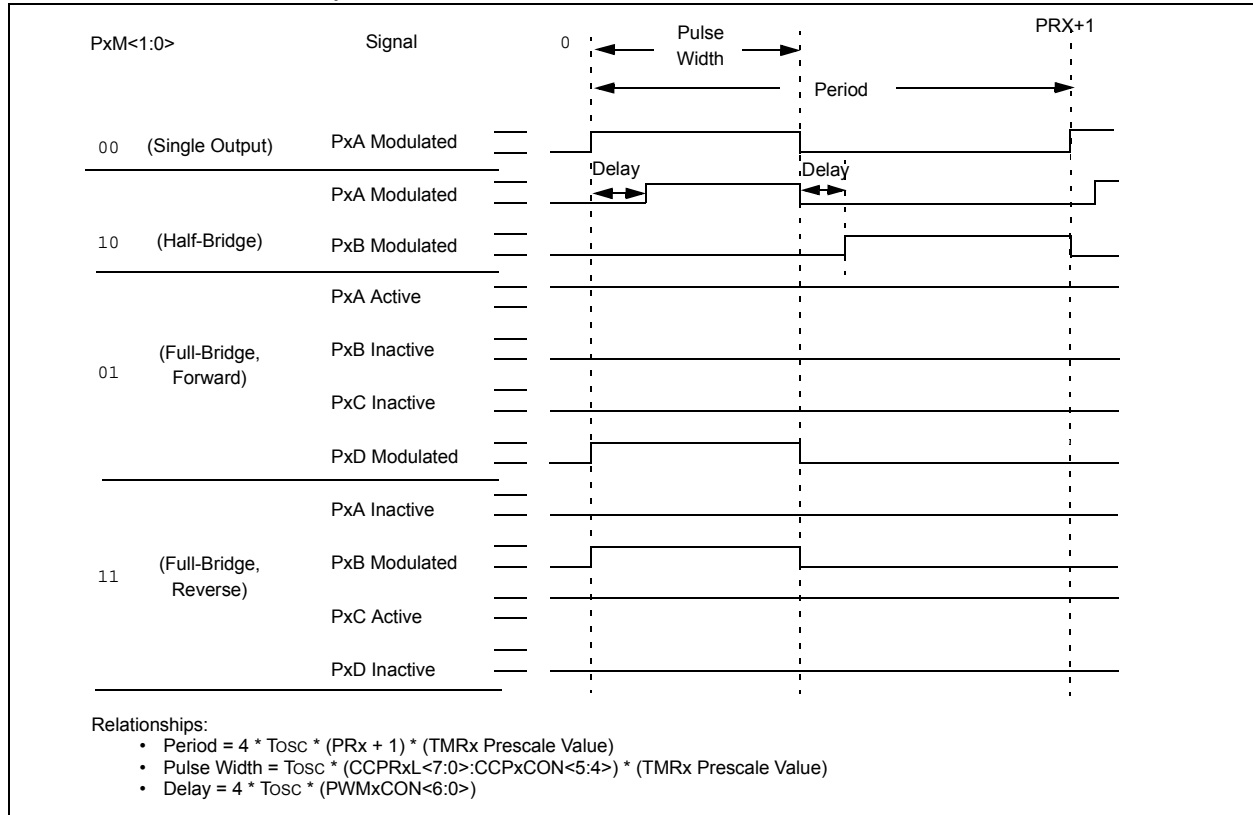
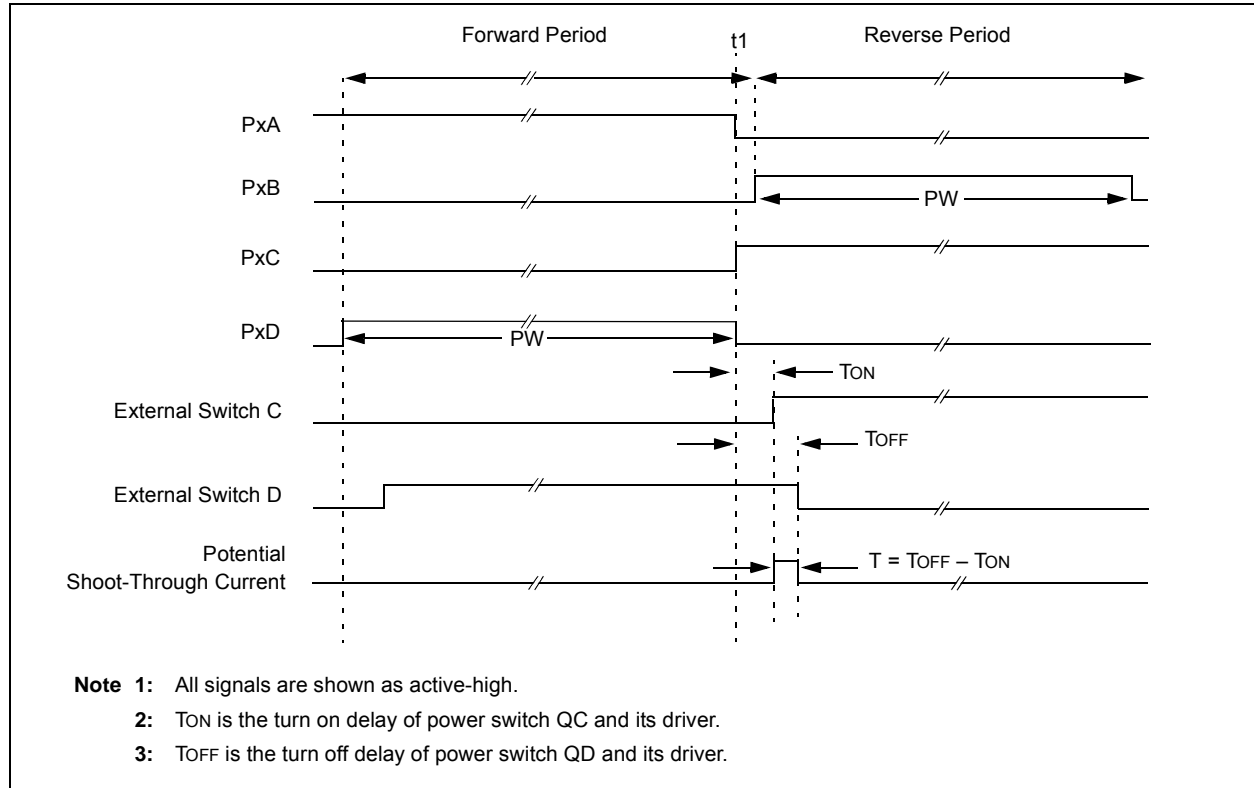


FIGURE 23-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



REGISTER 23-2: CCPTMRS0: PWM TIMER SELECTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-6 **C4TSEL<1:0>**: CCP4 Timer Selection bits
 00 = CCP4 is based off Timer2 in PWM mode
 01 = CCP4 is based off Timer4 in PWM mode
 10 = CCP4 is based off Timer6 in PWM mode
 11 = Reserved
- bit 5-4 **C3TSEL<1:0>**: CCP3 Timer Selection bits
 00 = CCP3 is based off Timer2 in PWM mode
 01 = CCP3 is based off Timer4 in PWM mode
 10 = CCP3 is based off Timer6 in PWM mode
 11 = Reserved
- bit 3-2 **C2TSEL<1:0>**: CCP2 Timer Selection bits
 00 = CCP2 is based off Timer2 in PWM mode
 01 = CCP2 is based off Timer4 in PWM mode
 10 = CCP2 is based off Timer6 in PWM mode
 11 = Reserved
- bit 1-0 **C1TSEL<1:0>**: CCP1 Timer Selection bits
 00 = CCP1 is based off Timer2 in PWM mode
 01 = CCP1 is based off Timer4 in PWM mode
 10 = CCP1 is based off Timer6 in PWM mode
 11 = Reserved

REGISTER 23-3: CCPTMRS1: PWM TIMER SELECTION CONTROL REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	—	—	—	—	C5TSEL<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-2 **Unimplemented**: Read as '0'
- bit 1-0 **C5TSEL<1:0>**: CCP5 Timer Selection bits
 00 = CCP5 is based off Timer2 in PWM mode
 01 = CCP5 is based off Timer4 in PWM mode
 10 = CCP5 is based off Timer6 in PWM mode
 11 = Reserved

24.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I²C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ($\overline{\text{ACK}}$) is an active-low signal, pulling the SDA line low indicated to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an $\overline{\text{ACK}}$ is placed in the ACKSTAT bit of the SSPCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the $\overline{\text{ACK}}$ value sent back to the transmitter. The ACKDT bit of the SSPCON2 register is set/cleared to determine the response.

Slave hardware will generate an $\overline{\text{ACK}}$ response if the AHEN and DHEN bits of the SSPCON3 register are clear.

There are certain conditions where an $\overline{\text{ACK}}$ will not be sent by the slave. If the BF bit of the SSPSTAT register or the SSPOV bit of the SSPCON1 register are set when a byte is received.

When the module is addressed, after the 8th falling edge of SCL on the bus, the ACKTIM bit of the SSPCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

24.5 I²C Slave Mode Operation

The MSSP Slave mode operates in one of four modes selected in the SSPM bits of SSPCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operated the same as the other modes with SSPIF additionally getting set upon detection of a Start, Restart, or Stop condition.

24.5.1 SLAVE MODE ADDRESSES

The SSPADD register (Register 24-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPBUF register and an interrupt is generated. If the value does not match, the module goes Idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 24-5) affects the address matching process. See **Section 24.5.9 “SSP Mask Register”** for more information.

24.5.1.1 I²C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

24.5.1.2 I²C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSb of the 10-bit address and stored in bits 2 and 1 of the SSPADD register.

After the acknowledge of the high byte the UA bit is set and SCL is held low until the user updates SSPADD with the low address. The low address byte is clocked in and all 8 bits are compared to the low address value in SSPADD. Even if there is not an address match; SSPIF and UA are set, and SCL is held low until SSPADD is updated to receive a high byte again. When SSPADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

24.6.4 I²C MASTER MODE START CONDITION TIMING

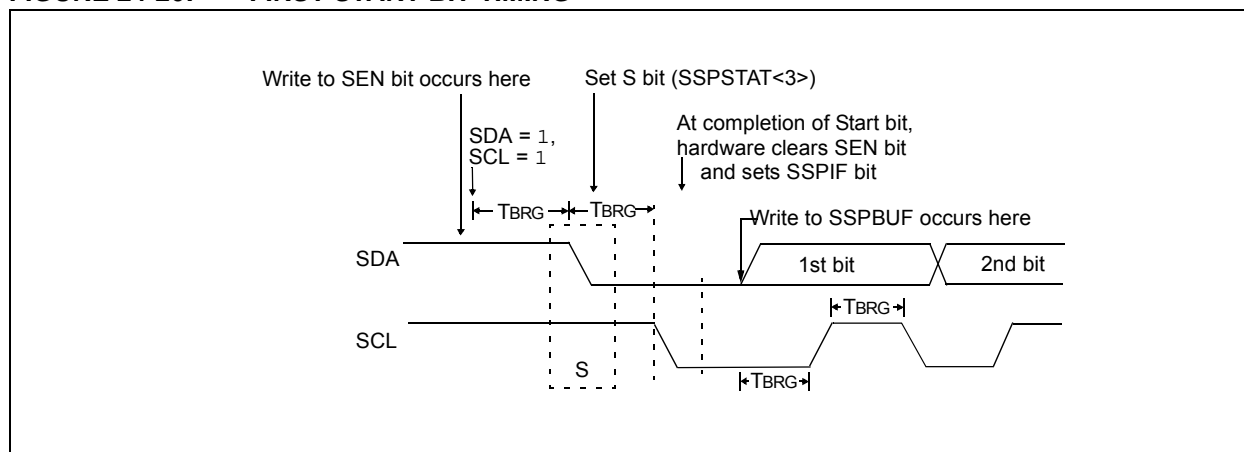
To initiate a Start condition, the user sets the Start Enable bit, SEN bit of the SSPCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit of the SSPSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPCON2 reg-

ister will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note 1: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

2: The Philips I²C specification states that a bus collision cannot occur on a Start.

FIGURE 24-26: FIRST START BIT TIMING



24.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

Note: The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

24.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

24.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

24.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

24.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSPIF is set by hardware on completion of the Start.
3. SSPIF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/W bit set.
5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the $\overline{\text{ACK}}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
8. User sets the RCEN bit of the SSPCON2 register and the Master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSPIF and BF are set.
10. Master clears SSPIF and reads the received byte from SSPBUF, clears BF.
11. Master sets $\overline{\text{ACK}}$ value sent to slave in ACKDT bit of the SSPCON2 register and initiates the $\overline{\text{ACK}}$ by setting the ACKEN bit.
12. Masters $\overline{\text{ACK}}$ is clocked out to the Slave and SSPIF is set.
13. User clears SSPIF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. Master sends a not $\overline{\text{ACK}}$ or Stop to end communication.

PIC16(L)F1934/6/7

REGISTER 24-5: SSPMSK: SSP MASK REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
MSK<7:0>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-1 **MSK<7:1>**: Mask bits
1 = The received address bit n is compared to SSPADD<n> to detect I²C address match
0 = The received address bit n is not used to detect I²C address match
- bit 0 **MSK<0>**: Mask bit for I²C Slave mode, 10-bit Address
I²C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):
1 = The received address bit 0 is compared to SSPADD<0> to detect I²C address match
0 = The received address bit 0 is not used to detect I²C address match
I²C Slave mode, 7-bit address, the bit is ignored

REGISTER 24-6: SSPADD: MSSP ADDRESS AND BAUD RATE REGISTER (I²C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ADD<7:0>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

Master mode:

- bit 7-0 **ADD<7:0>**: Baud Rate Clock Divider bits
SCL pin clock period = ((ADD<7:0> + 1) * 4) / Fosc

10-Bit Slave mode — Most Significant Address byte:

- bit 7-3 **Not used**: Unused for Most Significant Address byte. Bit state of this register is a “don't care”. Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.
- bit 2-1 **ADD<2:1>**: Two Most Significant bits of 10-bit address
- bit 0 **Not used**: Unused in this mode. Bit state is a “don't care”.

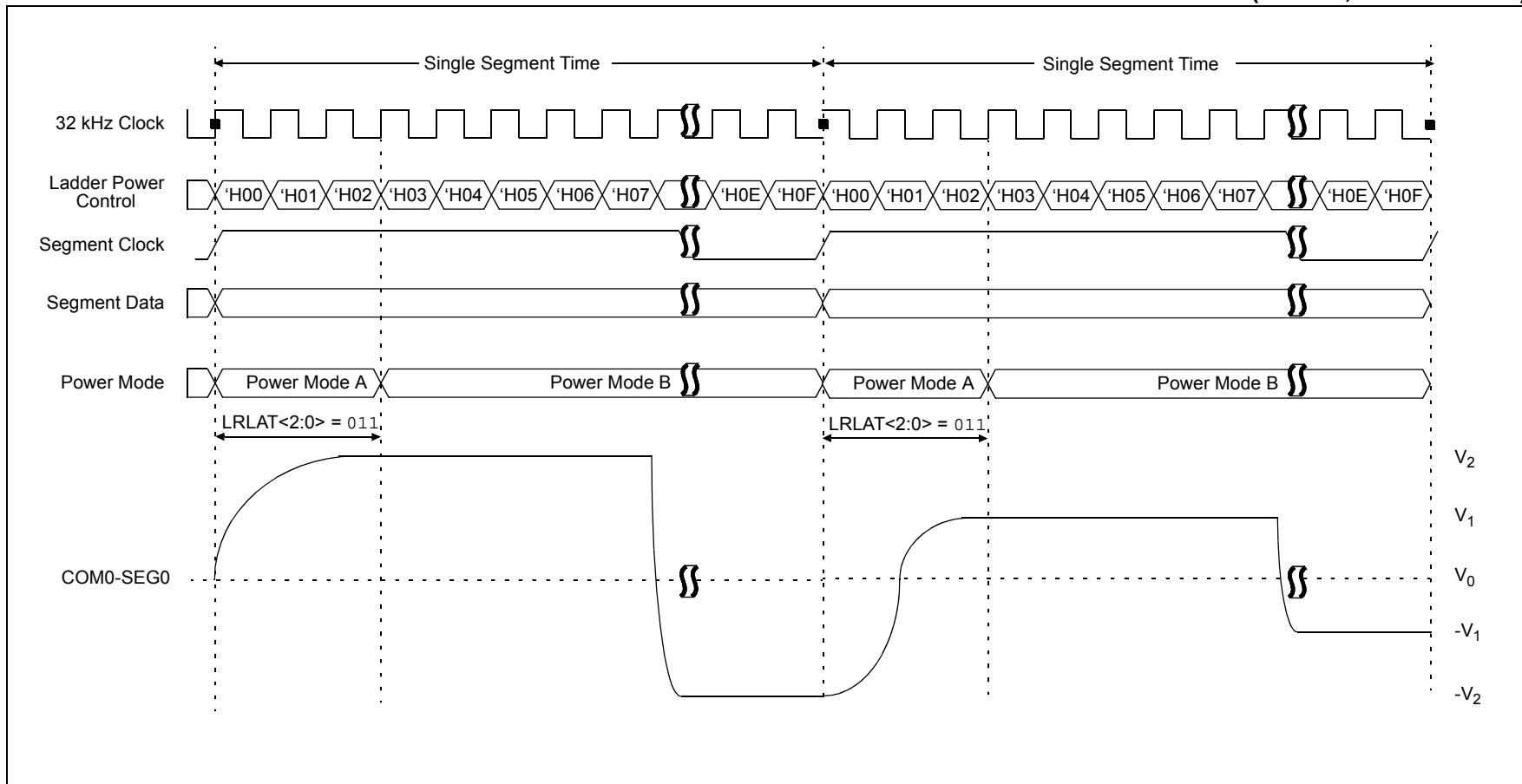
10-Bit Slave mode — Least Significant Address byte:

- bit 7-0 **ADD<7:0>**: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

- bit 7-1 **ADD<7:1>**: 7-bit address
- bit 0 **Not used**: Unused in this mode. Bit state is a “don't care”.

FIGURE 27-5: LCD INTERNAL REFERENCE LADDER POWER MODE SWITCHING DIAGRAM – TYPE A WAVEFORM (1/2 MUX, 1/2 BIAS DRIVE)



PIC16(L)F1934/6/7

BCF	Bit Clear f
Syntax:	[<i>label</i>] BCF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[<i>label</i>] BTFSC f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f < b >) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BRA	Relative Branch
Syntax:	[<i>label</i>] BRA label [<i>label</i>] BRA \$+k
Operands:	$-256 \leq \text{label} - \text{PC} + 1 \leq 255$ $-256 \leq k \leq 255$
Operation:	$(\text{PC}) + 1 + k \rightarrow \text{PC}$
Status Affected:	None
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $\text{PC} + 1 + k$. This instruction is a two-cycle instruction. This branch has a limited range.

BTFSS	Bit Test f, Skip if Set
Syntax:	[<i>label</i>] BTFSS f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$
Operation:	skip if $(f < b >) = 1$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

BRW	Relative Branch with W
Syntax:	[<i>label</i>] BRW
Operands:	None
Operation:	$(\text{PC}) + (W) \rightarrow \text{PC}$
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $\text{PC} + 1 + (W)$. This instruction is a two-cycle instruction.

BSF	Bit Set f
Syntax:	[<i>label</i>] BSF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

PIC16(L)F1934/6/7

FIGURE 30-12: PIC16(L)F1934/6/7 A/D CONVERSION TIMING (NORMAL MODE)

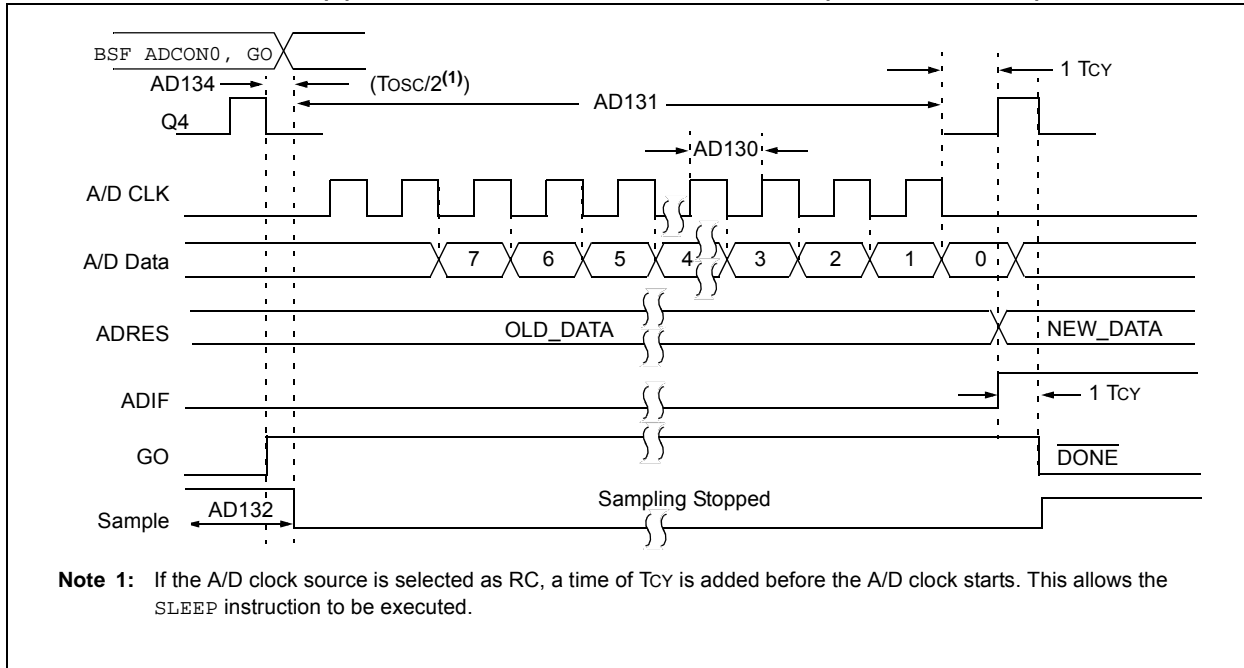


FIGURE 30-13: PIC16(L)F1934/6/7 A/D CONVERSION TIMING (SLEEP MODE)

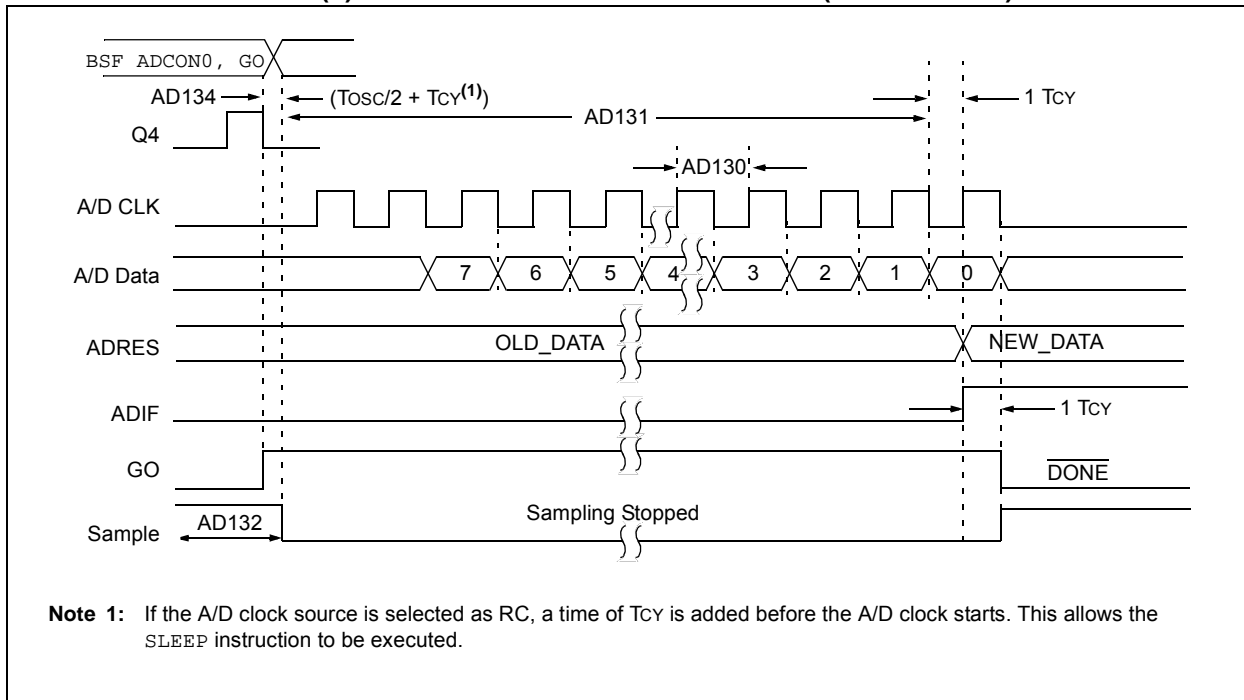


FIGURE 30-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

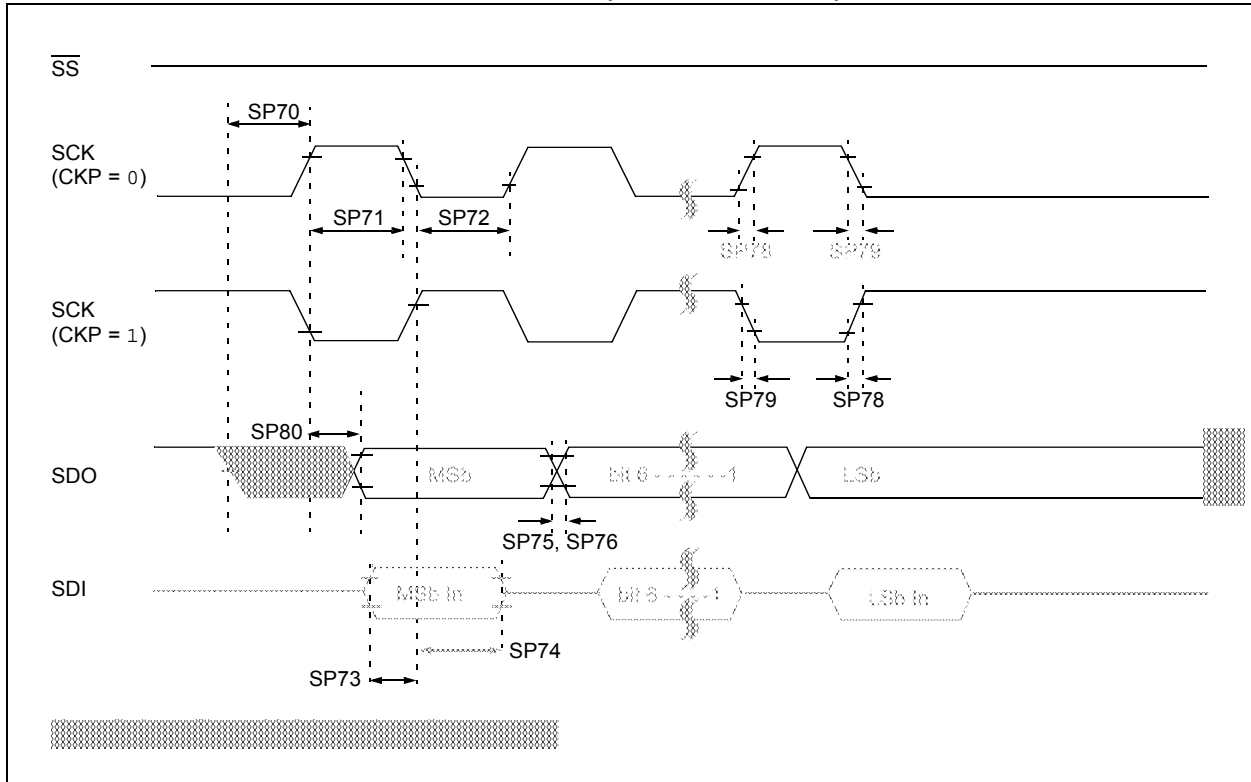
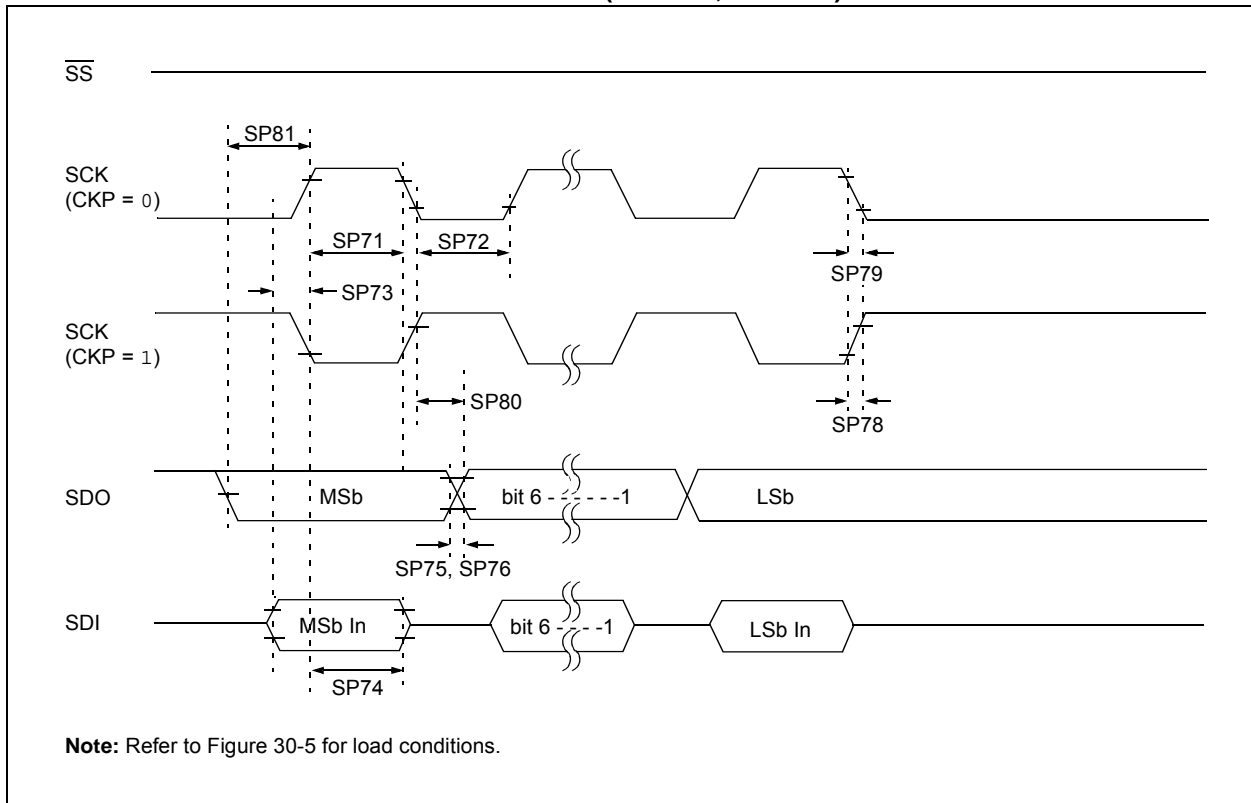


FIGURE 30-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



PIC16(L)F1934/6/7

FIGURE 31-46: PIC16LF1937 HF INTOSC

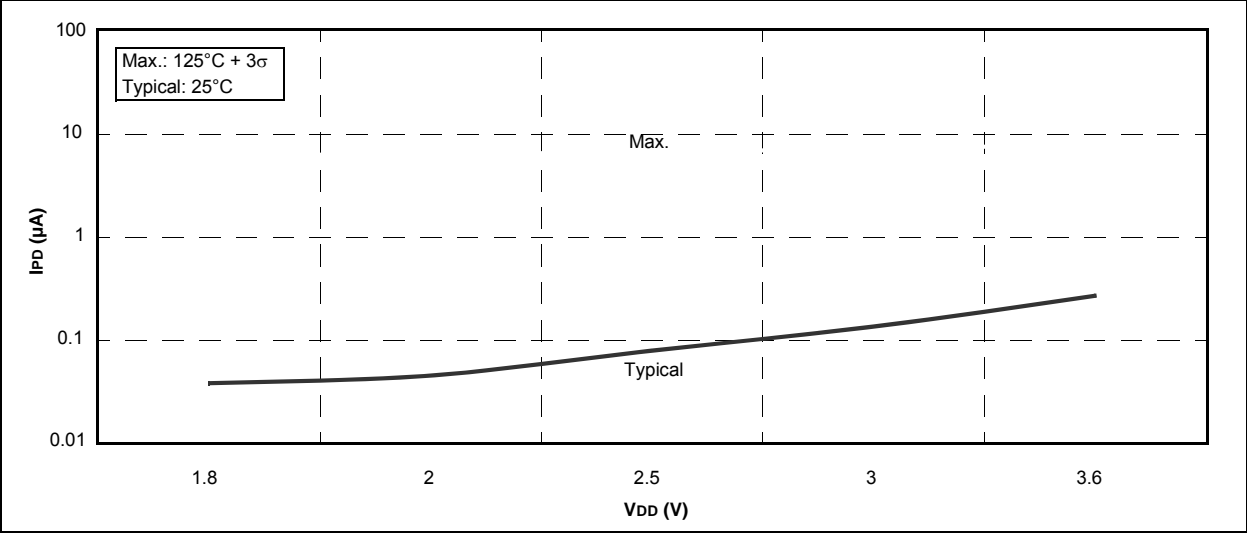


FIGURE 31-47: PIC16F1937 HF INTOSC

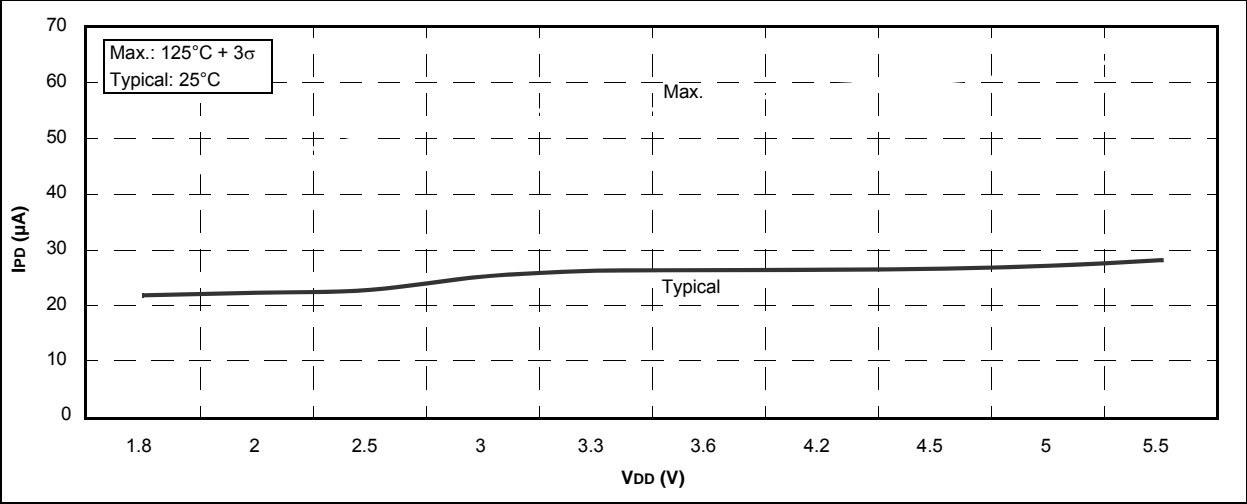
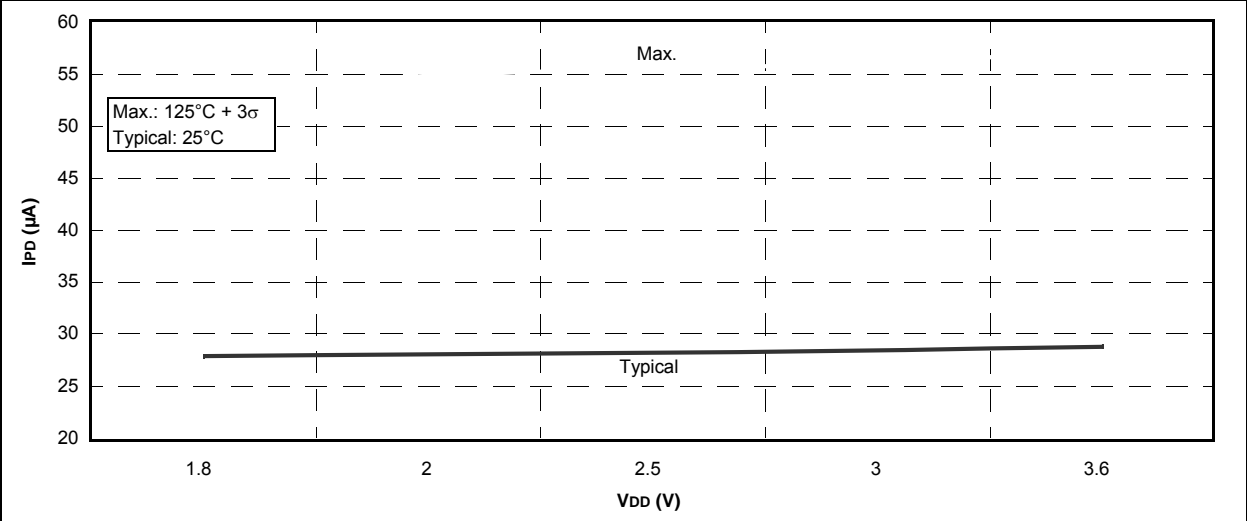


FIGURE 31-48: PIC16LF1937 COMPARATOR 1, HIGH POWER



APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2008)

Original release

Revision B (04/2009)

Revised data sheet title; Revised Features section.

Revision C (10/2009)

Added PIC16L/LF1933/34. General updates.

Revision D (12/2009)

General updates.

Revision E (5/2011)

Separated 193X data sheet into three separate data sheets. Added Characterization Data.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC® devices to the PIC16(L)F1934/6/7 family of devices.

B.1 PIC16F917 to PIC16F1937

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F917	PIC16F1937
Max. Operating Speed	20 MHz	32 MHz
Max. Program Memory (Words)	8K	8K
Max. SRAM (Bytes)	368	512
A/D Resolution	10-bit	10-bit
Timers (8/16-bit)	2/1	4/1
Oscillator Modes	4	8
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	RB<7:0>
Interrupt-on-change	RB<7:4>	RB<7:0>
Comparator	2	2
AUSART/EUSART	1/0	0/1
Extended WDT	Y	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	30 kHz - 8 MHz	500 kHz - 32 MHz
Clock Switching	Y	Y
Capacitive Sensing	N	Y
CCP/ECCP	2/0	2/3
Enhanced PIC16 CPU	N	Y
MSSP/SSP	0/1	1/0
LCD	Y	Y