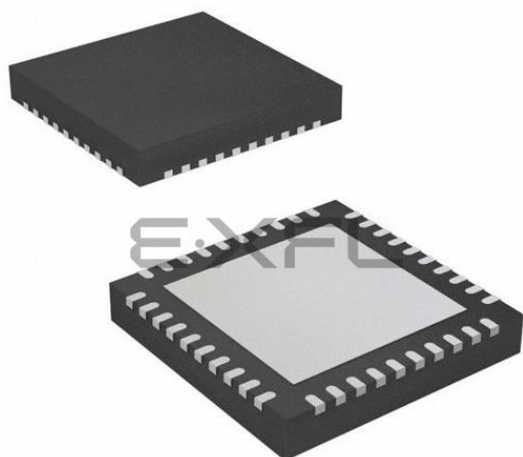




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1937-i-mv

PIC16(L)F1934/6/7

TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/OSC2/CLKOUT/VCAP ⁽²⁾ /SEG1	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	Fosc/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1934/6/7 only).
	SEG1	—	AN	LCD Analog output.
RA7/OSC1/CLKIN/SEG2	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG2	—	AN	LCD Analog output.
RB0/AN12/CPS0/CCP4/SRI/INT/SEG0	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
	SRI	—	ST	SR Latch input.
	INT	ST	—	External interrupt.
	SEG0	—	AN	LCD analog output.
RB1/AN10/C12IN3-/CPS1/P1C/VLCD1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	CPS1	AN	—	Capacitive sensing input 1.
	P1C	—	CMOS	PWM output.
	VLCD1	AN	—	LCD analog input.
RB2/AN8/CPS2/P1B/VLCD2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
	P1B	—	CMOS	PWM output.
	VLCD2	AN	—	LCD analog input.
RB3/AN9/C12IN2-/CPS3/CCP2 ⁽⁴⁾ /P2A ⁽⁴⁾ /VLCD3	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
	VLCD3	AN	—	LCD analog input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C™ = Schmitt Trigger input with I²C levels
HV = High Voltage XTAL = Crystal

- Note** 1: Pin function is selectable via the APFCON register.
2: PIC16F1934/6/7 devices only.
3: PIC16(L)F1936 devices only.
4: PORTD is available on PIC16(L)F1934/7 devices only.
5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

PIC16(L)F1934/6/7

TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/SDI/SDA/T1G ⁽¹⁾ /SEG11	RC4	ST	CMOS	General purpose I/O.
	SDI	ST	—	SPI data input.
	SDA	I ² C	OD	I ² C™ data input/output.
	T1G	ST	—	Timer1 Gate input.
	SEG11	—	AN	LCD Analog output.
RC5/SDO/SEG10	RC5	ST	CMOS	General purpose I/O.
	SDO	—	CMOS	SPI data output.
	SEG10	—	AN	LCD Analog output.
RC6/TX/CK/CCP3/P3A/SEG9	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	P3A	—	CMOS	PWM output.
	SEG9	—	AN	LCD Analog output.
RC7/RX/DT/P3B/SEG8	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	P3B	—	CMOS	PWM output.
	SEG8	—	AN	LCD Analog output.
RD0 ⁽⁴⁾ /CPS8/COM3	RD0	ST	CMOS	General purpose I/O.
	CPS8	AN	—	Capacitive sensing input 8.
	COM3	—	AN	LCD analog output.
RD1 ⁽⁴⁾ /CPS9/CCP4	RD1	ST	CMOS	General purpose I/O.
	CPS9	AN	—	Capacitive sensing input 9.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
RD2 ⁽⁴⁾ /CPS10/P2B	RD2	ST	CMOS	General purpose I/O.
	CPS10	AN	—	Capacitive sensing input 10.
	P2B	—	CMOS	PWM output.
RD3 ⁽⁴⁾ /CPS11/P2C/SEG16	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
	P2C	—	CMOS	PWM output.
	SEG16	—	AN	LCD analog output.
RD4 ⁽⁴⁾ /CPS12/P2D/SEG17	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
	P2D	—	CMOS	PWM output.
	SEG17	—	AN	LCD analog output.
RD5 ⁽⁴⁾ /CPS13/P1B/SEG18	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
	P1D	—	CMOS	PWM output.
	SEG18	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C™ = Schmitt Trigger input with I²C levels
HV = High Voltage XTAL = Crystal

- Note** 1: Pin function is selectable via the APFCON register.
2: PIC16F1934/6/7 devices only.
3: PIC16(L)F1936 devices only.
4: PORTD is available on PIC16(L)F1934/7 devices only.
5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD6 ⁽⁴⁾ /CPS14/P1C/SEG19	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
	P1C	—	CMOS	PWM output.
	SEG19	—	AN	LCD analog output.
RD7 ⁽⁴⁾ /CPS15/P1D/SEG20	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
	P1D	—	CMOS	PWM output.
	SEG20	—	AN	LCD analog output.
RE0 ⁽⁵⁾ /AN5/P3A ⁽¹⁾ /CCP3 ⁽¹⁾ /SEG21	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	P3A	—	CMOS	PWM output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SEG21	—	AN	LCD analog output.
RE1 ⁽⁵⁾ /AN6/P3B/SEG22	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	P3B	—	CMOS	PWM output.
	SEG22	—	AN	LCD analog output.
RE2 ⁽⁵⁾ /AN7/CCP5/SEG23	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG23	—	AN	LCD analog output.
RE3/MCLR/VPP	RE3	TTL	—	General purpose input.
	MCLR	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C™ = Schmitt Trigger input with I²C levels
HV = High Voltage XTAL = Crystal

- Note** 1: Pin function is selectable via the APFCON register.
2: PIC16F1934/6/7 devices only.
3: PIC16(L)F1936 devices only.
4: PORTD is available on PIC16(L)F1934/7 devices only.
5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

PIC16(L)F1934/6/7

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets	
Bank 2												
100h ⁽²⁾	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
101h ⁽²⁾	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
102h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000	
103h ⁽²⁾	STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	---1 1000	---q quuu	
104h ⁽²⁾	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu	
105h ⁽²⁾	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000	
106h ⁽²⁾	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu	
107h ⁽²⁾	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000	
108h ⁽²⁾	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000	
109h ⁽²⁾	WREG	Working Register								0000 0000	uuuu uuuu	
10Ah ^(1, 2)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000
10Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCF	0000 0000	0000 0000	
10Ch	LATA	PORTA Data Latch								xxxx xxxx	uuuu uuuu	
10Dh	LATB	PORTB Data Latch								xxxx xxxx	uuuu uuuu	
10Eh	LATC	PORTC Data Latch								xxxx xxxx	uuuu uuuu	
10Fh ⁽³⁾	LATD	PORTD Data Latch								xxxx xxxx	uuuu uuuu	
110h	LATE	—	—	—	—	—	LATE2 ⁽³⁾	LATE1 ⁽³⁾	LATE0 ⁽³⁾	---- -xxx	---- -uuu	
111h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	0000 -100	0000 -100	
112h	CM1CON1	C1INTP	C1INTN	C1PCH1	C1PCH0	—	—	C1NCH<1:0>		0000 --00	0000 --00	
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	0000 -100	0000 -100	
114h	CM2CON1	C2INTP	C2INTN	C2PCH1	C2PCH0	—	—	C2NCH<1:0>		0000 --00	0000 --00	
115h	CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	---- --00	---- --00	
116h	BORCON	SBOREN	—	—	—	—	—	—	BORRDY	1--- ---q	u--- ---u	
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR<1:0>		0q00 0000	0q00 0000	
118h	DACCON0	DACEN	DACLPS	DACOE	---	DACPSS<1:0>		---	DACNSS	000- 00-0	000- 00-0	
119h	DACCON1	---	---	---	DACR<4:0>					---	0000	---0 0000
11Ah	SRCON0	SRLN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR	0000 0000	0000 0000	
11Bh	SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	0000 0000	0000 0000	
11Ch	—	Unimplemented								—	—	
11Dh	APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	-000 0000	-000 0000	
11Eh	—	Unimplemented								—	—	
11Fh	—	Unimplemented								—	—	

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** These registers can be addressed from any bank.
- 3:** These registers/bits are not implemented on PIC16(L)F1936 devices, read as '0'.
- 4:** Unimplemented, read as '1'.

6.11 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Reset Instruction Reset ($\overline{\text{RI}}$)
- Stack Overflow Reset (STKOVF)
- Stack Underflow Reset (STKUNF)
- MCLR Reset ($\overline{\text{RMCLR}}$)

The PCON register bits are shown in Register 6-2.

REGISTER 6-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	—	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:

HC = Bit is cleared by hardware

HS = Bit is set by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-m/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7	STKOVF: Stack Overflow Flag bit 1 = A Stack Overflow occurred 0 = A Stack Overflow has not occurred or set to '0' by firmware
bit 6	STKUNF: Stack Underflow Flag bit 1 = A Stack Underflow occurred 0 = A Stack Underflow has not occurred or set to '0' by firmware
bit 5-4	Unimplemented: Read as '0'
bit 3	$\overline{\text{RMCLR}}$: MCLR Reset Flag bit 1 = A $\overline{\text{MCLR}}$ Reset has not occurred or set to '1' by firmware 0 = A MCLR Reset has occurred (set to '0' in hardware when a $\overline{\text{MCLR}}$ Reset occurs)
bit 2	$\overline{\text{RI}}$: RESET Instruction Flag bit 1 = A RESET instruction has not been executed or set to '1' by firmware 0 = A RESET instruction has been executed (set to '0' in hardware upon executing a RESET instruction)
bit 1	$\overline{\text{POR}}$: Power-on Reset Status bit 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0	$\overline{\text{BOR}}$: Brown-out Reset Status bit 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	CHS<4:0>					GO/DONE	ADON	163
ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		164
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	134
APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	131
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	183
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	183
CM1CON1	C1NTP	C1INTN	C1PCH<1:0>		—	—	C1NCH<1:0>		184
CM2CON1	C2NTP	C2INTN	C2PCH<1:0>		—	—	C2NCH<1:0>		184
CPSCON0	CPSON	—	—	—	CPSRNG<1:0>		CPSOUT	T0XCS	323
CPSCON1	—	—	—	—	CPSCH<3:0>				324
DACCON0	DACEN	DACLPS	DACOE	---	DACPSS<1:0>		---	DACNSS	176
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	133
LCDCON	LCDEN	SLPEN	WERR	—	CS<1:0>		LMUX<1:0>		329
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	333
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	333
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			193
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	133
SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	189
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				287
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	133

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

TABLE 12-4: SUMMARY OF CONFIGURATION WORD WITH PORTA

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD	62
	7:0	CP	MCLRE	PWRT	WDTE<1:0>		FOSC<2:0>			
CONFIG2	13:8	—	—	LVP	DEBUG	—	BORV	STVREN	PLLEN	64
	7:0	—	—	VCAPEN<1:0> ⁽¹⁾		—	—	WRT<1:0>		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTA.

Note 1: PIC16F1934/6/7 only.

PIC16(L)F1934/6/7

REGISTER 12-11: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits

1 = Port pin is > V_{IH}

0 = Port pin is < V_{IL}

REGISTER 12-12: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **TRISC<7:0>**: PORTC Tri-State Control bits

1 = PORTC pin configured as an input (tri-stated)

0 = PORTC pin configured as an output

REGISTER 12-13: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **LATC<7:0>**: PORTC Output Latch Value bits⁽¹⁾

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

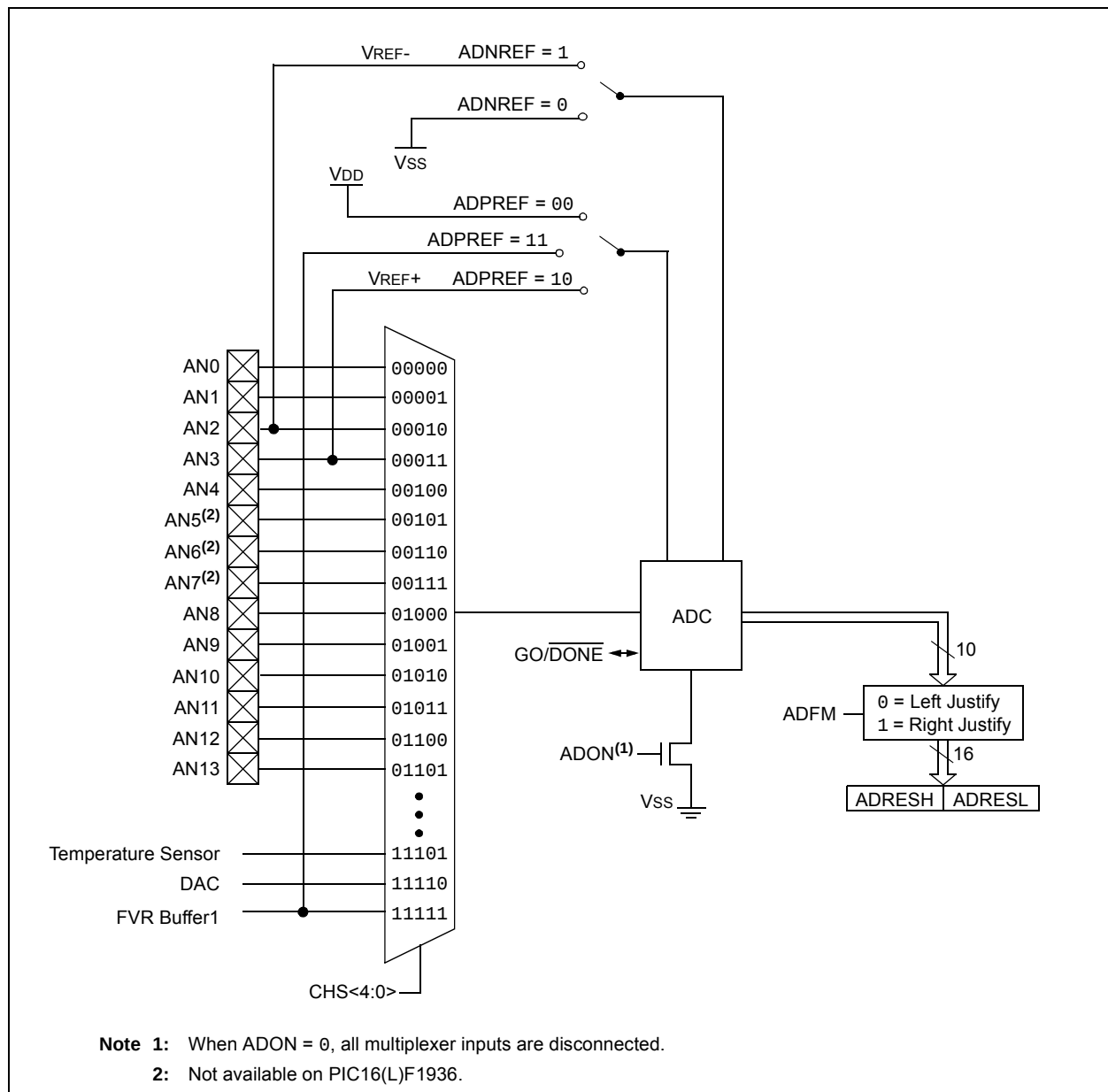
15.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 15-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

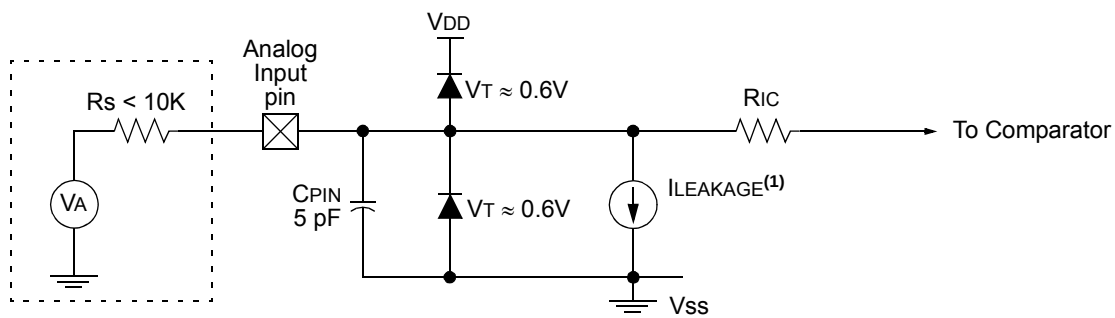
The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 15-1: ADC BLOCK DIAGRAM



PIC16(L)F1934/6/7

FIGURE 18-3: ANALOG INPUT MODEL

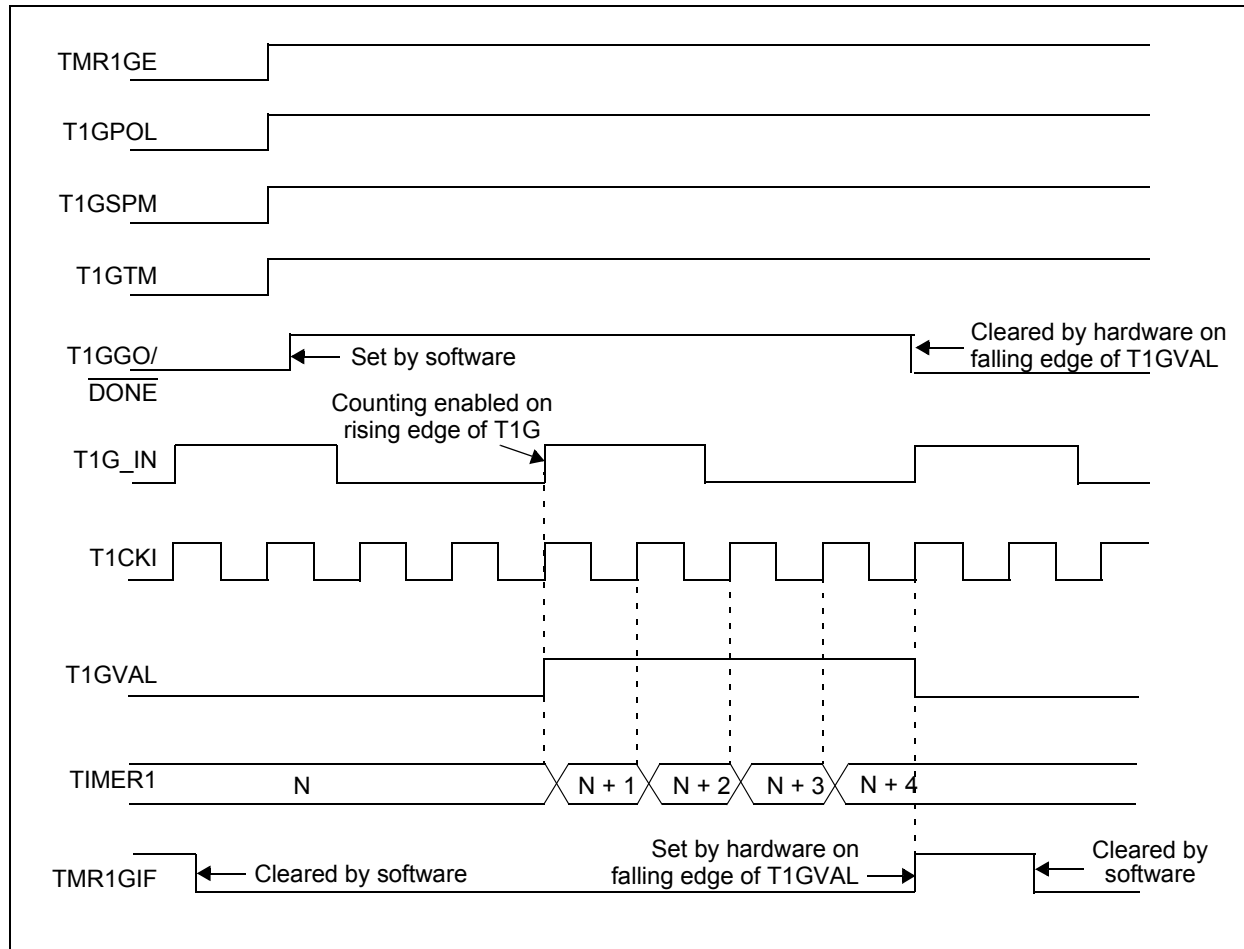


Legend: C_{PIN} = Input Capacitance
 $I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
 R_{IC} = Interconnect Resistance
 R_S = Source Impedance
 V_A = Analog Voltage
 V_T = Threshold Voltage

Note 1: See the applicable Electrical Specifications Chapter.

PIC16(L)F1934/6/7

FIGURE 21-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



PIC16(L)F1934/6/7

23.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PRx is 255. The resolution is a function of the PRx register value as shown by Equation 23-4.

EQUATION 23-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR_x + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 23-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 32 MHz)

PWM Frequency	1.95 kHz	7.81 kHz	31.25 kHz	125 kHz	250 kHz	333.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 23-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 23-7: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

TABLE 23-9: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	PxM<1:0>	CCPx/PxA	PxB	PxC	PxD
Single	00	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: PWM Steering enables outputs in Single mode.

FIGURE 23-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

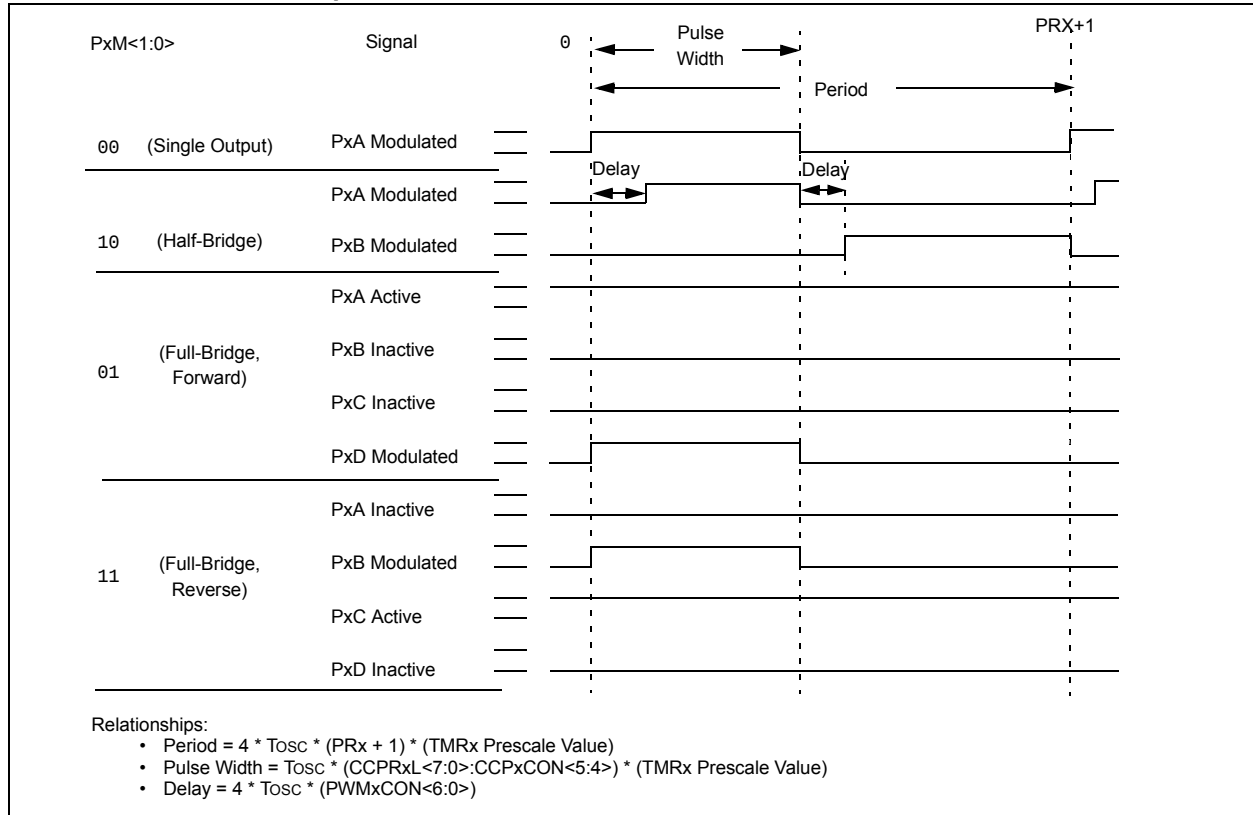
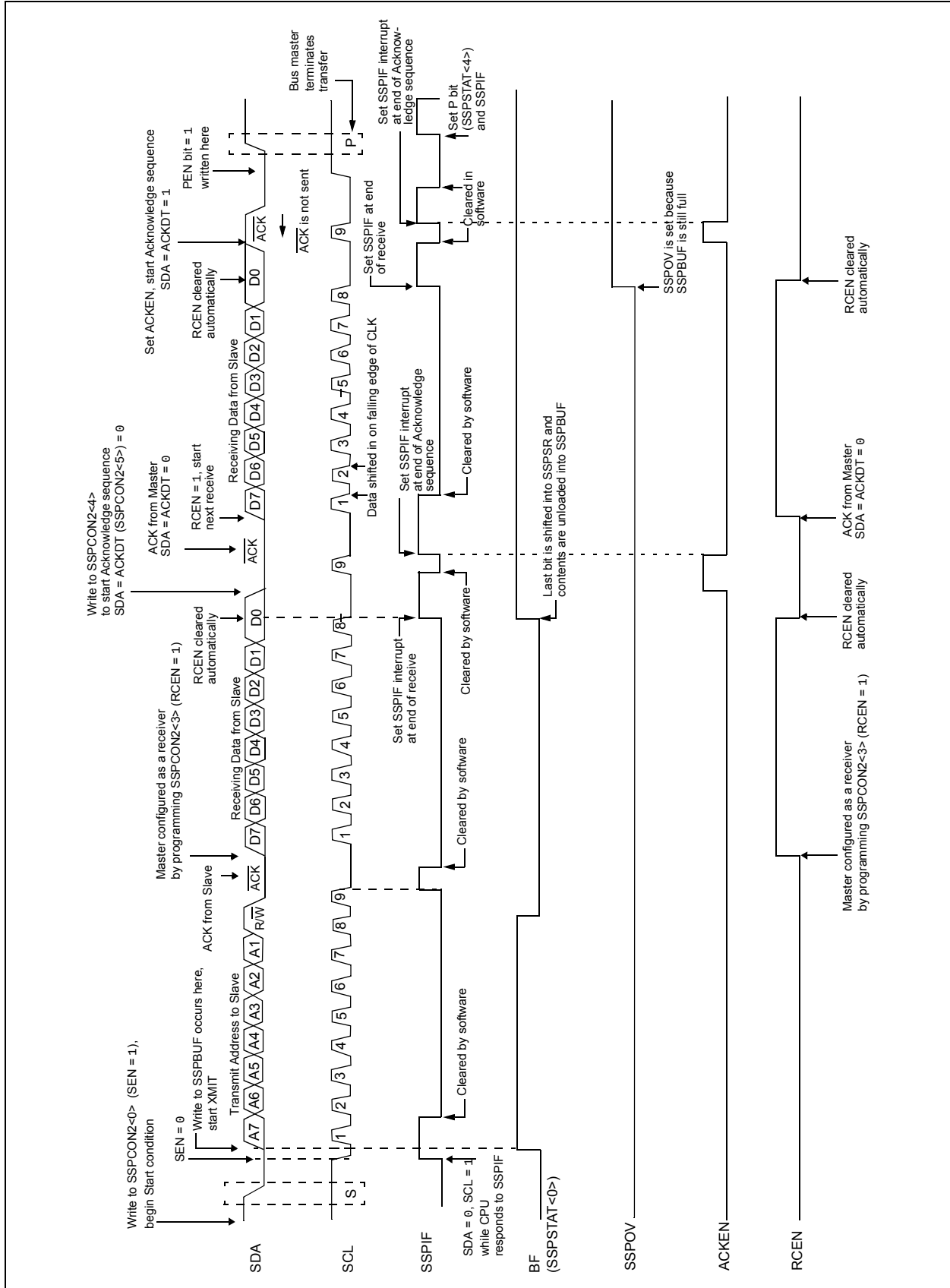


FIGURE 24-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



26.7.3 FREQUENCY THRESHOLD

The frequency threshold should be placed midway between the value of nominal frequency and the reduced frequency of the capacitive sensing oscillator. Refer to Application Note AN1103, “*Software Handling for Capacitive Sensing*” (DS01103) for more detailed information on the software required for CPS module.

Note: For more information on general capacitive sensing refer to Application Notes:

- AN1101, “*Introduction to Capacitive Sensing*” (DS01101)
- AN1102, “*Layout and Physical Design Guidelines for Capacitive Sensing*” (DS01102)

26.8 Operation during Sleep

The capacitive sensing oscillator will continue to run as long as the module is enabled, independent of the part being in Sleep. In order for the software to determine if a frequency change has occurred, the part must be awake. However, the part does not have to be awake when the timer resource is acquiring counts.

Note: Timer0 does not operate when in Sleep, and therefore cannot be used for capacitive sense measurements in Sleep.

PIC16(L)F1934/6/7

27.1 LCD Registers

The module contains the following registers:

- LCD Control register (LCDCON)
- LCD Phase register (LCDPS)
- LCD Reference Ladder register (LCDRL)
- LCD Contrast Control register (LDCST)
- LCD Reference Voltage Control register (LCDREF)
- Up to 3 LCD Segment Enable registers (LCDSEn)
- Up to 12 LCD data registers (LCDDATAn)

TABLE 27-1: LCD SEGMENT AND DATA REGISTERS

Device	# of LCD Registers	
	Segment Enable	Data
PIC16(L)F1936	2	8
PIC16(L)F1934/7	3	12

The LCDCON register (Register 27-1) controls the operation of the LCD driver module. The LCDPS register (Register 27-2) configures the LCD clock source prescaler and the type of waveform; Type-A or Type-B. The LCDSEn registers (Register 27-5) configure the functions of the port pins.

The following LCDSEn registers are available:

- LCDSE0 SE<7:0>
- LCDSE1 SE<15:8>
- LCDSE2 SE<23:16>⁽¹⁾

Note 1: PIC16(L)F1934/7 only.

Once the module is initialized for the LCD panel, the individual bits of the LCDDATAn registers are cleared/set to represent a clear/dark pixel, respectively:

- LCDDATA0 SEG<7:0>COM0
- LCDDATA1 SEG<15:8>COM0
- LCDDATA2 SEG<23:16>COM0⁽¹⁾
- LCDDATA3 SEG<7:0>COM1
- LCDDATA4 SEG<15:8>COM1
- LCDDATA5 SEG<23:16>COM1⁽¹⁾
- LCDDATA6 SEG<7:0>COM2
- LCDDATA7 SEG<15:8>COM2
- LCDDATA8 SEG<23:16>COM2⁽¹⁾
- LCDDATA9 SEG<7:0>COM3
- LCDDATA10 SEG<15:8>COM3
- LCDDATA11 SEG<23:16>COM3⁽¹⁾

Note 1: PIC16(L)F1934/7 only.

As an example, LCDDATAn is detailed in Register 27-6.

Once the module is configured, the LCDEN bit of the LCDCON register is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN bit of the LCDCON register.

FIGURE 31-65: PIC16F1937 BOR CURRENT

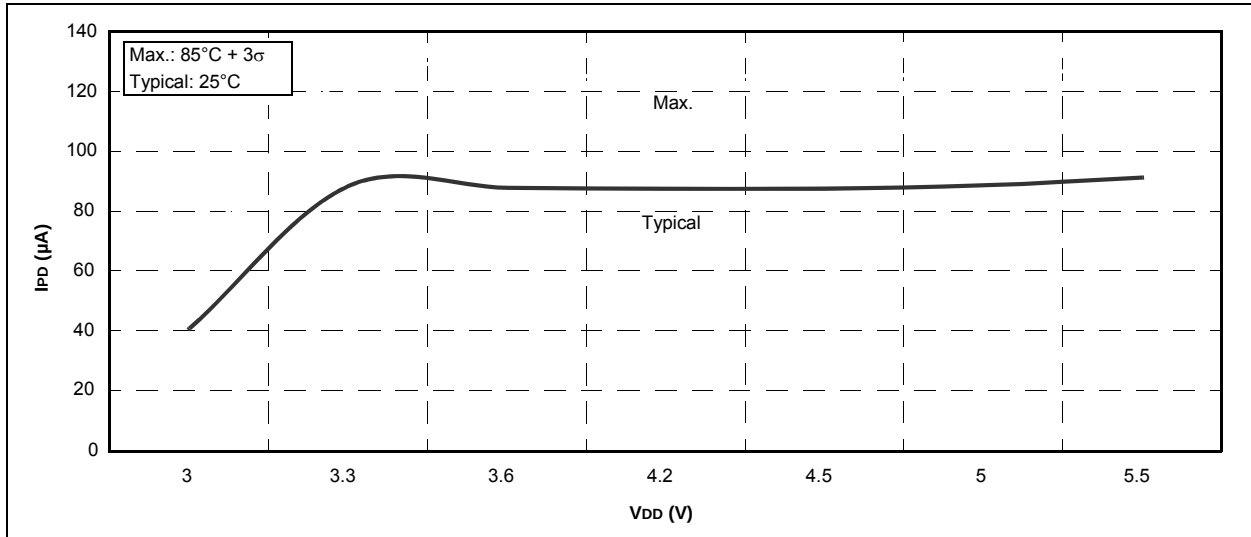
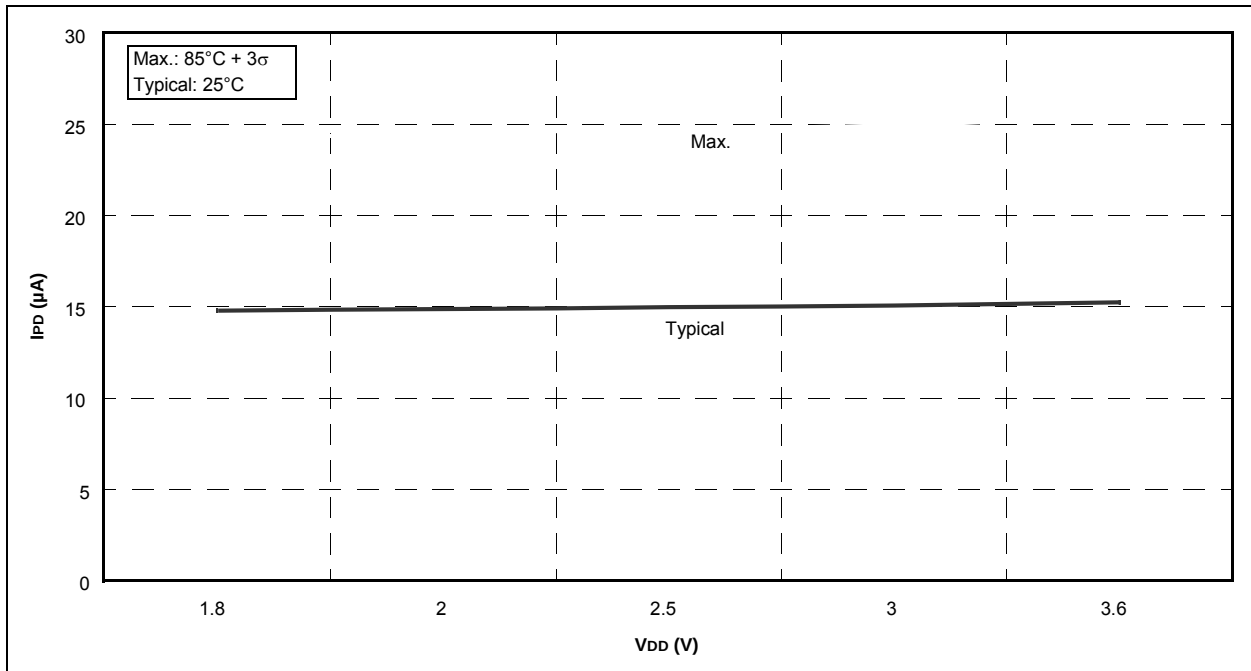


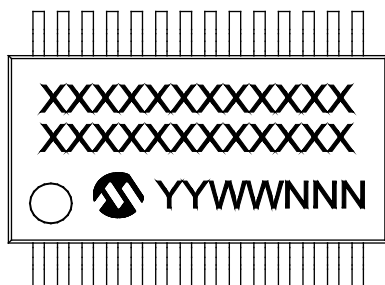
FIGURE 31-66: PIC16LF1937 FVR_ADC



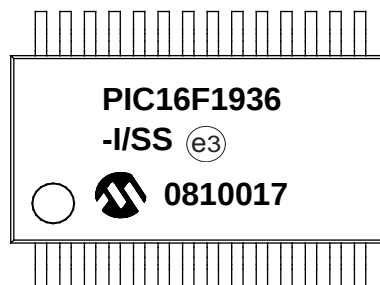
PIC16(L)F1934/6/7

Package Marking Information (Continued)

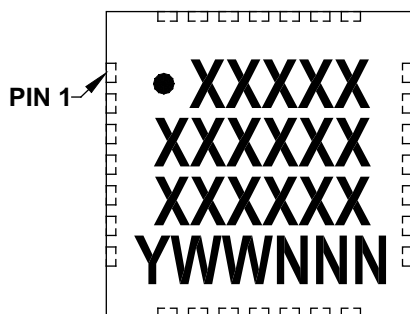
28-Lead SSOP (5.30 mm)



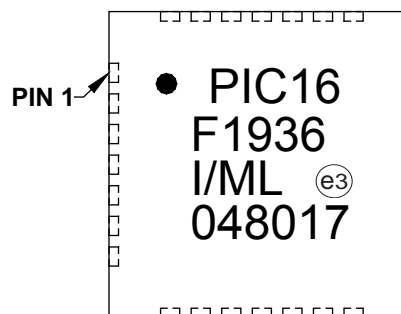
Example



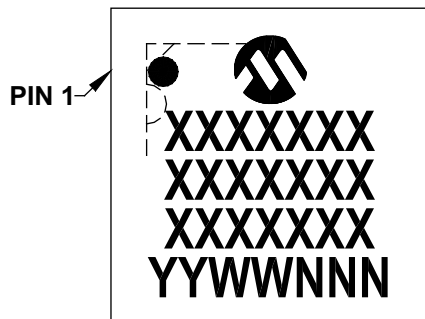
28-Lead UQFN (4x4x0.5 mm)



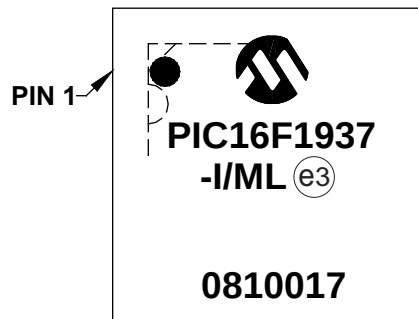
Example



40-Lead UQFN (5x5x0.5 mm)

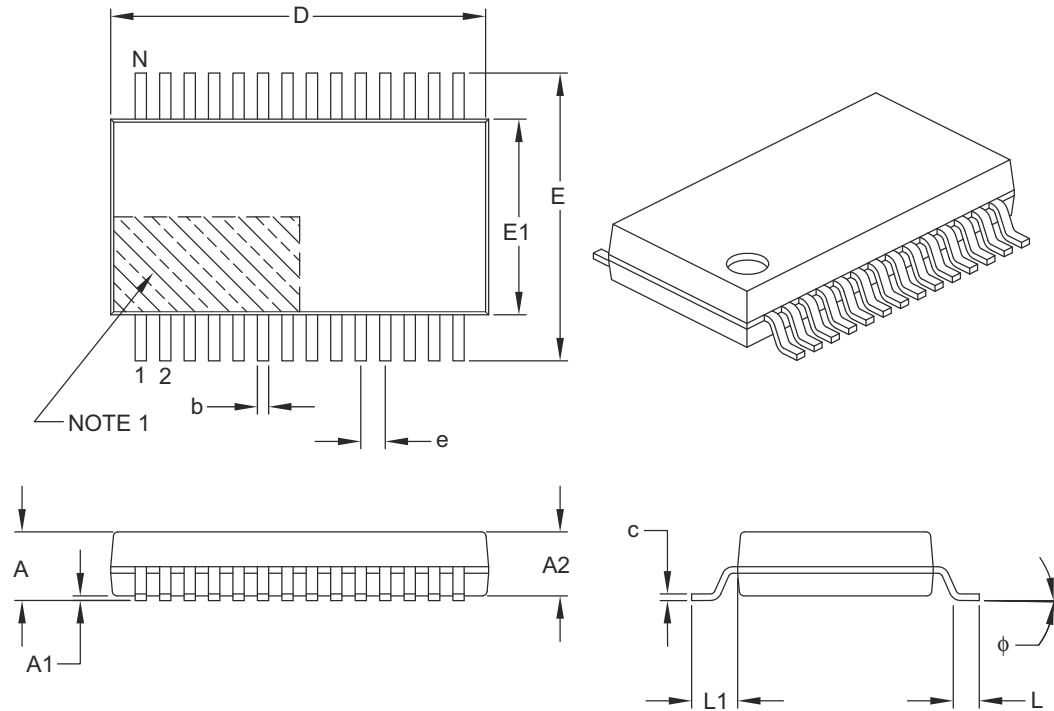


Example



28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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