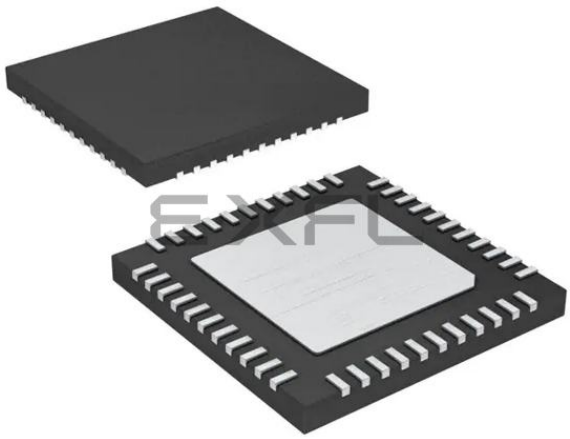

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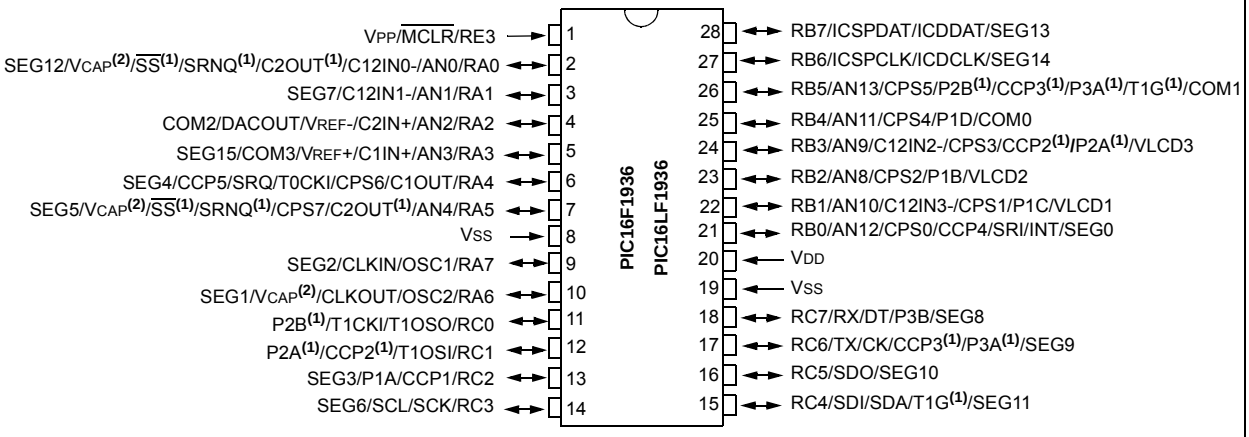
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1937t-i-ml

Pin Diagram – 28-Pin SPDIP/SOIC/SSOP (PIC16(L)F1936)

28-pin SPDIP, SOIC, SSOP



Note 1: Pin function is selectable via the APFCON register.

2: PIC16F1936 devices only.

TABLE 2: 40/44-PIN SUMMARY(PIC16(L)F1934/7)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ANSEL	A/D	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	LCD	Interrupt	Pull-up	Basic
RA0	2	17	19	19	Y	AN0	—	C12IN0-/ C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG12	—	—	VCAP
RA1	3	18	20	20	Y	AN1	—	C12IN1-	—	—	—	—	—	SEG7	—	—	—
RA2	4	19	21	21	Y	AN2/ VREF-	—	C2IN+/ DACOUT	—	—	—	—	—	COM2	—	—	—
RA3	5	20	22	22	Y	AN3/ VREF+	—	C1IN+	—	—	—	—	—	SEG15	—	—	—
RA4	6	21	23	23	Y	—	CPS6	C1OUT	SRQ	T0CKI		—	—	SEG4	—	—	—
RA5	7	22	24	24	Y	AN4	CPS7	C2OUT(1)	SRNQ(1)	—	—	—	$\overline{SS}$(1)	SEG5	—	—	VCAP
RA6	14	29	31	33	—	—	—	—	—	—	—	—	—	SEG1	—	—	OSC2/ CLKOUT VCAP
RA7	13	28	30	32	—	—	—	—	—	—	—	—	—	SEG2	—	—	OSC1/ CLKIN
RB0	33	8	8	9	Y	AN12	CPS0	—	SRI	—	—	—	—	SEG0	INT/ IOC	Y	—
RB1	34	9	9	10	Y	AN10	CPS1	C12IN3-	—	—	—	—	—	VLCD1	IOC	Y	—
RB2	35	10	10	11	Y	AN8	CPS2	—	—	—	—	—	—	VLCD2	IOC	Y	—
RB3	36	11	11	12	Y	AN9	CPS3	C12IN2-	—	—	CCP2(1)/ P2A(1)	—	—	VLCD3	IOC	Y	—
RB4	37	12	14	14	Y	AN11	CPS4	—	—	—	—	—	—	COM0	IOC	Y	—
RB5	38	13	15	15	Y	AN13	CPS5	—	—	T1G(1)	CCP3(1)/ P3A(1)	—	—	COM1	IOC	Y	—
RB6	39	14	16	16	—	—	—	—	—	—	—	—	—	SEG14	IOC	Y	ICSPCLK/ ICDCLK
RB7	40	15	17	17	—	—	—	—	—	—	—	—	—	SEG13	IOC	Y	ICSPDAT/ ICDDAT
RC0	15	30	32	34	—	—	—	—	—	T1OSO/ T1CKI	P2B(1)	—	—	—	—	—	—
RC1	16	31	35	35	—	—	—	—	—	T1OSI	CCP2(1)/ P2A(1)	—	—	—	—	—	—
RC2	17	32	36	36	—	—	—	—	—	—	CCP1/ P1A	—	—	SEG3	—	—	—
RC3	18	33	37	37	—	—	—	—	—	—	—	—	SCK/SCL	SEG6	—	—	—
RC4	23	38	42	42	—	—	—	—	—	T1G(1)	—	—	SDI/SDA	SEG11	—	—	—
RC5	24	39	43	43	—	—	—	—	—	—	—	—	SDO	SEG10	—	—	—
RC6	25	40	44	44	—	—	—	—	—	—	—	TX/CK	—	SEG9	—	—	—
RC7	26	1	1	1	—	—	—	—	—	—	—	RX/DT	—	SEG8	—	—	—
RD0	19	34	38	38	Y	—	CPS8	—	—	—	—	—	—	COM3	—	—	—
RD1	20	35	39	39	Y	—	CPS9	—	—	—	CCP4	—	—	—	—	—	—
RD2	21	36	40	40	Y	—	CPS10	—	—	—	P2B(1)	—	—	—	—	—	—
RD3	22	37	41	41	Y	—	CPS11	—	—	—	P2C	—	—	SEG16	—	—	—
RD4	27	2	2	2	Y	—	CPS12	—	—	—	P2D	—	—	SEG17	—	—	—
RD5	28	3	3	3	Y	—	CPS13	—	—	—	P1B	—	—	SEG18	—	—	—
RD6	29	4	4	4	Y	—	CPS14	—	—	—	P1C	—	—	SEG19	—	—	—
RD7	30	5	5	5	Y	—	CPS15	—	—	—	P1D	—	—	SEG20	—	—	—
RE0	8	23	25	25	Y	AN5	—	—	—	—	CCP3(1) P3A(1)	—	—	SEG21	—	—	—
RE1	9	24	26	26	Y	AN6	—	—	—	—	P3B	—	—	SEG22	—	—	—
RE2	10	25	27	27	Y	AN7	—	—	—	—	CCP5	—	—	SEG23	—	—	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	11, 32	7, 26	7, 28	7,8, 28	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	12, 31	6, 27	6, 29	6,30, 31	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be moved using the APFCON register.

TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA6/OSC2/CLKOUT/VCAP(2)/ SEG1	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1934/6/7 only).
	SEG1	—	AN	LCD Analog output.
RA7/OSC1/CLKIN/SEG2	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG2	—	AN	LCD Analog output.
RB0/AN12/CPS0/CCP4/SRI/INT/ SEG0	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
	SRI	—	ST	SR Latch input.
	INT	ST	—	External interrupt.
	SEG0	—	AN	LCD analog output.
RB1/AN10/C12IN3-/CPS1/P1C/ VLCD1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	CPS1	AN	—	Capacitive sensing input 1.
	P1C	—	CMOS	PWM output.
	VLCD1	AN	—	LCD analog input.
RB2/AN8/CPS2/P1B/VLCD2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
	P1B	—	CMOS	PWM output.
	VLCD2	AN	—	LCD analog input.
RB3/AN9/C12IN2-/CPS3/ CCP2(1)/P2A(1)/VLCD3	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
	VLCD3	AN	—	LCD analog input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin function is selectable via the APFCON register.
2: PIC16F1934/6/7 devices only.
3: PIC16(L)F1936 devices only.
4: PORTD is available on PIC16(L)F1934/7 devices only.
5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

12.2 PORTA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 12-3). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 12-1 shows how to initialize an I/O port.

Reading the PORTA register (Register 12-2) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

The TRISA register (Register 12-3) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

12.2.1 ANSELA REGISTER

The ANSELA register (Register 12-5) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

12.2.2 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 12-2.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input functions, such as ADC, comparator and CapSense inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown in Table 12-2.

TABLE 12-2: PORTA OUTPUT PRIORITY

Pin Name	Function Priority(1)
RA0	VCAP SEG12 (LCD) SRNQ (SR Latch) C2OUT (Comparator) RA0
RA1	SEG7 (LCD) RA1
RA2	COM2 (LCD) AN2 (DAC) RA2
RA3	COM3 (LCD) 28-pin only SEG15 RA3
RA4	SEG4 (LCD) SRQ (SR Latch) C1OUT (Comparator) CCP5, 28-pin only RA4
RA5	VCAP (enabled by Config. Word) SEG5 (LCD) SRNQ (SR Latch) C2OUT (Comparator) RA5
RA6	VCAP (enabled by Config. Word) OSC2 (enabled by Config. Word) CLKOUT (enabled by Config. Word) SEG1 (LCD) RA6
RA7	OSC1/CLKIN (enabled by Config. Word) SEG2 (LCD) RA7

Note 1: Priority listed from highest to lowest.

REGISTER 12-20: LATE: PORTE DATA LATCH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	LATE2	LATE1	LATE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **LATE<2:0>**: PORTE Output Latch Value bits(1)

Note 1: Writes to PORTE are actually written to corresponding LATE register. Reads from PORTE register is return of actual I/O pin values.

REGISTER 12-21: ANSELE: PORTE ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	ANSE2(2)	ANSE1(2)	ANSE0(2)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSE<2:0>**: Analog Select between Analog or Digital Function on Pins RE<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: ANSELE register is not implemented on the PIC16(L)F1936. Read as '0'

NOTES:

23.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains three Enhanced Capture/Compare/PWM modules (ECCP1, ECCP2, and ECCP3) and two standard Capture/Compare/PWM modules (CCP4 and CCP5).

The Capture and Compare functions are identical for all five CCP modules (ECCP1, ECCP2, ECCP3, CCP4, and CCP5). The only differences between CCP modules are in the Pulse-Width Modulation (PWM) function. The standard PWM function is identical in modules, CCP4 and CCP5. In CCP modules ECCP1, ECCP2, and ECCP3, the Enhanced PWM function has slight variations from one another. Full-Bridge ECCP modules have four available I/O pins while Half-Bridge ECCP modules only have two available I/O pins. See Table 23-1 for more information.

Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to ECCP1, ECCP2, ECCP3, CCP4 and CCP5. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.

TABLE 23-1: PWM RESOURCES

Device Name	ECCP1	ECCP2	ECCP3	CCP4	CCP5
PIC16(L)F1936	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM
PIC16(L)F1934/7	Enhanced PWM Full-Bridge	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM

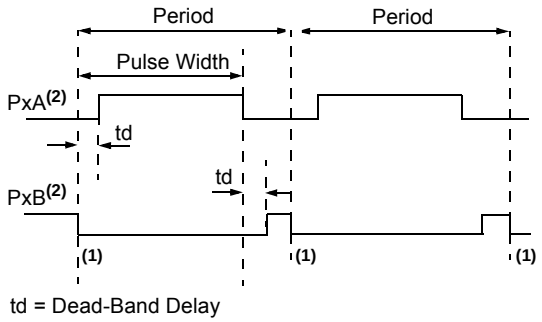
23.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCPx/PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 23-9). This mode can be used for Half-Bridge applications, as shown in Figure 23-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWMxCON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 23.4.5 "Programmable Dead-Band Delay Mode"** for more details of the dead-band delay operations.

Since the PxA and PxB outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure PxA and PxB as outputs.

FIGURE 23-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

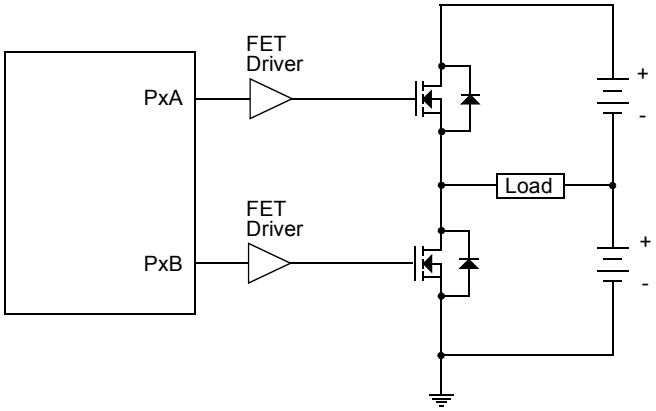


Note 1: At this time, the TMRx register is equal to the PRx register.

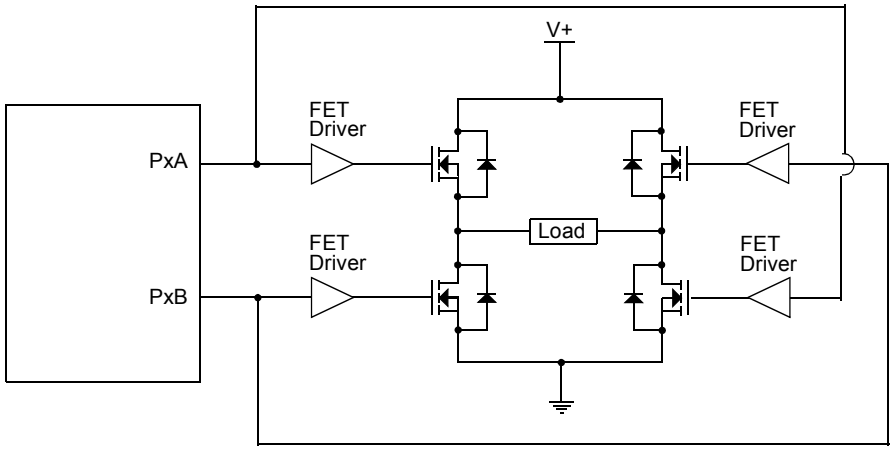
2: Output signals are shown as active-high.

FIGURE 23-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS

Standard Half-Bridge Circuit ("Push-Pull")



Half-Bridge Output Driving a Full-Bridge Circuit



24.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 24-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and Status bits appropriately set).

The clock polarity is selected by appropriately programming the CKP bit of the SSPCON1 register and the CKE bit of the SSPSTAT register. This then, would give waveforms for SPI communication as shown in Figure 24-6, Figure 24-8 and Figure 24-9, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 * TCY)
- FOSC/64 (or 16 * TCY)
- Timer2 output/2
- Fosc/(4 * (SSPADD + 1))

Figure 24-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 24-6: SPI MODE WAVEFORM (MASTER MODE)

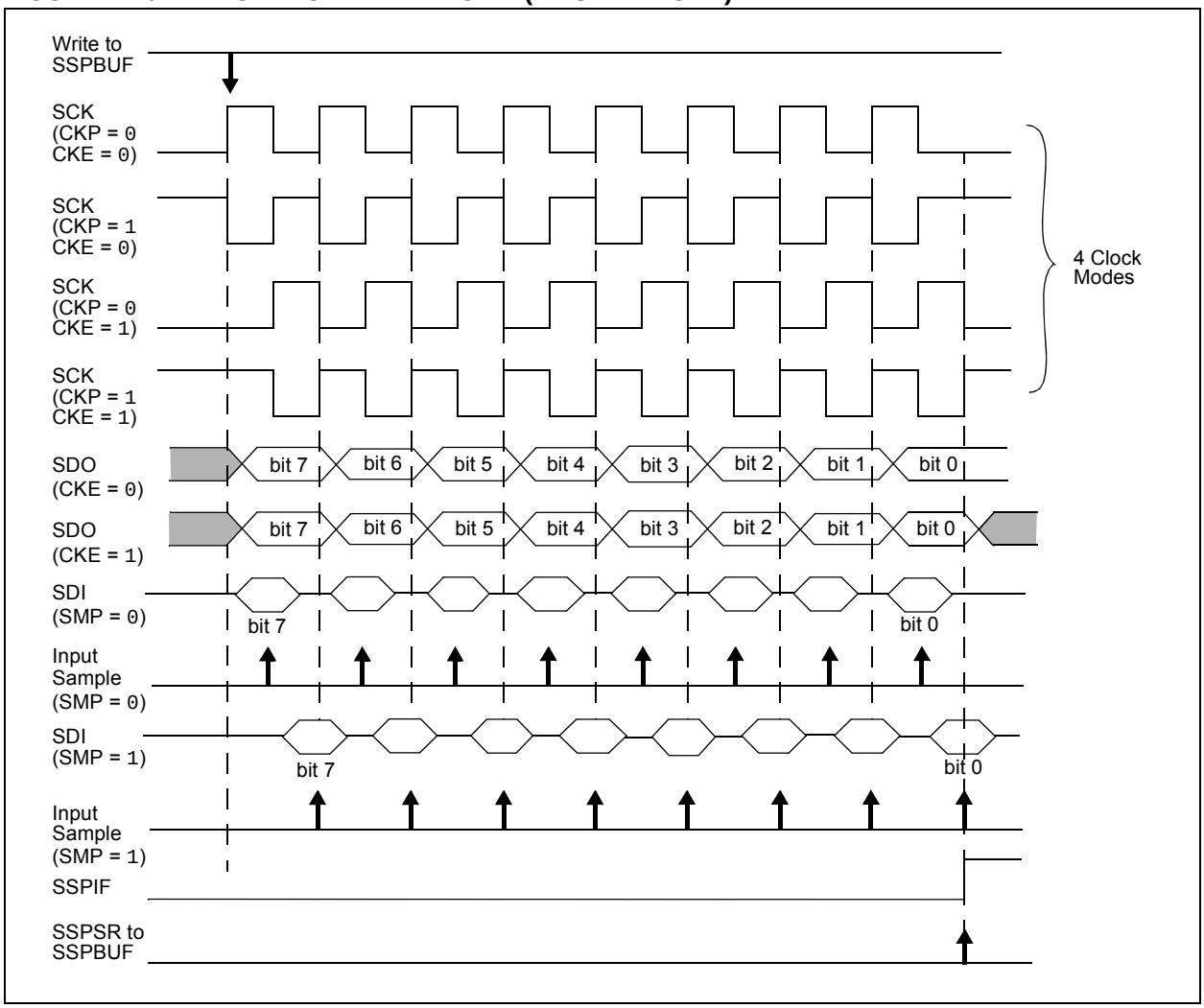


FIGURE 24-12: I²C START AND STOP CONDITIONS

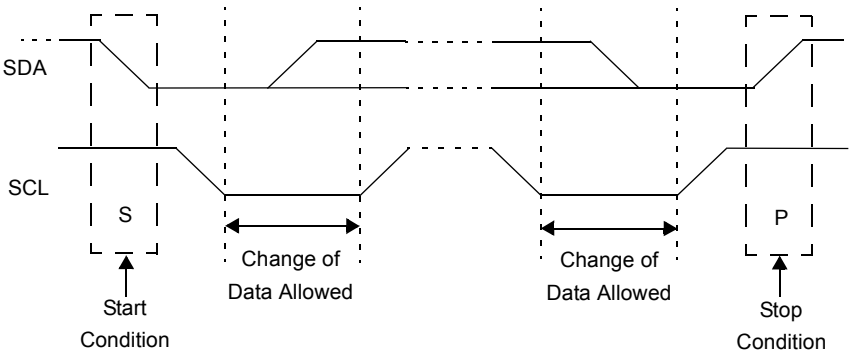
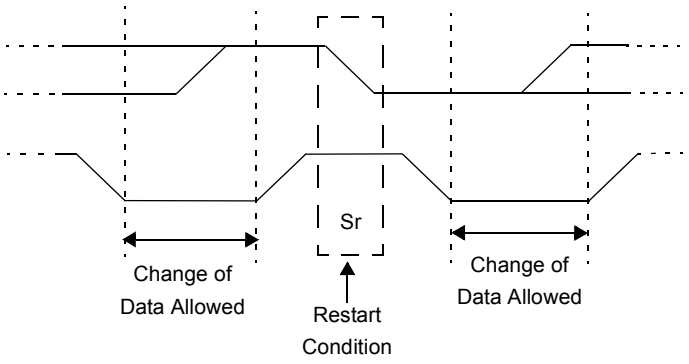


FIGURE 24-13: I²C RESTART CONDITION



24.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPCON3 register enables additional clock stretching and interrupt generation after the 8th falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPIF interrupt is set.

Figure 24-18 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPSTAT is set; SSPIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with R/$\overline{W}$ bit set. After the 8th falling edge of the SCL line the CKP bit is cleared and SSPIF interrupt is generated.
4. Slave software clears SSPIF.
5. Slave software reads ACKTIM bit of SSPCON3 register, and R/$\overline{W}$ and D/$\overline{A}$ of the SSPSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to $\overline{ACK}$ or not $\overline{ACK}$ and sets ACKDT bit of the SSPCON2 register accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the $\overline{ACK}$ value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPIF after the $\overline{ACK}$ if the R/$\overline{W}$ bit is set.
11. Slave software clears SSPIF.
12. Slave loads value to transmit to the master into SSPBUF setting the BF bit.

Note: SSPBUF cannot be loaded until after the $\overline{ACK}$.

13. Slave sets CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an $\overline{ACK}$ value on the 9th SCL pulse.
15. Slave hardware copies the $\overline{ACK}$ value into the ACKSTAT bit of the SSPCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not $\overline{ACK}$ the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not $\overline{ACK}$ on the last byte to ensure that the slave releases the SCL line to receive a Stop.

27.4.3 AUTOMATIC POWER MODE SWITCHING

As an LCD segment is electrically only a capacitor, current is drawn only during the interval where the voltage is switching. To minimize total device current, the LCD internal reference ladder can be operated in a different power mode for the transition portion of the duration. This is controlled by the LCDRL register (Register 27-7).

The LCDRL register allows switching between two power modes, designated 'A' and 'B'. 'A' Power mode is active for a programmable time, beginning at the time when the LCD segments transition. 'B' Power mode is the remaining time before the segments or commons change again. The LRLAT<2:0> bits select how long, if any, that the 'A' Power mode is active. Refer to Figure 27-4.

To implement this, the 5-bit prescaler used to divide the 32 kHz clock down to the LCD controller's 1 kHz base rate is used to select the power mode.

FIGURE 27-4: LCD INTERNAL REFERENCE LADDER POWER MODE SWITCHING DIAGRAM – TYPE A

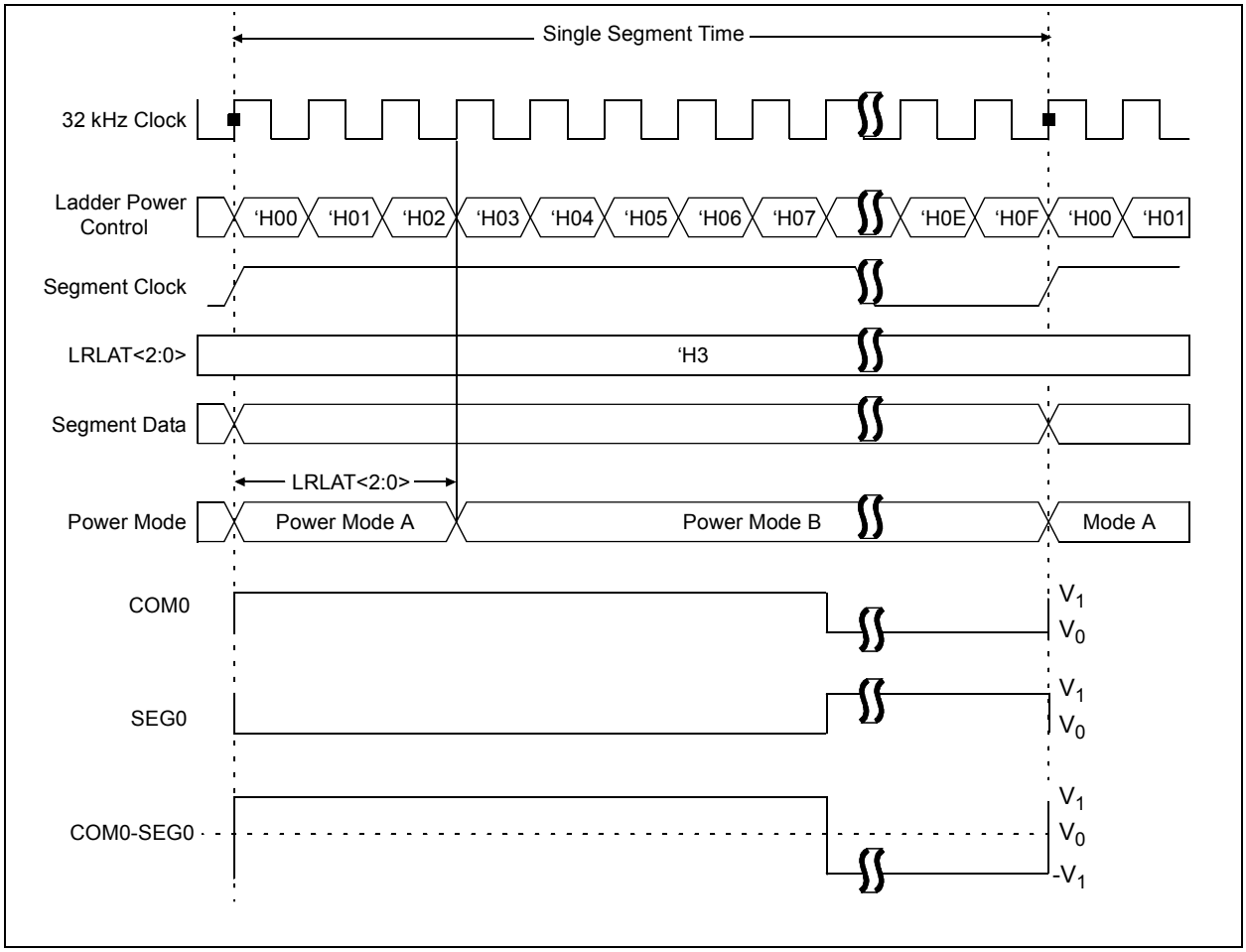
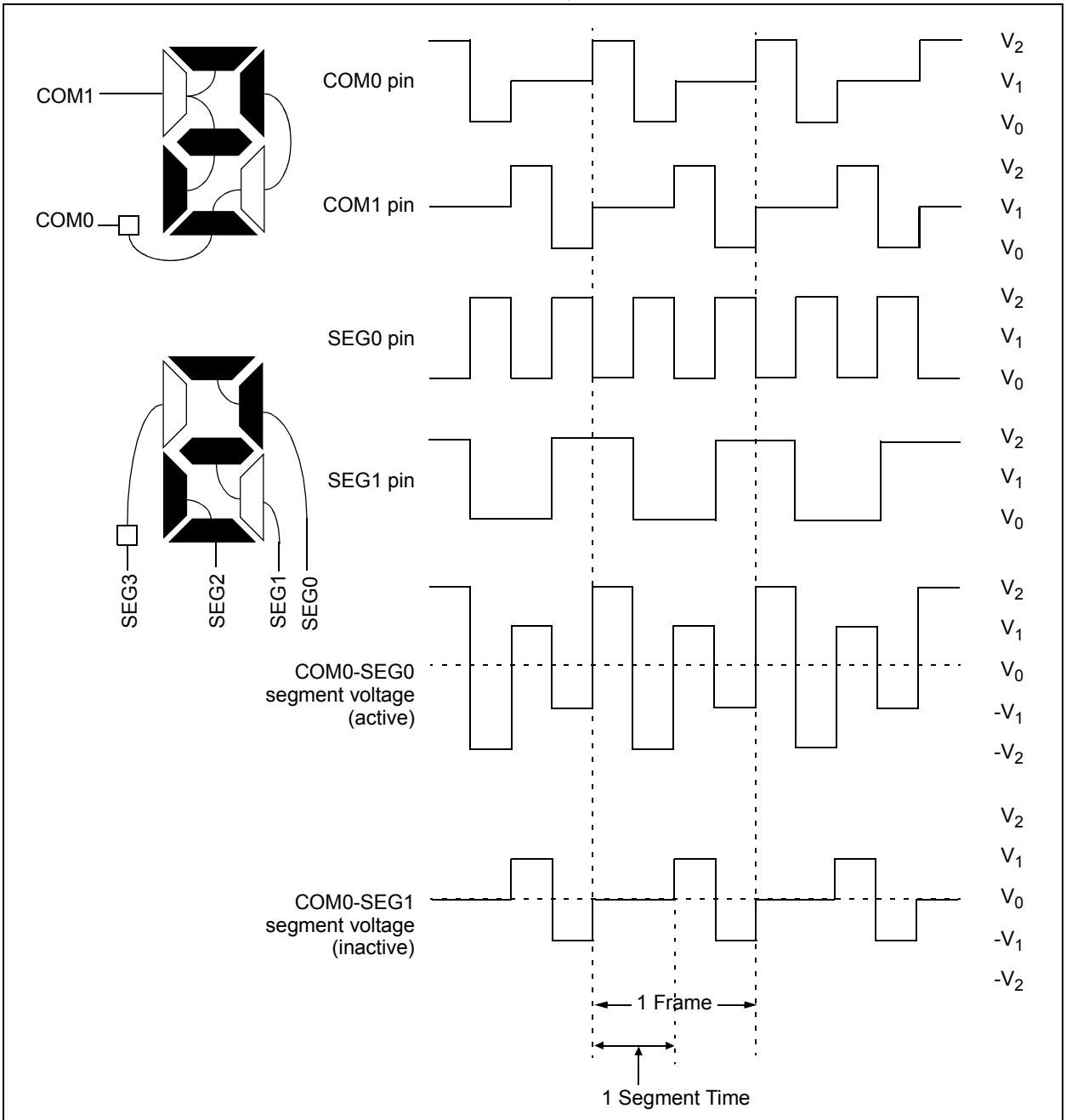


FIGURE 27-9: TYPE-A WAVEFORMS IN 1/2 MUX, 1/2 BIAS DRIVE



Note: 1 Frame = 2 single segment times.

NOTES:

BCF **Bit Clear f**

Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BRA **Relative Branch**

Syntax:	[*label*] BRA label [*label*] BRA $+k
Operands:	-256 ≤ label - PC + 1 ≤ 255 -256 ≤ k ≤ 255
Operation:	(PC) + 1 + k → PC
Status Affected:	None
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + k. This instruction is a two-cycle instruction. This branch has a limited range.

BRW **Relative Branch with W**

Syntax:	[*label*] BRW
Operands:	None
Operation:	(PC) + (W) → PC
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + (W). This instruction is a two-cycle instruction.

BSF **Bit Set f**

Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

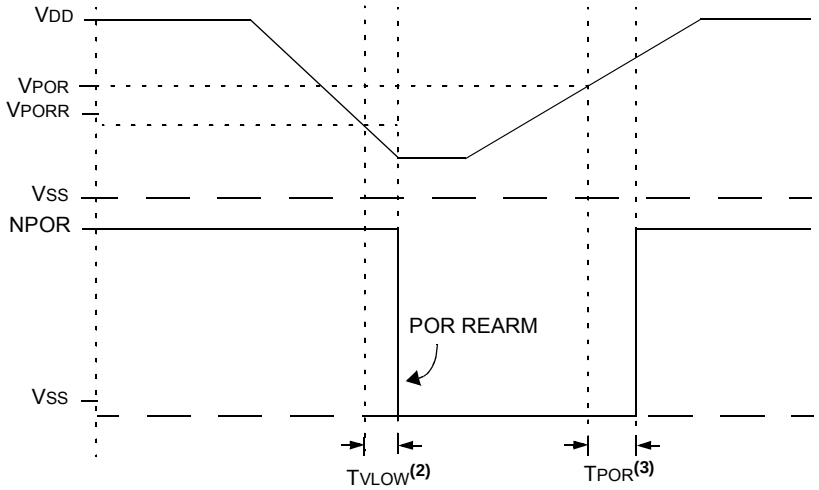
BTFSC **Bit Test f, Skip if Clear**

Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS **Bit Test f, Skip if Set**

Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

FIGURE 30-4: POR AND POR REARM WITH SLOW RISING VDD



Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

FIGURE 31-62: PIC16LF1937 TIMER 1 OSCILLATOR

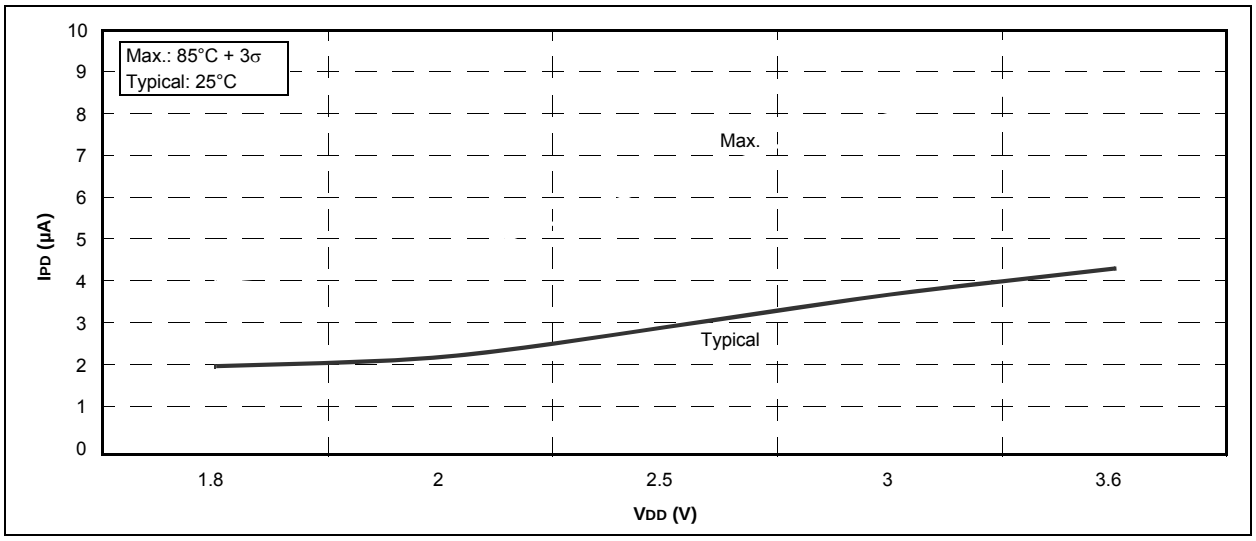


FIGURE 31-63: PIC16F1937 TIMER 1 OSCILLATOR

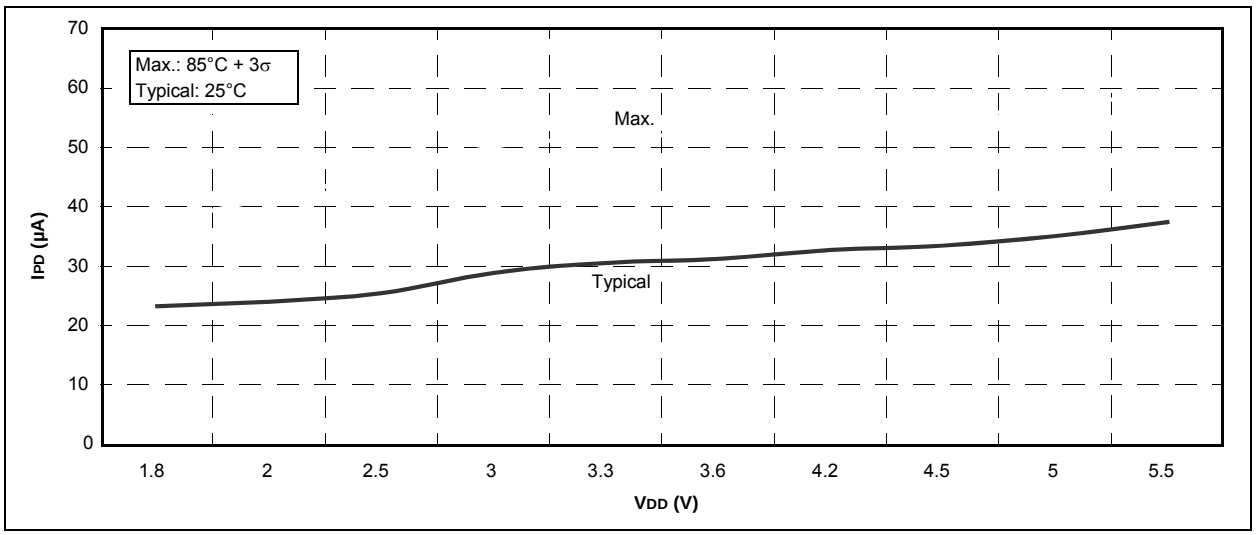
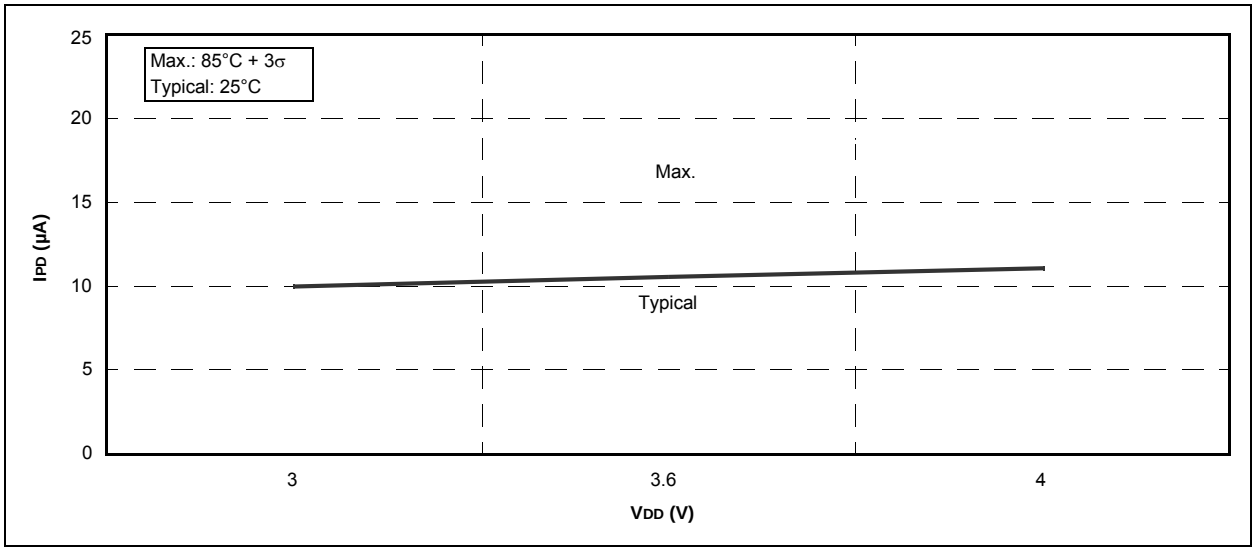
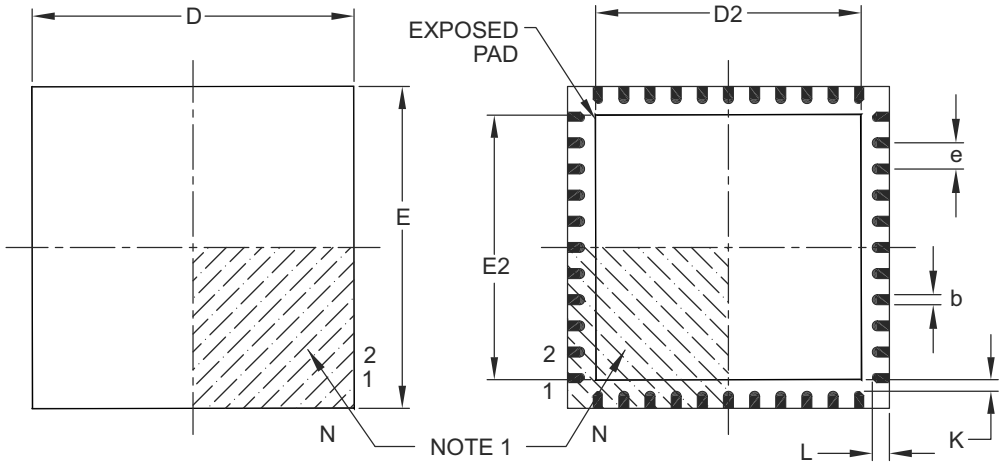


FIGURE 31-64: PIC16LF1937 BOR CURRENT

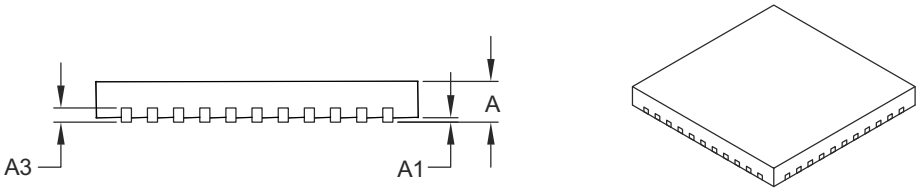


44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

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