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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1937t-i-pt

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Name	Function	Input Type	Output Type	Description
RA0/AN0/C12IN0-/C2OUT ⁽¹⁾ /	RA0	TTL	CMOS	General purpose I/O.
SRNQ ⁽¹⁾ / SS⁽¹⁾/VCAP⁽²⁾/SEG12	AN0	AN	—	A/D Channel 0 input.
	C12IN0-	AN	_	Comparator C1 or C2 negative input.
	C2OUT		CMOS	Comparator C2 output.
	SRNQ	_	CMOS	SR Latch inverting output.
	SS	ST		Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1934/6/7 only).
	SEG12	_	AN	LCD Analog output.
RA1/AN1/C12IN1-/SEG7	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	_	A/D Channel 1 input.
	C12IN1-	AN	_	Comparator C1 or C2 negative input.
	SEG7	_	AN	LCD Analog output.
RA2/AN2/C2IN+/VREF-/	RA2	TTL	CMOS	General purpose I/O.
DACOUT/COM2	AN2	AN	_	A/D Channel 2 input.
	C2IN+	AN	_	Comparator C2 positive input.
	VREF-	AN	_	A/D Negative Voltage Reference input.
	DACOUT	_	AN	Voltage Reference output.
	COM2		AN	LCD Analog output.
RA3/AN3/C1IN+/VREF+/	RA3	TTL	CMOS	General purpose I/O.
COM3 ⁽³⁾ /SEG15	AN3	AN	_	A/D Channel 3 input.
	C1IN+	AN	_	Comparator C1 positive input.
	VREF+	AN	—	A/D Voltage Reference input.
	COM3 ⁽³⁾	_	AN	LCD Analog output.
	SEG15		AN	LCD Analog output.
RA4/C1OUT/CPS6/T0CKI/SRQ/	RA4	TTL	CMOS	General purpose I/O.
CCP5/SEG4	C10UT		CMOS	Comparator C1 output.
	CPS6	AN	_	Capacitive sensing input 6.
	TOCKI	ST	—	Timer0 clock input.
	SRQ		CMOS	SR Latch non-inverting output.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG4	_	AN	LCD Analog output.
RA5/AN4/C2OUT ⁽¹⁾ /CPS7/	RA5	TTL	CMOS	General purpose I/O.
SRNQ ⁽¹⁾ /SS ⁽¹⁾ /VCAP ⁽²⁾ /SEG5	AN4	AN	—	A/D Channel 4 input.
	C2OUT	_	CMOS	Comparator C2 output.
	CPS7	AN	_	Capacitive sensing input 7.
	SRNQ	_	CMOS	SR Latch inverting output.
	SS	ST	_	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1934/6/7 only).
	SEG5	_	AN	LCD Analog output.

TABLE 1-2: PIC16(L)F1934/6/7 PINOUT DESCRIPTION

Legend:AN= Analog input or outputCMOS = CMOS compatible input or outputOD= Open DrainTTL = TTL compatible inputST= Schmitt Trigger input with CMOS levels l^2C^{TM} = Schmitt Trigger input with l²C

HV = High Voltage XTAL = Crystal

levels

Note 1: Pin function is selectable via the APFCON register.

2: PIC16F1934/6/7 devices only.

3: PIC16(L)F1936 devices only.

4: PORTD is available on PIC16(L)F1934/7 devices only.

5: RE<2:0> are available on PIC16(L)F1934/7 devices only.

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3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

constants			
RETLW 1	DATA0	;Index0	data
RETLW 1	DATA1	;Index1	data
RETLW 1	DATA2		
RETLW 1	DATA3		
my_functio	n		
; LOT:	S OF CODE		
MOVLW	LOW constan	ts	
MOVWF	FSR1L		
MOVLW	HIGH consta	nts	
MOVWF	FSR1H		
MOVIW	0[FSR1]		
;THE PROGR	AM MEMORY IS	IN W	

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.5** "Indirect Addressing" for more information.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation of the PIC16(L)F1934/6/7. These registers are listed below:

- INDF0
- INDF1
- PCL
- STATUS
- FSR0 Low
- FSR0 High
- FSR1 Low
- FSR1 High
- BSR
- WREG
- PCLATH
- INTCON

Note: The core registers are the first 12 addresses of every data memory bank.

TABLE 3-4: PIC16(L)F1934 MEMORY MAP, BANKS 8-15

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	INDF0	480h	INDF0	500h	INDF0	580h	INDF0	600h	INDF0	680h	INDF0	700h	INDF0	780h	INDF0
401h	INDF1	481h	INDF1	501h	INDF1	581h	INDF1	601h	INDF1	681h	INDF1	701h	INDF1	781h	INDF1
402h	PCL	482h	PCL	502h	PCL	582h	PCL	602h	PCL	682h	PCL	702h	PCL	782h	PCL
403h	STATUS	483h	STATUS	503h	STATUS	583h	STATUS	603h	STATUS	683h	STATUS	703h	STATUS	783h	STATUS
404h	FSR0L	484h	FSR0L	504h	FSR0L	584h	FSR0L	604h	FSR0L	684h	FSR0L	704h	FSR0L	784h	FSR0L
405h	FSR0H	485h	FSR0H	505h	FSR0H	585h	FSR0H	605h	FSR0H	685h	FSR0H	705h	FSR0H	785h	FSR0H
406h	FSR1L	486h	FSR1L	506h	FSR1L	586h	FSR1L	606h	FSR1L	686h	FSR1L	706h	FSR1L	786h	FSR1L
407h	FSR1H	487h	FSR1H	507h	FSR1H	587h	FSR1H	607h	FSR1H	687h	FSR1H	707h	FSR1H	787h	FSR1H
408h	BSR	488h	BSR	508h	BSR	588h	BSR	608h	BSR	688h	BSR	708h	BSR	788h	BSR
409h	WREG	489h	WREG	509h	WREG	589h	WREG	609h	WREG	689h	WREG	709h	WREG	789h	WREG
40Ah	PCLATH	48Ah	PCLATH	50Ah	PCLATH	58Ah	PCLATH	60Ah	PCLATH	68Ah	PCLATH	70Ah	PCLATH	78Ah	PCLATH
40Bh	INTCON	48Bh	INTCON	50Bh	INTCON	58Bh	INTCON	60Bh	INTCON	68Bh	INTCON	70Bh	INTCON	78Bh	INTCON
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	_	58Dh	_	60Dh	—	68Dh	—	70Dh	—	78Dh	_
40Eh	—	48Eh	_	50Eh	_	58Eh	_	60Eh		68Eh	—	70Eh	—	78Eh	—
40Fh	_	48Fh	_	50Fh	_	58Fh	_	60Fh	—	68Fh	—	70Fh	—	78Fh	_
410h	_	490h	_	510h	_	590h	_	610h	—	690h	—	710h	—	790h	_
411h	—	491h		511h		591h		611h		691h		711h		791h	
412h	—	492h		512h	—	592h	_	612h		692h		712h		792h	
413h	—	493h		513h	—	593h	_	613h		693h		713h		793h	
414h		494h		514h	—	594h	_	614h		694h		714h		794h	
415h	TMR4	495h	_	515h	_	595h	_	615h	—	695h	—	715h	—	795h	
416h	PR4	496h	—	516h	—	596h	—	616h	—	696h	—	716h	—	796h	
417h	T4CON	497h		517h		597h		617h		697h		717h		797h	
418h	—	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	
41Ah	_	49Ah		51Ah	_	59Ah	_	61Ah		69Ah		71Ah		79Ah	See Table 3-9 or
41Bh		49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	_	71Bh	_	79Bh	Table 3-10
41Ch	TMR6	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	
41Dh	PR6	49Dh	_	51Dh	_	59Dh	_	61Dh	—	69Dh		71Dh		79Dh	
41Eh	16CON	49Eh	_	51Eh	_	59Eh	_	61Eh	—	69Eh		71Eh		79Eh	
41Fh	_	49Fh	_	51Fh	_	59Fh	_	61Fh	—	69Fh		71Fh		79Fh	
420n		4A0n		520n		5AUN		620h		6AUN		720n		7A0n	
	Unimplemented														
	Read as 0														
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h		4F0h		570h		5F0h		670h		6F0h		770h		7F0h	
	Accesses														
	70h – 7Fh														
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 15	(Continued)										
7A6h	LCDDATA6	SEG7 COM2	SEG6 COM2	SEG5 COM2	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2	XXXX XXXX	uuuu uuuu
7A7h	LCDDATA7	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2	XXXX XXXX	uuuu uuuu
7A8h	LCDDATA8 ⁽ 3)	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	XXXX XXXX	uuuu uuuu
7A9h	LCDDATA9	SEG7 COM3	SEG6 COM3	SEG5 COM3	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3	XXXX XXXX	uuuu uuuu
7AAh	LCDDATA1 0	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3	XXXX XXXX	uuuu uuuu
7ABh	LCDDATA11 ⁽ 3)	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	XXXX XXXX	uuuu uuuu
7ACh — 7EFh	_	Unimplemen	nted							_	_

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred Note 1: to the upper byte of the program counter.

2: These registers can be addressed from any bank.

These registers/bits are not implemented on PIC16(L)F1936 devices, read as '0'. 3:

4: Unimplemented, read as '1'.

PIC16(L)F1934/6/7

	• · = · •	. = •			. =		•••••	/					
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on BOR	Value otł Res	on all her sets
Banks 1	6-30												
x00h/ x80h ⁽²⁾	INDF0	Addressing (not a physi	this location u cal register)	ses contents o	of FSR0H/FSF	R0L to address	data memor	ý		xxxx	xxxx	xxxx	xxxx
x00h/ x81h ⁽²⁾ INDF1 Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx	xxxx	xxxx	xxxx		
x02h/ x82h ⁽²⁾	PCL	Program Co	Program Counter (PC) Least Significant Byte							0000	0000	0000	0000
x03h/ x83h ⁽²⁾	STATUS	-	-	_	TO	PD	Z	DC	С	1	1000	d	quuu
x04h/ x84h ⁽²⁾ FSR0L Indirect Data Memory Address 0 Low Pointer										0000	0000	uuuu	uuuu
x05h/ x85h (2)	FSR0H	Indirect Dat	indirect Data Memory Address 0 High Pointer							0000	0000	0000	0000
x06h/ x86h ⁽²⁾	FSR1L	Indirect Dat	Indirect Data Memory Address 1 Low Pointer							0000	0000	uuuu	uuuu
x07h/ x87h ⁽²⁾	FSR1H	Indirect Dat	a Memory Add	dress 1 High P	Pointer					0000	0000	0000	0000
x08h/ x88h ⁽²⁾	BSR	—	—	—		I	BSR<4:0>			0	0000	0	0000
x09h/ x89h ⁽²⁾	WREG	Working Re	gister							0000	0000	uuuu	uuuu
x0Ah/ x8Ah ^{(1),(2)}	PCLATH	-	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	r			-000	0000	-000	0000
x0Bh/ x8Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000	0000	0000	0000
x0Ch/ x8Ch	_	Unimpleme	nted							-	-	-	_
 x1Fh/ x9Fh													

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) TABLE 3-12.

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.

These registers can be addressed from any bank. 2:

These registers/bits are not implemented on PIC16(L)F1936 devices, read as '0'. 3:

4: Unimplemented, read as '1'.

5.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

5.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources

The oscillator module can be configured in one of eight clock modes.

- 1. ECL External Clock Low-Power mode (0 MHz to 0.5 MHz)
- 2. ECM External Clock Medium-Power mode (0.5 MHz to 4 MHz)
- 3. ECH External Clock High-Power mode (4 MHz to 32 MHz)
- 4. LP 32 kHz Low-Power Crystal mode.
- 5. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode (up to 4 MHz)
- 6. HS High Gain Crystal or Ceramic Resonator mode (4 MHz to 20 MHz)
- 7. RC External Resistor-Capacitor (RC).
- 8. INTOSC Internal oscillator (31 kHz to 32 MHz).

Clock Source modes are selected by the FOSC<2:0> bits in the Configuration Word 1. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The EC clock mode relies on an external logic level signal as the device clock source. The LP, XT, and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The RC clock mode requires an external resistor and capacitor to set the oscillator frequency.

The INTOSC internal oscillator block produces low, medium, and high frequency clock sources, designated LFINTOSC, MFINTOSC, and HFINTOSC. (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these three clock sources.

TABLE 10-3:	SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER
-------------	---

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCF	<3:0>		—	SCS	64	
STATUS	—	_	—	TO	PD	Z	DC	С	29
WDTCON	—				WDTPS<4:0>	>		SWDTEN	113

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8	_	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD	60
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE<1:0>			62		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	131	
CCPxCON	PxM<1:0>		DCxB<1:0>			CCPxM<3:0>				
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	142	
LCDCON	LCDEN	SLPEN	WERR	—	CS<	1:0>	LMUX	<1:0>	329	
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	333	
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	333	
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	142	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	301	
SSPCON1	WCOL	SSPOV	SSPEN	CKP		SSPM	<3:0>		287	
SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	286	
T1CON	TMR1C	S<1:0>	T1CKP	T1CKPS<1:0>		T1SYNC	_	TMR10N	203	
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	300	
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142	

|--|

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

12.5 PORTD Registers

PORTD is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISD (Register 12-14). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-1 shows how to initialize an I/O port.

Reading the PORTD register (Register 12-14) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATD).

Note:	PORTD is available on PIC16(L)F1934
	and PIC16(L)F1937 only.

The TRISD register (Register 12-15) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

12.5.1 ANSELD REGISTER

The ANSELD register (Register 12-17) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELD bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELD bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELD bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

12.5.2 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each PORTD pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 12-9.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in Table 12-9.

Pin Name	Function Priority ⁽¹⁾
RD0	COM3 (LCD) RD0
RD1	CCP4 (CCP) RD1
RD2	P2B (CCP) RD2
RD3	SEG16 (LCD) P2C (CCP) RD3
RD4	SEG17 (LCD) P2D (CCP) RD4
RD5	SEG18 (LCD) P1B (CCP) RD5
RD6	SEG19 (LCD) P1C (CCP) RD6
RD7	SEG20 (LCD) P1D (CCP) RD7

TABLE 12-9: PORTD OUTPUT PRIORITY

Note 1: Priority listed from highest to lowest.

13.6 Interrupt-On-Change Registers

REGISTER 13-1: IOCBP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	
bit 7							bit 0	
Legend:								
R = Readable b	bit	W = Writable I	bit	U = Unimplemented bit, read as '0'				
u = Bit is uncha	u = Bit is unchanged x = Bit is unknown			-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared					

bit 7-0

IOCBP<7:0>: Interrupt-on-Change Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-2: IOCBN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	
bit 7 bit 0								

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 IOCBN<7:0>: Interrupt-on-Change Negative Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-3: IOCBF: INTERRUPT-ON-CHANGE FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	
IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	
bit 7 bit 0								

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-0

IOCBF<7:0>: Interrupt-on-Change Flag bits

- 1 = An enabled change was detected on the associated pin.
 Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.
- 0 = No change was detected, or the user cleared the detected change.

23.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PRx is 255. The resolution is a function of the PRx register value as shown by Equation 23-4.

EQUATION 23-4: PWM RESOLUTION

Resolution =
$$\frac{\log[4(PRx+1)]}{\log(2)}$$
 bits

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

PWM Frequency	1.95 kHz	7.81 kHz	31.25 kHz	125 kHz	250 kHz	333.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 23-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 23-7: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

24.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 24-29).

24.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

24.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPIF bit is set (Figure 24-30).

24.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).









Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	302
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	98
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	99
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	102
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	301
SPBRGL				BRG	<7:0>				303*
SPBRGH				BRG<	:15:8>				303*
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142
TXREG	EUSART Transmit Data Register								293*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	300

TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Transmission.

* Page provides register information.

27.5 LCD Multiplex Types

The LCD driver module can be configured into one of four multiplex types:

- Static (only COM0 is used)
- 1/2 multiplex (COM<1:0> are used)
- 1/3 multiplex (COM<2:0> are used)
- 1/4 multiplex (COM<3:0> are used)

The LMUX<1:0> bit setting of the LCDCON register decides which of the LCD common pins are used (see Table 27-4 for details).

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, then the TRIS setting of that pin is overridden.

Multiplex	LMUX <1:0>	СОМЗ	COM2	COM1	
Static	00	Unused	Unused	Unused	
1/2	01	Unused	Unused	Active	
1/3	10	Unused	Active	Active	
1/4	11	Active	Active	Active	

TABLE 27-4: COMMON PIN USAGE

27.6 Segment Enables

The LCDSEn registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or as one of the pin's alternate functions. To configure the pin as a segment pin, the corresponding bits in the LCDSEn registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEn registers overrides any bit settings in the corresponding TRIS register.

Note: On a Power-on Reset, these pins are configured as normal I/O, not LCD pins.

27.7 Pixel Control

The LCDDATAx registers contain bits which define the state of each pixel. Each bit defines one unique pixel.

Register 27-6 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

27.8 LCD Frame Frequency

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

TABLE 27-5: FRAME FREQUENCY FORMULAS

Multiplex	Frame Frequency =
Static	Clock source/(4 x 1 x (LPD Prescaler) x 32))
1/2	Clock source/(2 x 2 x (LPD Prescaler) x 32))
1/3	Clock source/(1 x 3 x (LPD Prescaler) x 32))
1/4	Clock source/(1 x 4 x (LPD Prescaler) x 32))

Note: Clock source is Fosc/256, T1OSC or LFINTOSC.

TABLE 27-6: APPROXIMATE FRAME FREQUENCY (IN Hz) USING Fosc @ 8 MHz, TIMER1 @ 32.768 kHz OR LFINTOSC

LP<3:0>	Static	1/2	1/3	1/4
2	122	122	162	122
3 81		81	108	81
4 61		61	81	61
5	5 49		65	49
6 41		41	54	41
7 35		35	47	35

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For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 28-4 for more information.





30.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param No.	Sym.	Characteristic	Тур.	Units	Conditions		
TH01	θJA	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package		
			80	°C/W	28-pin SOIC package		
			90	°C/W	28-pin SSOP package		
			27.5	°C/W	28-pin UQFN 4x4mm package		
			27.5	°C/W	28-pin QFN 6x6mm package		
			47.2	°C/W	40-pin PDIP package		
			46	°C/W	44-pin TQFP package		
			24.4	°C/W	44-pin QFN 8x8mm package		
TH02	θJC	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package		
			24	°C/W	28-pin SOIC package		
			24	°C/W	28-pin SSOP package		
			24	°C/W	28-pin UQFN 4x4mm package		
			24	°C/W	28-pin QFN 6x6mm package		
			24.7	°C/W	40-pin PDIP package		
			14.5	°C/W	44-pin TQFP package		
			20	°C/W	44-pin QFN 8x8mm package		
TH03	TJMAX	Maximum Junction Temperature	150	°C			
TH04	PD	Power Dissipation	_	W	PD = PINTERNAL + PI/O		
TH05	PINTERNAL	Internal Power Dissipation	_	W	PINTERNAL = IDD x VDD ⁽¹⁾		
TH06	Pi/o	I/O Power Dissipation	_	W	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$		
TH07	Pder	Derated Power	_	W	Pder = PDmax (Τj - Τa)/θja ⁽²⁾		

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature

3: T_J = Junction Temperature

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28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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