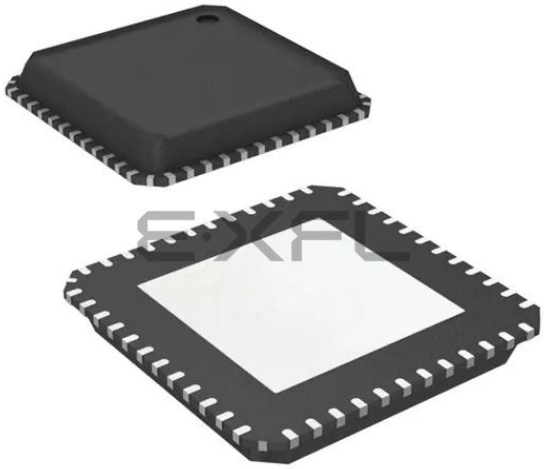

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3K x 8
Interface	SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9871qxa20xuma1

Table 1 Acronyms

Acronyms	Name
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PPB	Private Peripheral Bus
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit
ROM	Read Only Memory
SCU-DM	System Control Unit - Digital Modules
SCU-PM	System Control Unit - Power Modules
SFR	Special Function Register
SOW	Short Open Window (for WDT)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
STM	Store Instruction
SWD	ARM Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
VPRE	Pre Regulator
WDT	Watchdog Timer in SCU-DM
WDT1	Watchdog Timer in SCU-PM
WMU	Wake-up Management Unit
100TP	100 Time Programmable

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
P2				**Port 2** Port 2 is a 5-bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0/XTAL1	29	I/I	I	AN0 ADC analog input 0 Alternate function mapping see **Table 10**
P2.2/XTAL2	30	I/O	I	AN2 ADC analog input 2 Alternate function mapping see **Table 10**
P2.3	35	I	I	AN3 ADC analog input 3 Alternate function mapping see **Table 10**
P2.4	32	I	I	AN4 ADC analog input 4 Alternate function mapping see **Table 10**
P2.5	31	I	I	AN5 ADC analog input 5 Alternate function mapping see **Table 10**
Power Supply				
VS	45	P	–	Battery supply input
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.
VDDC	38	P	–	[3)]Core supply (1.5 V during Active Mode). Do not connect external loads, connect external buffer capacitor.
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)
GND	19	P	–	GND digital
GND	28	P	–	GND digital
GND	39	P	–	GND analog
Monitor Input				
MON	14	I	–	High Voltage Monitor Input
PWM Interface				
PWM_IO	43	I/O	–	PWM interface input/output
GND_PWM	42	P	–	PWM ground
Charge Pump				
CP1H	48	P	–	Charge Pump Capacity 1 High, connect external C
CP1L	1	P	–	Charge Pump Capacity 1 Low, connect external C
CP2H	3	P	–	Charge Pump Capacity 2 High, connect external C
CP2L	4	P	–	Charge Pump Capacity 2 Low, connect external C
VCP	2	P	–	Charge Pump Capacity
VSD	47	P	–	Battery supply input for Charge Pump
MOSFET Driver				
VDH	44	P	–	Voltage Drain High Side MOSFET Driver
SH3	46	P	–	Source High Side FET 3
SH2	6	P	–	Source High Side FET 2

5.3 Power Supply Generation Unit (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. PWM Interface).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (Undervoltage Reset, V_{DDPUV})
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

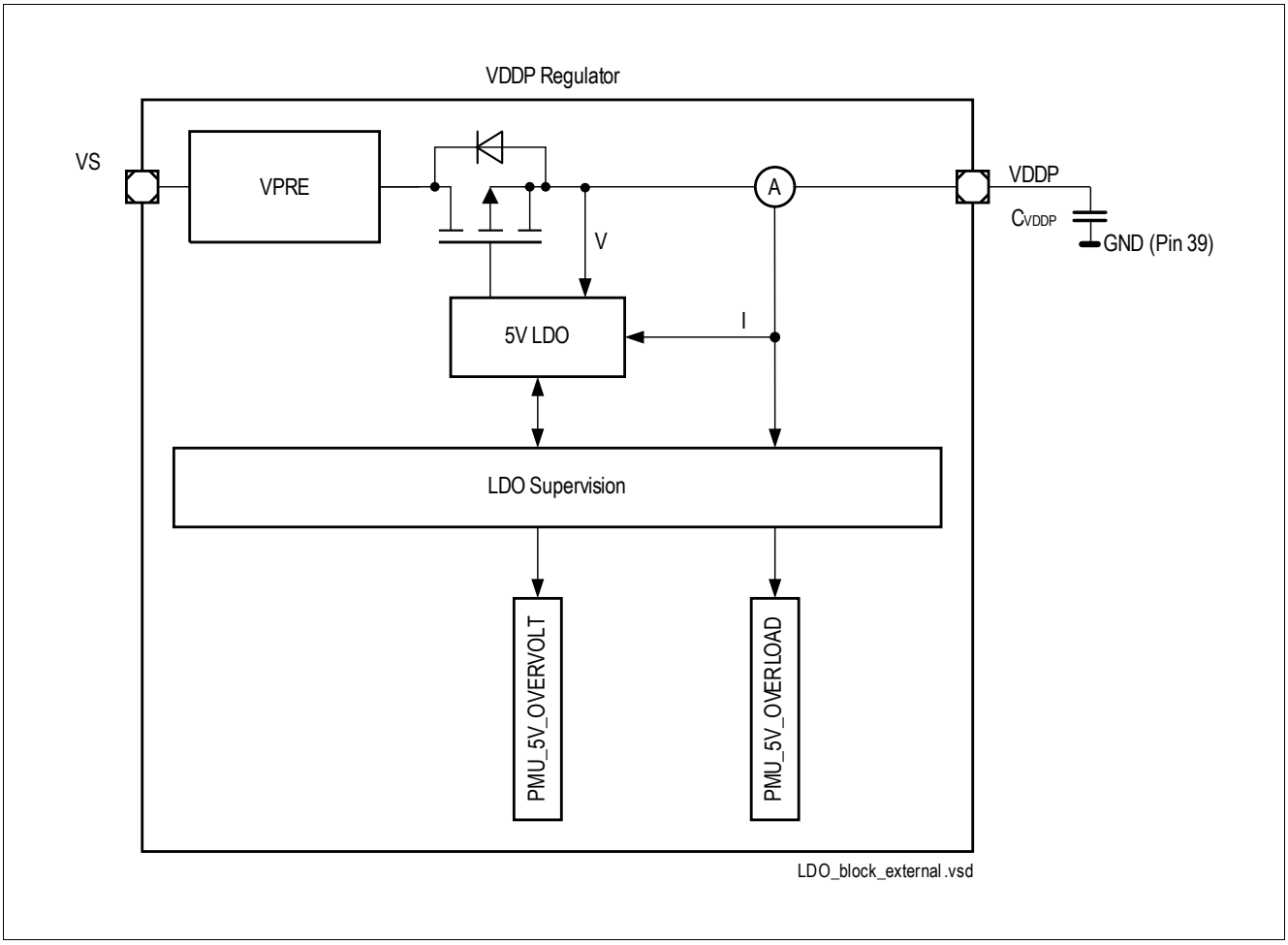

Figure 5 Module Block Diagram of VDDP Voltage Regulator

Table 5 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

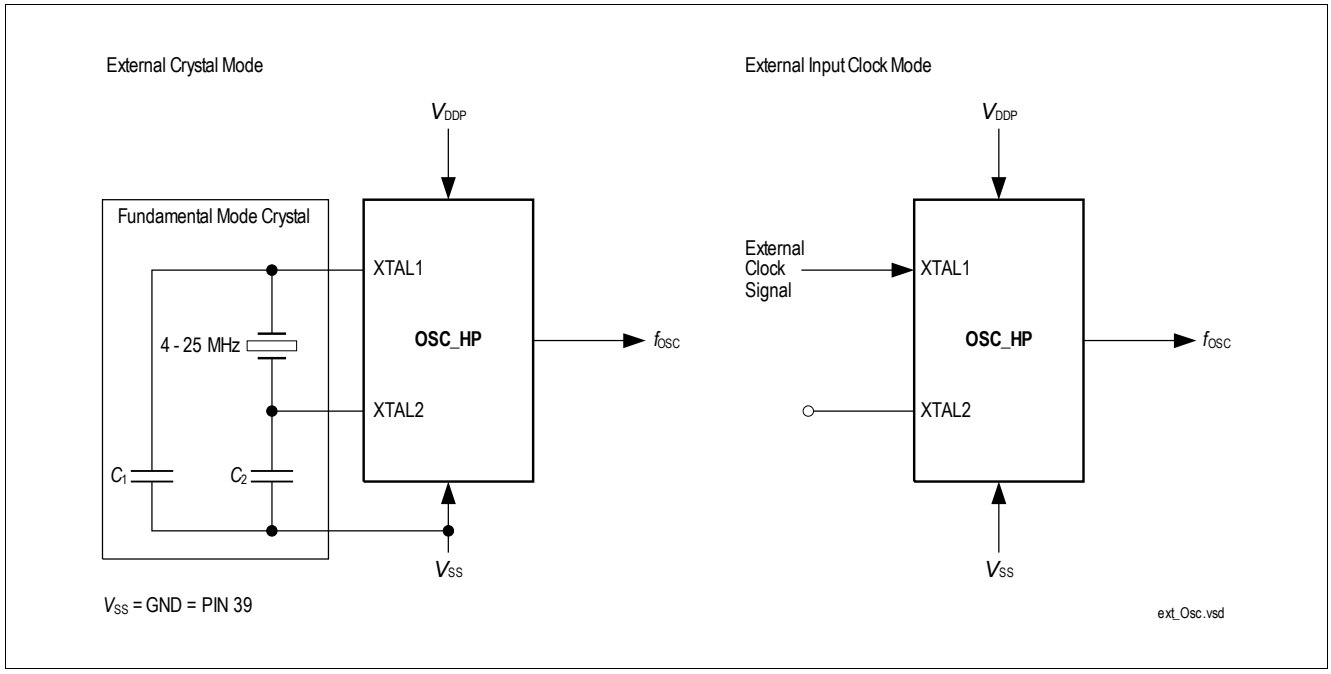

Figure 10 TLE9871QXA20 External Circuitry for the OSC_HP

8.2.1 Block Diagram

Figure 12 shows the functional blocks of the Cortex M3.

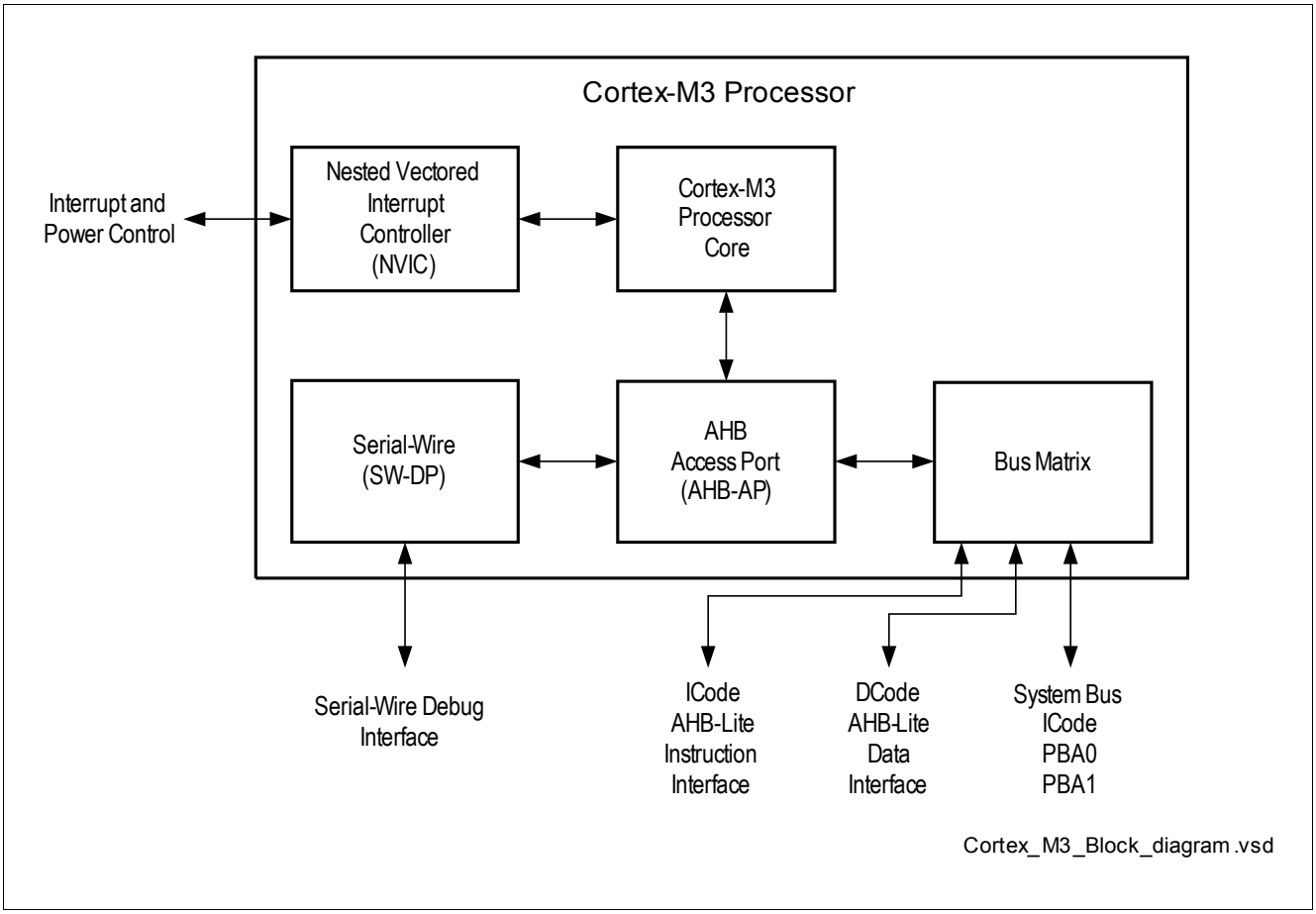

Figure 12 Cortex M3 Block Diagram

9.3 Functional Description

9.3.1 DMA Mode Overview

The DMA controller implements the following 13 hardware DMA requests:

- ADC1 complete sequence 1 done: DMA transfer is requested on completion of the ADC1 channel conversion sequence.
- ADC1 exceptional sequence 2 (ESM) done: DMA transfer is requested on completion of the ADC1 conversion sequence triggered by an exceptional measurement request.
- SSC1/2 transmit byte: DMA transfer is requested upon the completion of data transmission via SSC1/2
- SSC1/2: receive byte: DMA transfer is requested upon the completion of data reception via SSC1/2.
- ADC1 channel 0 conversion done: DMA transfer is requested on completion of the ADC1 channel 0 conversion.
- ADC1 channel 1 conversion done: DMA transfer is requested on completion of the ADC1 channel 1 conversion.
- ADC1 channel 2 conversion done: DMA transfer is requested on completion of the ADC1 channel 2 conversion.
- ADC1 channel 3 conversion done: DMA transfer is requested on completion of the ADC1 channel 3 conversion.
- ADC1 channel 4 conversion done: DMA transfer is requested on completion of the ADC1 channel 4 conversion.
- ADC1 channel 5 conversion done: DMA transfer is requested on completion of the ADC1 channel 5 conversion.
- ADC1 channel 6 conversion done: DMA transfer is requested on completion of the ADC1 channel 6 conversion.
- ADC1 channel 7 conversion done: DMA transfer is requested on completion of the ADC1 channel 7 conversion.
- Timer3 ccu6_int: DMA transfer is requested following a timer trigger.

11 Memory Control Unit

11.1 Features

- Handles all system memories and their interaction with the CPU
- Memory protection functions for all system memories (D-Flash, P-Flash, RAM)
- Address management with access violation detection including reporting
- Linear address range for all memories (no paging)

11.2 Introduction

11.2.1 Block Diagram

The Memory Control Unit (MCU) is divided in the following sub-modules:

- NVM Memory module (embedded Flash Memory)
- RAM memory module
- BootROM memory module
- Memory Protection Unit (MPU) module

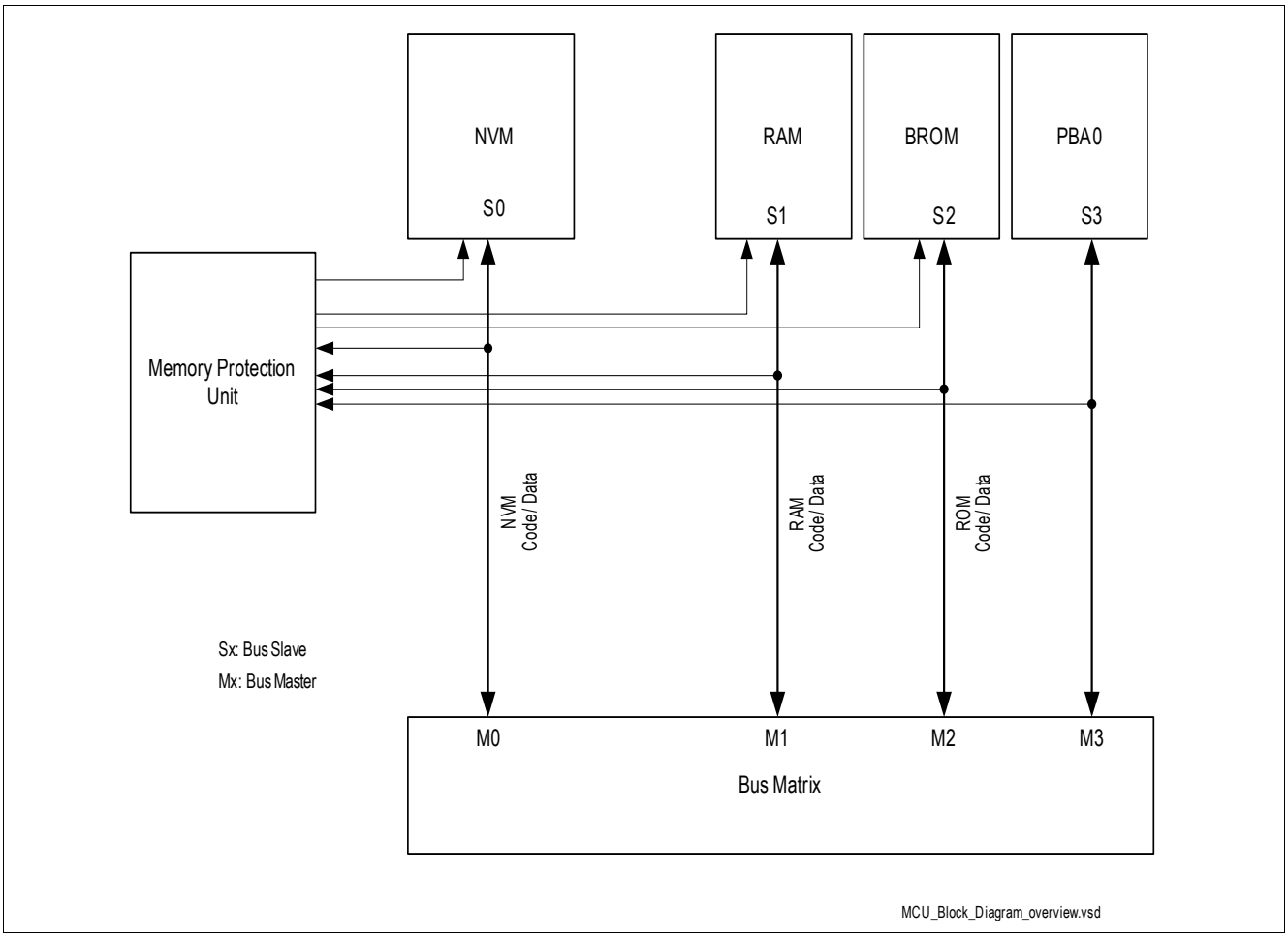

Figure 15 MCU Block View

14 GPIO Ports and Peripheral I/O

The TLE9871QXA20 has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 17 shows the block diagram of an TLE9871QXA20 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open drain pin with or without internal pull-up/pull-down device.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output mode at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined in registers

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer 21
P1.1	Input	GPI	P1_DATA.P1	
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	-
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer 21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2_0	UART2
P1.2	Input	GPI	P1_DATA.P2	
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer 2
		INP3	T21EX_3	Timer 21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

17 Timer3

17.1 Features

- 16-bit incremental timer/counter (counting up)
- Counting frequency up to f_{sys}
- Selectable clock prescaler
- 6 modes of operation
- Interrupt up on overflow
- Interrupt on compare

17.2 Introduction

The possible applications for the timer include measuring the time interval between events, counting events and generating a signal at regular intervals.

Timer3 can function as timer or counter. When functioning as a timer, Timer3 is incremented in periods based on the MI_CLK or LP_CLK clock. When functioning as a counter, Timer3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer3 can be configured in four different operating modes to use in a variety of applications, see **Table 12**.

Several operating modes can be used for different tasks such as the following:

- simple time measurement between two events
- triggering of the measuring unit upon PWM/CCU6 unit
- measurement of the 100kHz LP_CLK2

17.3 Functional Description

Six modes of operation are provided to fulfill various tasks using this timer. In every mode the clocking source can be selected between MI_CLK and LP_CLK. A prescaler provides in addition capability to divide the selected clock source by 2, 4 or 8. The timer counts upwards, starting with the value in the timer count registers, until the maximum count value which depends on the selected mode of operation. Timer 3 provides two individual interrupts upon counter overflow, one for the low-byte and one for the high-byte counter register.

17.3.1 Timer3 Modes Overview

The following table provides an overview of the timer modes together with the reasonable configuration options in **Table 12**.

Table 12 Timer3 Modes

Mode	Sub-Mode	Operation
0	**No Sub-Mode**	**13-bit Timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler.
1	**a**	**16-bit Timer** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter.
1	**b**	**16-bit Timer triggered by an event** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter, which is triggered by an event to enable a single shot measurement on a preset channel with the measurement unit.

18 Capture/Compare Unit 6 (CCU6)

18.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

18.2 Introduction

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive DC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide efficient software-control.

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

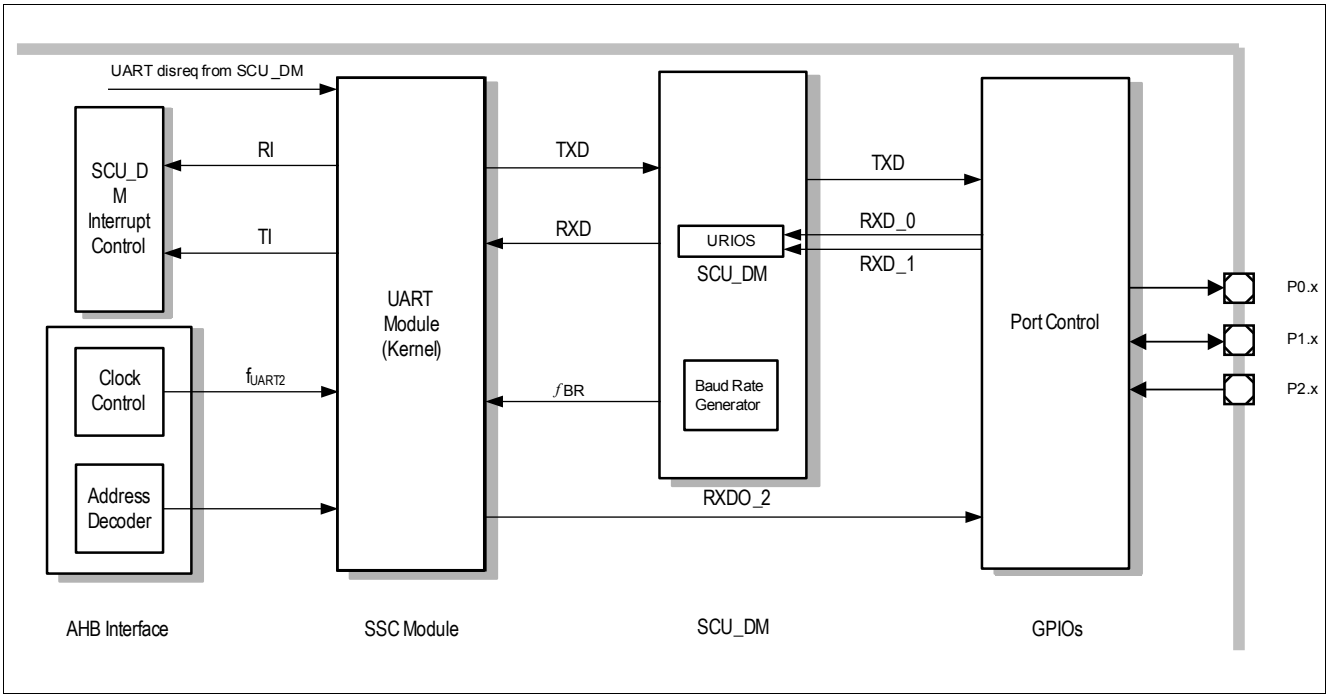

Figure 22 UART Block Diagram

24.2.1 Block Diagram

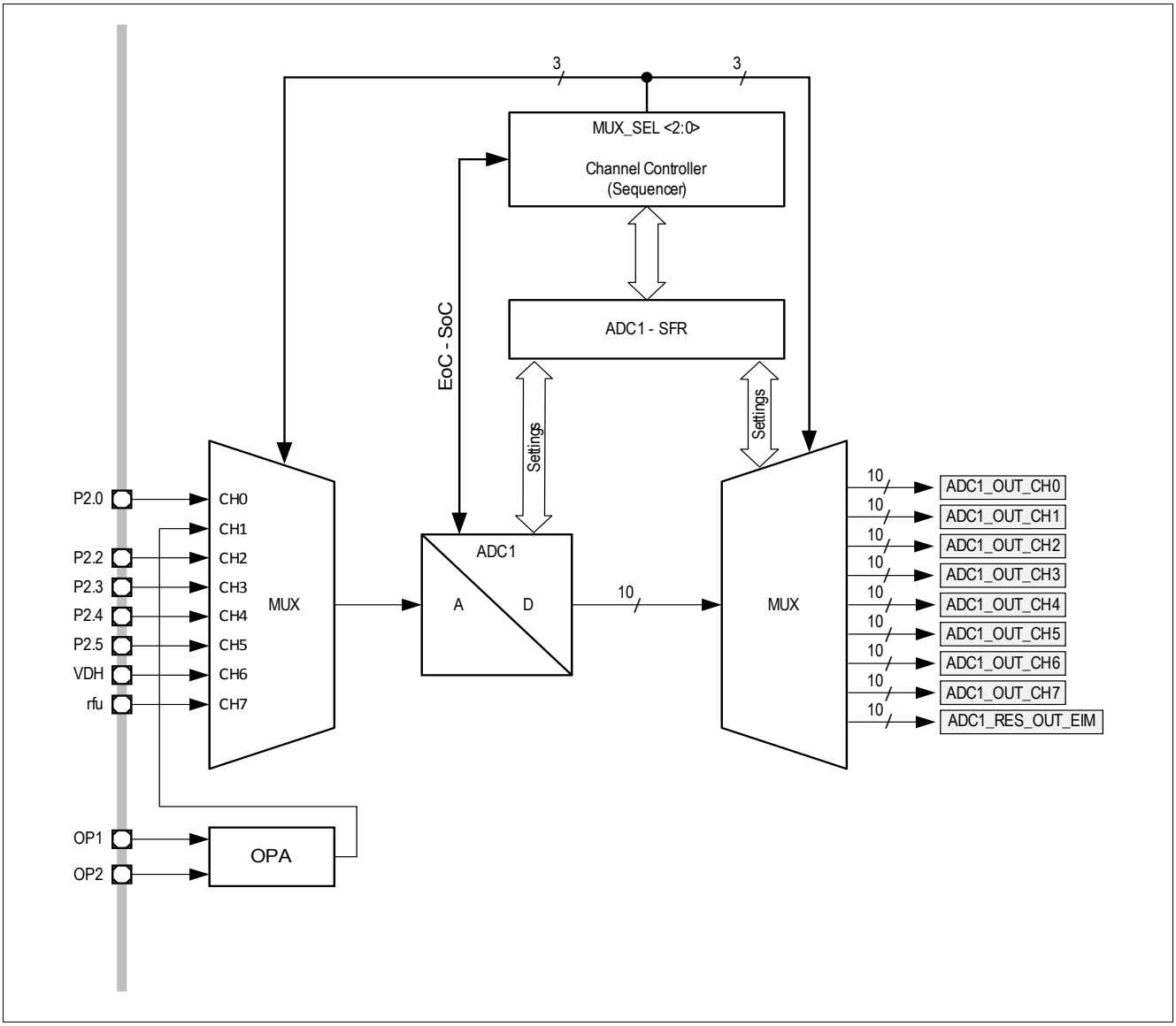

Figure 28 ADC1 Top Level Block Diagram

As shown in the figure above, the ADC1 postprocessing consists of a channel controller (Sequencer) and an 8-channel demultiplexer. The channel control block controls the multiplexer sequencing on the analog side before the ADC1 and on the digital domain after the ADC1. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to give a higher priority to some channels compared to the other channel measurements.

26.2.1 Block Diagram

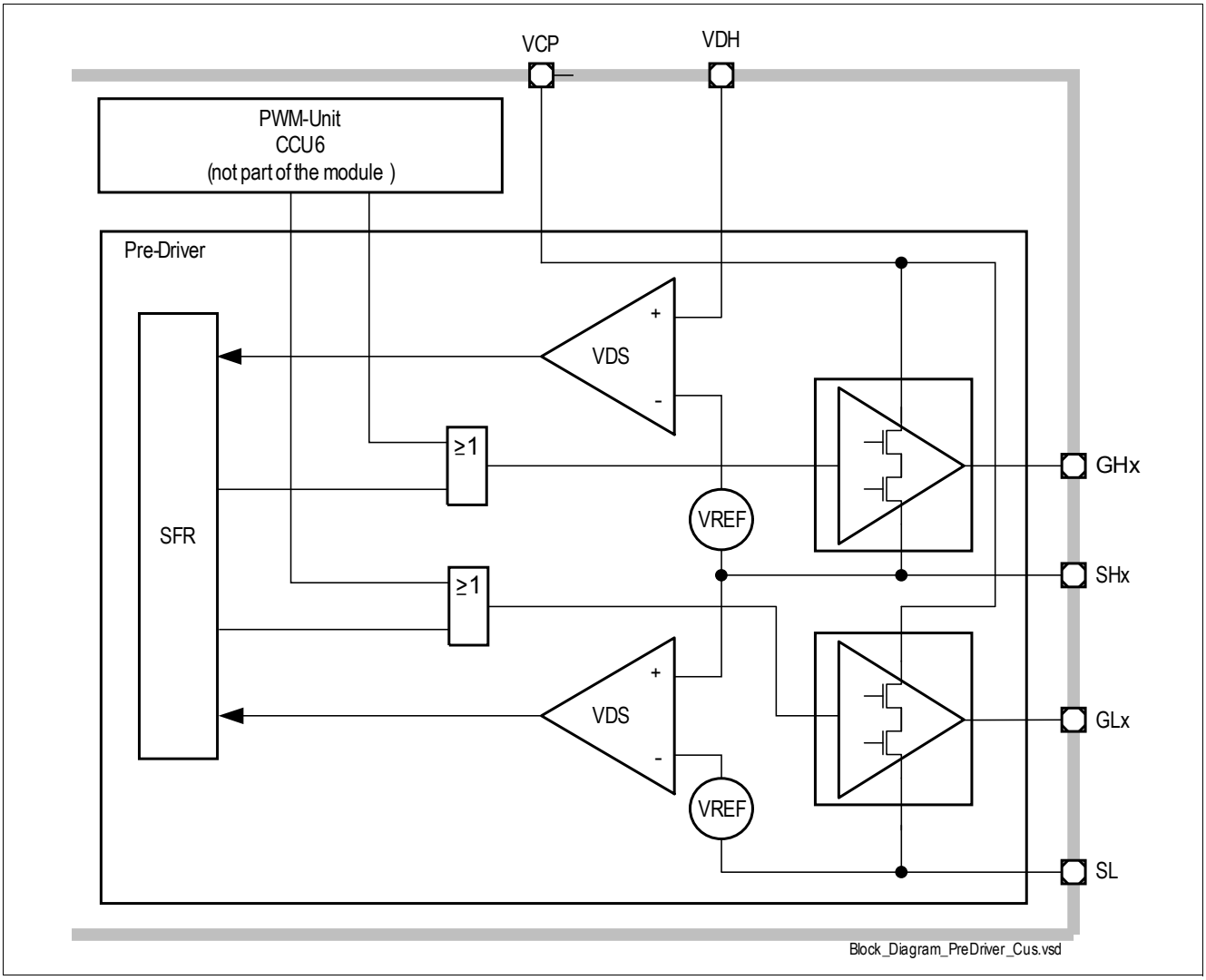

Figure 30 Driver Module Block Diagram (incl. system connections)

26.2.2 General

The Driver can be controlled in two different ways:

- In Normal Mode the output stage is fully controllable through the SFR registers CTRLx (x = 1,2,3). Protection functions such as overcurrent and open-load detection are available.
- The PWM Mode can also be enabled by the corresponding bit in CTRL1 and CTRL2. The PWM must be configured in the System PWM Module (CCU6). All protection functions are available in PWM mode as well.

Protection Functions

- Overcurrent detection and shutdown feature for external MOSFET by Drain Source measurement
- Programmable minimum cross current protection time
- Open-load detection feature in Off-state for external MOSFET.

Table 17 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage range at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	–	48	V	7)	P_1.1.15
Voltages – GPIOs							
Voltage on any port pin	V_{in}	-0.3	–	V_{DDP} +0.3	V	$V_{IN} < V_{DDPmax}$ 8)	P_1.1.16
Current at VCP Pin							
Max. current at VCP pin	I_{VCP}	-15	–	–	mA	–	P_1.1.35
Injection Current at GPIOs							
Injection current on any port pin	I_{GPIONM}	-5	–	5	mA	9)	P_1.1.34
Sum of all injected currents in Normal Mode	I_{GPIOAM_sum}	-50	–	50	mA	9)	P_1.1.30
Sum of all injected currents in Power Down Mode (Stop Mode)	I_{GPIOPD_sum}	-5000	–	50	µA	9)	P_1.1.36
Sum of all injected currents in Sleep Mode	$I_{GPIOSleep\_sum}$	-5	–	5	mA	9)	P_1.1.37
Other Voltages							
Input voltage VAREF	V_{AREF}	-0.3	–	V_{DDP} +0.3	V	–	P_1.1.17
Input voltage OP1, OP2	V_{OAI}	-7	–	7	V	–	P_1.1.23
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_1.1.18
Storage temperature	T_{stg}	-55	–	150	°C	–	P_1.1.19
ESD Susceptibility							
ESD susceptibility all pins	V_{ESD1}	-2	–	2	kV	HBM 10)	P_1.1.20
ESD susceptibility pins MON, VS, VSD vs.GND	V_{ESD2}	-4	–	4	kV	HBM 11)	P_1.1.21
ESD susceptibility pins PWM_IO vs. GND_PWM	V_{ESD3}	-6	–	6	kV	HBM 10)	P_1.1.22
ESD susceptibility **CDM** all pins vs. GND	V_{ESD_CDM1}	-500	–	500	V	12)	P_1.1.28
ESD susceptibility **CDM** pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) vs. GND	V_{ESD_CDM2}	-750	–	750	V	12)	P_1.1.43

1) Not subject to production test, specified by design.

2) Conditions and min. value is derived from application condition for reverse polarity event.

3) Min voltage -28V with external 3.9kΩ series resistor only.

Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	110	µA	T_J = -40°C to 85°C; V_S = 5.5 V to 18V; t_{Cyclic_ON} = 4ms; t_{Cyclic_OFF} = 2048 ms;2)	P_1.3.4
Current consumption in Stop Mode	I_{Stop}	–	100	150	µA	System in Stop Mode, microcontroller not clocked, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_S = 5.5V to 18V	P_1.3.10

1) Current on V_S, ADC1/2 active, timer running, PWM interface active (recessive).

2) Incl. leakage currents form VDH, VSD and MON

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

1) The typical oscillator frequency is 5 MHz
2) V_{DDC} = 1.5 V, T_j = 25°C
3) Not subject to production test, specified by design.
4) This parameter is valid for PLL operation with an external clock source and thus reflects the real PLL performance.

29.4 Flash Memory

This chapter includes the parameters for the 36 kByte embedded flash module.

29.4.1 Flash Parameters

Table 28 Flash Characteristics[1)]

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.9
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[4)]Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.6

1) Not subject for production test, specified by design.
2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.
3) Derived by extrapolation of lifetime tests.
4) Temperature: 25 °C
5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

Table 30 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) I_{OL} ≤ I_{OLmax}	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) I_{OL} ≤ I_{OLnom}	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) I_{OH} ≥ I_{OHmax}	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) I_{OH} ≥ I_{OHnom}	P_5.1.9
Input leakage current	I_{OZ2}	-5	–	+5	µA	6) T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	T_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

5) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.

6) The given values are worst-case values. In production tests, this leakage current is only tested at 150°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

29.11 High-Voltage Monitoring Input

29.11.1 Electrical Characteristics

Table 39 Electrical Characteristics Monitoring Input

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MON Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_S	0.5*V_S	0.6*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V; T_J = -40°C to 85°C	P_11.1.1
Wake-up/monitoring threshold voltage extended range	V_{MONth_extend}	0.44*V_S	0.53*V_S	0.64*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s)	P_11.1.11
Threshold hysteresis	$V_{MONth,hys}$	0.015*V_S	0.05*V_S	0.1*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V;	P_11.1.12
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_S	0.06*V_S	0.12*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 18V to 28V;	P_11.1.2
Pull-up current	$I_{PU, MON}$	-20	-10	-1	µA	0.6*V_S	P_11.1.3
Pull-down current	$I_{PD, MON}$	3	10	20	µA	0.4*V_S	P_11.1.4
Input leakage current	$I_{LK,MON}$	-2.5	–	2.5	µA	[1] 0 V < V_{MON_IN} < 28 V	P_11.1.5
Timing							
Wake-up filter time (internal analog filter delay)	$t_{FT,MON}$	–	500	–	ns	[2] The overall filter time for MON wake-up is a sum of $t_{FT,MON}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_MON_FT;	P_11.1.6

1) Input leakage is valid for disabled state.

2) With pull-up, pull down current disabled.

Table 40 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Open load diagnosis currents							
Pull-up diagnosis current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnosis current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin1}	8.5	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, Bridge Driver enabled	P_12.1.53
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V < V_{VSD} < 28, I_{CP}=10mA, @250kHz f_{CP}	P_12.1.49
Turn ON Time	t_{ON_VCP}	80	88	120	us	8 V < V_{VSD} < 28, (25%)[2)6)], C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250kHz	P_12.1.59
Rise time	t_{rise_VCP}	60	72	88	us	8 V < V_{VSD} < 28, (25-75%)[2)7)], C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250kHz	P_12.1.60

1) Specification for BLDC Drive, 6 MOSFET switching with 25 KHz. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.
2) Not subject to production test.
3) This resistance is connected through a diode between SHx and GHx to ground.
4) ICHARGE = IDISCHARGE = 3(min).
5) ICHARGE = IDISCHARGE = 31(max).
6) This time applies when Bit DRV_CP_CTRL_STS.bit.CP_EN is set
7) This time applies when Bit DRV_CP_CLK_CTRL.bit.CPCLK_EN is set