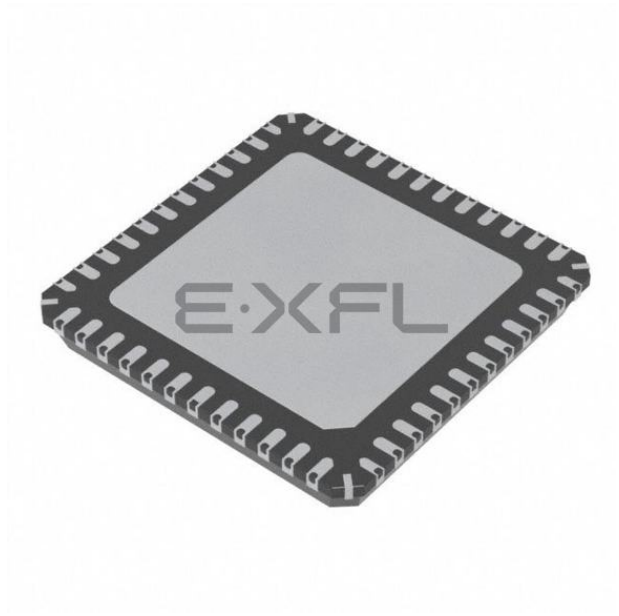

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3K x 8
Interface	SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9871qxa20xuma2

1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
CP	Charge Pump for MOSFET driver
CSA	Current Sense Amplifier
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIM	Exceptional Interrupt Measurement
FSM	Finite State Machine
GPIO	General Purpose Input Output
H-Bridge	Half Bridge
ICU	Interrupt Control Unit
IEN	Interrupt Enable
IIR	Infinite Impulse Response
LDM	Load Instruction
LDO	Low DropOut voltage regulator
LSB	Least Significant Bit
LTI	Lead Tip Inspection
MCU	Micro Controller Unit
MF	Measurement Functions
MSB	Most Significant Bit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MTSR	Master Transmit Slave Receive
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OTP	One Time Programmable
OSC	Oscillator
PBA	Peripheral Bridge
PCU	Power Control Unit

Sleep Mode is activated after 5 consecutive watchdog failures or in case of supply failure (5 times). In this case, MON is enabled as the wake source and Cyclic Wake-Up is activated with 1s of wake time.

Sleep Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Sleep Mode. The transition to Cyclic Wake-Up Mode is performed by first setting the corresponding bits in the mode control register followed by the Sleep and Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (PWM interface and/or MON) are available, as in normal Sleep Mode.

When using Sleep Mode with cyclic wake-up the voltage regulator is switched off and started again with the wake. A limited number of registers is buffered during sleep, and can be used by SW e.g. for counting sleep/wake cycles.

MCU Slow Down Mode

In MCU Slow Down Mode the MCU frequency is reduced for saving power during operation. PWM communication is still possible. LS MOSFET can be activated.

Wake-Up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. This is to ensure that no wake-up event is lost.

As default wake-up source, the MON input is activated after power-on reset only. Additionally, the device is in Cyclic Wake-Up Mode with the max. configurable dead time setting.

The following table shows the possible power mode configurations including the Stop Mode.

Table 3 Power Mode Configurations

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
VDDEXT	ON/OFF	ON (no dynamic load)/OFF	OFF	–
Bridge Driver	ON/OFF	OFF	OFF	
PWM TRx	ON/OFF	wake-up only/ OFF	wake-up only/ OFF	–
VS sense	ON/OFF brownout detection	brownout detection	POR on VS	brownout det. done in PCU
GPIO 5V (wake-up)	n.a.	disabled/static	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ OFF	–
Measurement	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/STOP	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–

Table 3 Power Mode Configurations (cont'd)

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
LP_CLK (18 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON/OFF	ON/OFF	ON/OFF	for cyclic wake-up

1) May not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by PWM interface or by cyclic wake-up.

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

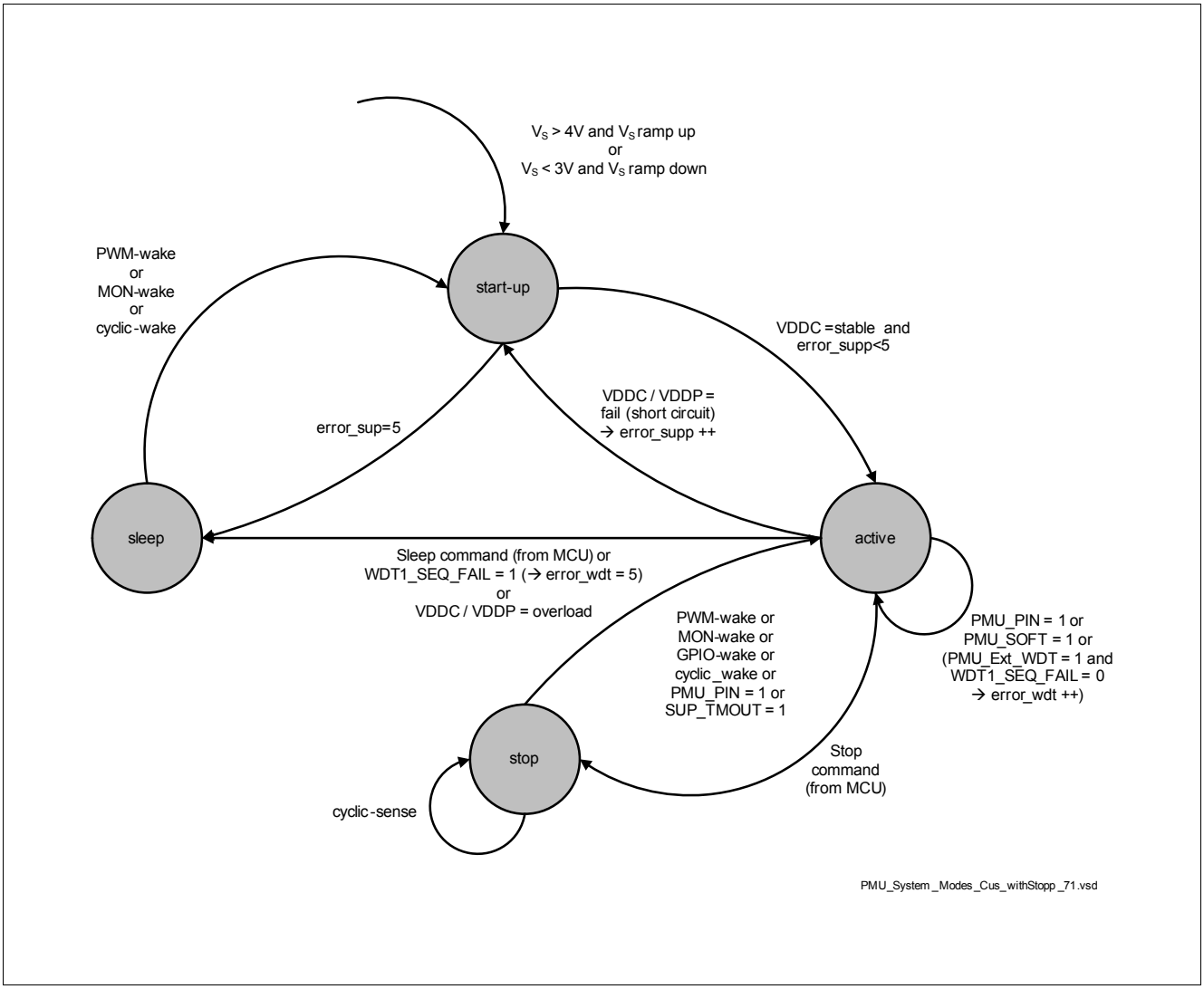

Figure 4 Power Management Unit System Modes

5.3 Power Supply Generation Unit (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. PWM Interface).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (Undervoltage Reset, V_{DDPUV})
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

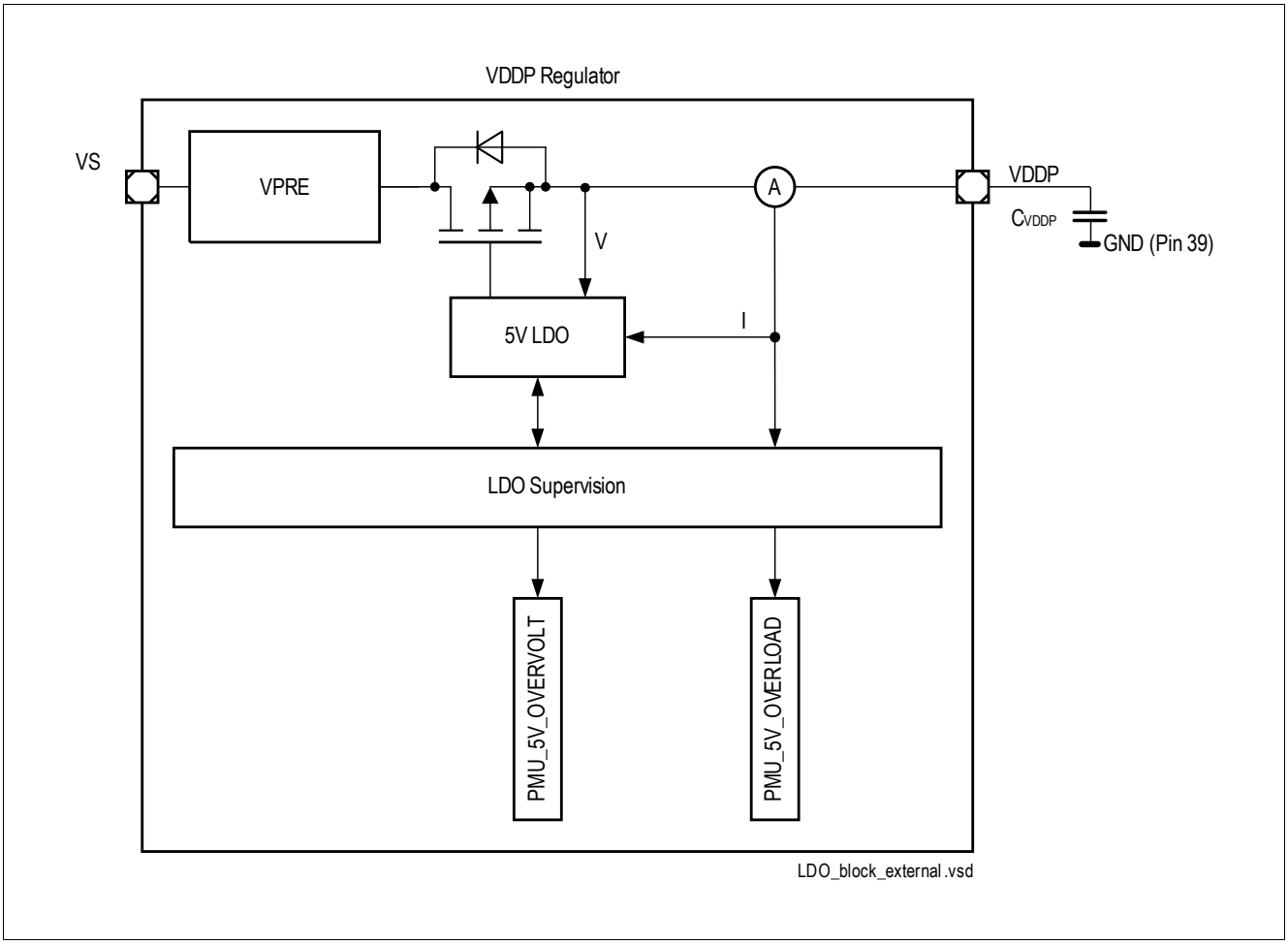

Figure 5 Module Block Diagram of VDDP Voltage Regulator

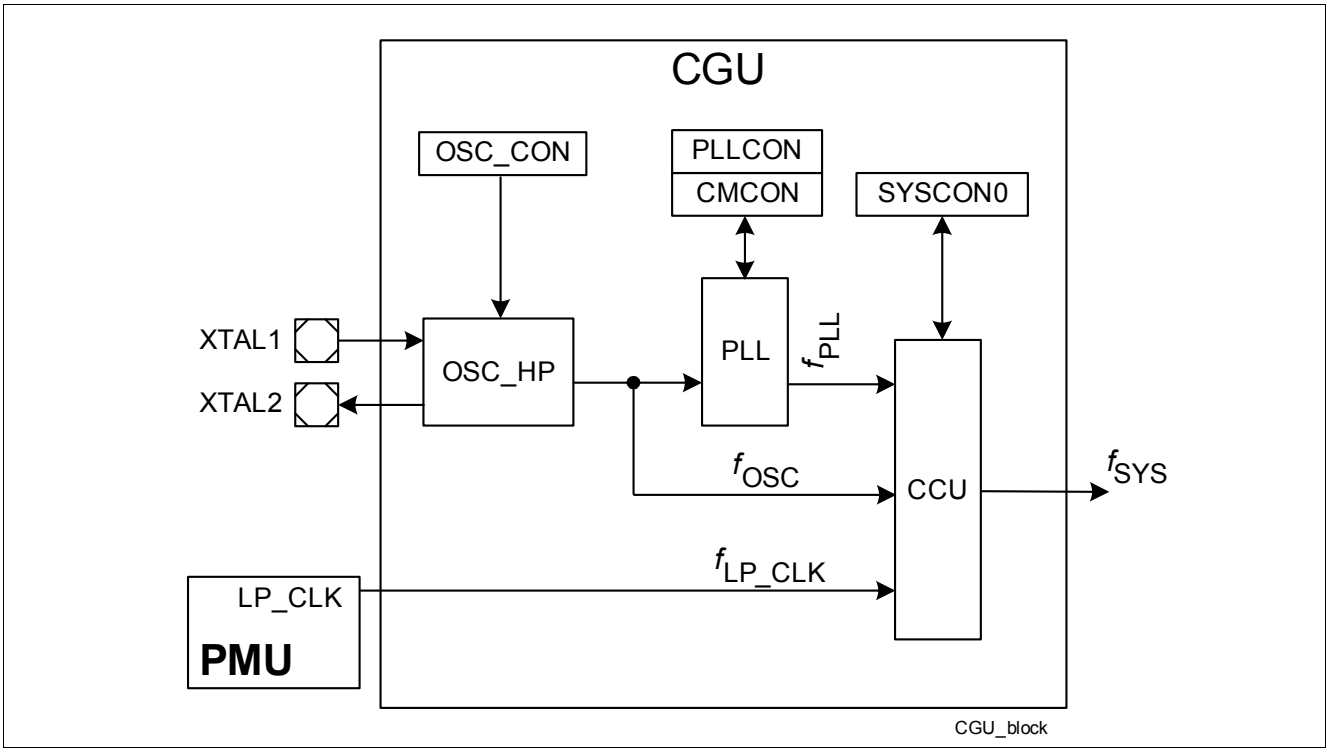

Figure 9 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9871QXA20 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user configurable.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input, and XTAL2 as the output.

Figure 10 shows the recommended external circuitry for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal to or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal, it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It normally consists of the two load capacitances C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative resistance method. The following load cap values can be used as starting point for the evaluation:

12 Interrupt System

12.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

12.2 Introduction

12.2.1 Overview

The TLE9871QXA20 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, DMA, Bridge Driver and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 6 Interrupt Vector Table

Service Request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU- ADC8/T3	2	Measurement Unit, VBG, Timer3, BEMF
ADC1	3	ADC1 interrupt / VREF5V Overload / VREF5V OV/UV, 10-bit ADC
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 interrupt (receive, transmit), Timer2, PWM-Interface
UART2	11	UART2 interrupt (receive, transmit), Timer21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge Driver / Charge Pump
DMA	15	DMA Controller

Table 7 NMI Interrupt Table

Service Request	Node	Description
Watchdog Timer NMI	NMI	Watchdog Timer overflow
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature

Table 7 NMI Interrupt Table

Service Request	Node	Description
Oscillator Watchdog NMI	NMI	Oscillator Watchdog / MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

14 GPIO Ports and Peripheral I/O

The TLE9871QXA20 has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 17 shows the block diagram of an TLE9871QXA20 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open drain pin with or without internal pull-up/pull-down device.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output mode at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined in registers

Px_ALTSEL0 and Px_ALTSEL1. When a port pin is used as an alternate function, its direction must be set accordingly in the register Px_DIR.

Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register Px_PUDSEL selects whether a pull-up or the pull-down device is activated while register Px_PUDEN enables or disables the pull device.

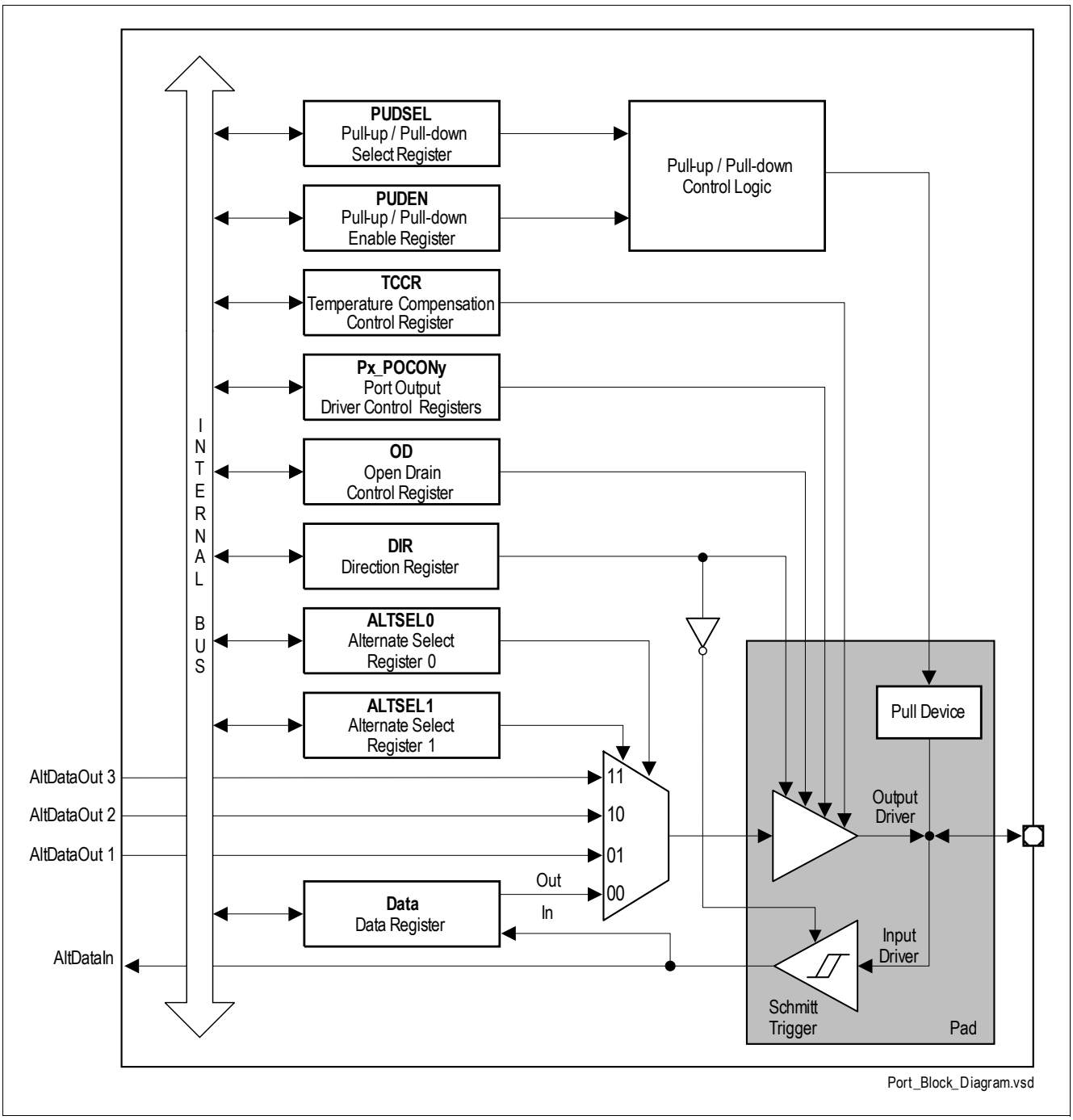

Figure 17 General Structure of Bidirectional Port (P0, P1)

14.2.2 Port 2

Figure 18 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

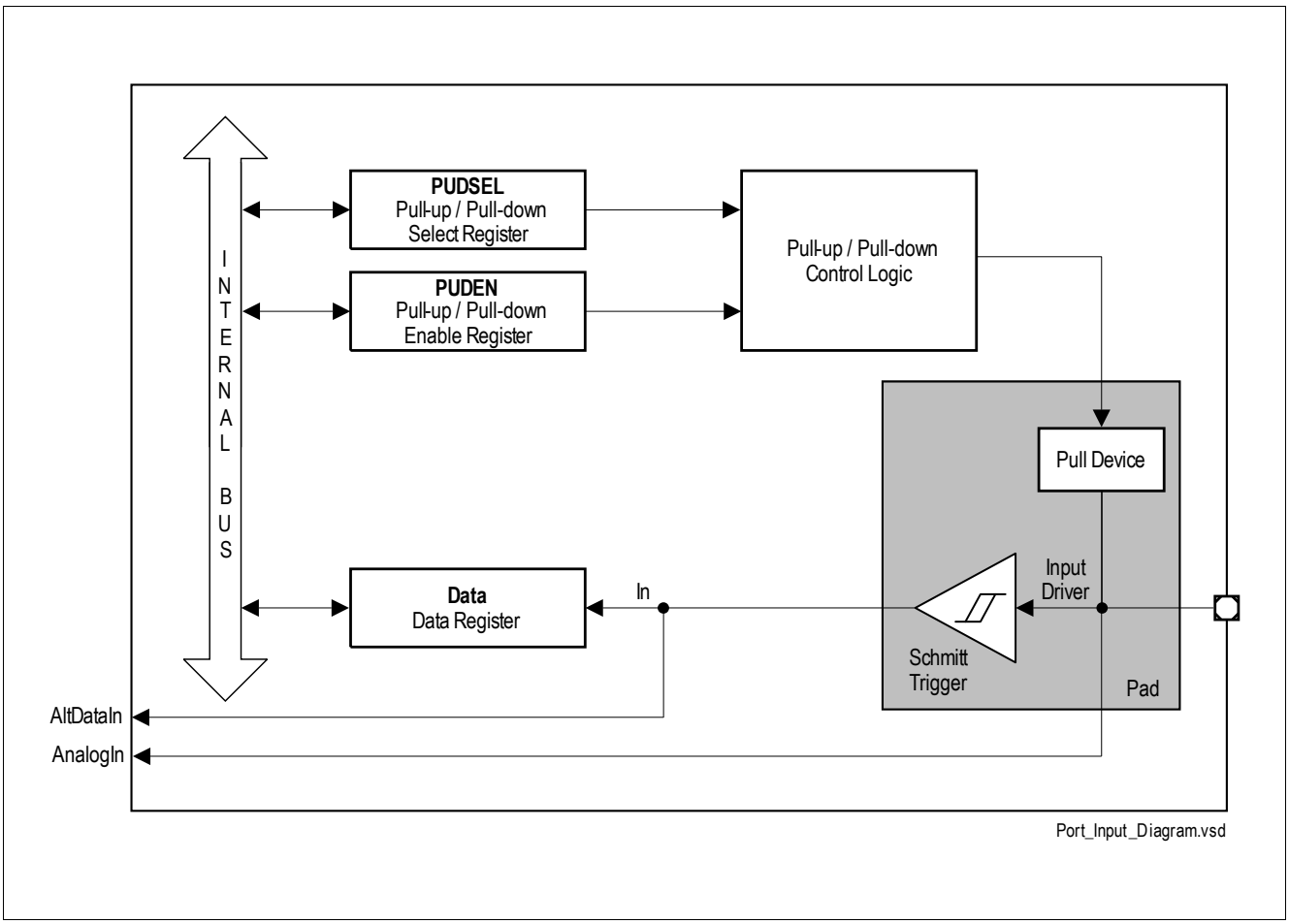

Figure 18 General Structure of Input Port (P2)

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer 21
P1.1	Input	GPI	P1_DATA.P1	
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	-
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer 21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2_0	UART2
P1.2	Input	GPI	P1_DATA.P2	
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer 2
		INP3	T21EX_3	Timer 21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

Table 9 Port 1 Input / Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.3	Input	GPI	P1_DATA.P3	
		INP1	T6INB	GPT12T6
		INP2	–	
		INP3	CC62_0	CCU6
		INP4	T6EUDB	GPT12T6
		INP5	–	
		INP6	CCPOS0_2	CCU6
		INP7	EXINT1_1	SCU
	Output	GPO	P1_DATA.P3	
		ALT1	EXF21_1	Timer 21
		ALT2	CC62_0	CCU6
		ALT3	TXD2_1	UART2
P1.4	Input	GPI	P1_DATA.P4	
		INP1	EXINT2_1	SCU
		INP2	T21EX_1	Timer 21
		INP3	T5EUDA	GPT12T5
		INP4	RxD1	UART1
		INP5	T2INB	GPT12T2
		INP6	CCPOS1_2	CCU6
		INP7	MRST_1_3	SSC1
	Output	GPO	P1_DATA.P4	
		ALT1	CLKOUT_1	SCU
		ALT2	COUT62_0	CCU6
		ALT3	RxD1	UART1 / PWM_RxD

Table 12 Timer3 Modes (cont'd)

Mode	Sub-Mode	Operation
2	**No Sub-Mode**	**8-bit Timer with auto-reload** The timer register TL3 is reloaded with a user-defined 8-bit value in TH3 upon overflow.
3	**a**	**Timer3 operates as two 8-bit timers** The timer registers TL3 and TH3, operate as two separate 8-bit counters.
3	**b**	**Timer3 operates as Two 8-bit timers for clock measurement** The timer registers, TL3 and TH3 operate as two separate 8-bit counters. In this mode the LP_CLK2 Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as a counter which counts the time between the edges.

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

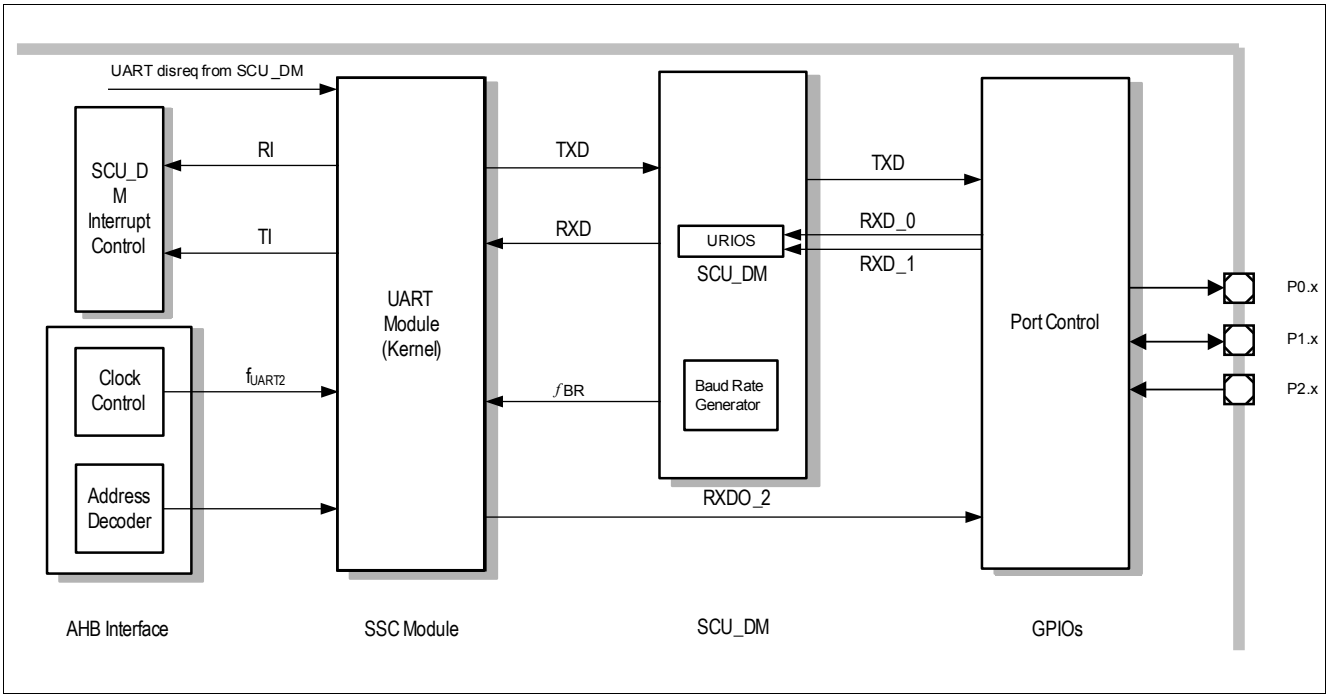

Figure 22 UART Block Diagram

Table 15 External Components (BOM)

Symbol	Function	Component
C_{VS1}	Blocking capacitor at VS pin	≥ 100 nF Ceramic, ESR < 1Ω
C_{VS2}	Blocking capacitor at VS pin	> 2.2 µF Elco[1)]
C_{VDDP}	Blocking capacitor at VDDP pin	470 nF + 100 nF Ceramic, ESR < 1Ω
C_{VDD_EXT}	Blocking capacitor at VDDEXT pin	100nF, Ceramic ESR < 1Ω
C_{VDDC}	Blocking capacitor at VDDC pin	470 nF + 100 nF Ceramic, ESR < 1Ω
C_{VAREF}	Blocking capacitor at VAREF pin	100 nF, Ceramic ESR < 1Ω
C_{PWM_IO}	Standard C for PWM Interface slave	–
C_{VSD}	Filter C for charge pump end driver	1 µF
C_{CPS1}	Charge pump capacitor	220 nF
C_{CP2S}	Charge pump capacitor	220 nF
C_{VCP}	Charge pump capacitor	470 nF
C_{MON}	Filter C for ISO pulses	10nF
C_{VDH}	Capacitor	3.3 nF
C_{PH1}	Capacitor	220 µF
C_{PH2}	Capacitor	220 µF
C_{PH3}	Capacitor	220 µF
$C_{OPAFILT}$	Capacitor	100 nF
C_{EMCP1}	Capacitor	1 nF
C_{EMCP2}	Capacitor	1 nF
C_{EMCP3}	Capacitor	1 nF
C_{PFILT1}, C_{PFILT2}	Capacitor	
R_{MON}	Resistor at MON pin	3.9kΩ
R_{VSD}	Limitation of reverse current due to transient (-2V, 8ms)	2Ω
R_{VDH}	Resistor	1kΩ
R_{GATE}	Resistor	2Ω
$R_{OPAFILT}$	Resistor	12Ω
R_{SH1}	Resistor	optional
R_{SH2}	Resistor	optional
R_{SH3}	Resistor	optional
L_{PFILT}		–
D_{VS}	Reverse-polarity protection diode	–

1) The capacitor must be dimensioned so as to ensure that flash operations modifying the content of the flash are never interrupted (e.g. in case of power loss).

28.2 ESD Immunity According to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “Gun test” (150pF, 330Ω) has been performed. The results and test condition will be available in a test report.

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin PWM_IO, versus GND[1)]	> 6	kV	positive pulse
ESD at pin PWM_IO, versus GND[1)]	< -6	kV	negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100nF, R_{MON} = 1kΩ, C_{PWM_IO} = 220pF, C_{VS} = >20µF ELCO + 100nF ESR < 1Ω, C_{VSD} = 1µF, R_{VSD} = 2Ω.

29.1.4 Thermal Resistance

Table 20 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	1) measured to Exposed Pad	P_1.4.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_1.4.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

29.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding bits in register PMCON0 are set until the sequence is terminated.

Table 21 System Timing1)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Wake-up over battery	t_{start}	–	–	3	ms	Battery ramp-up time to code execution	P_1.5.6
Wake-up over battery	$t_{startSW}$	–	–	1.5	ms	Battery ramp-up time to till MCU reset is released; V_S > 3 V and RESET = 1	P_1.5.1
Sleep-Exit	$t_{sleep\ -\ exit}$	–	–	1.5	ms	Rising/falling edge of any wake-up signal (PWM interface, MON) till MCU reset is released;	P_1.5.2
Sleep-Entry	$t_{sleep\ -\ entry}$	–	–	330	µs	2)	P_1.5.3

1) Not subject to production test, specified by design.

2) Wake events during Sleep-Entry are stored and lead to wake-up after Sleep Mode is reached.

29.8 Measurement Unit

29.8.1 System Voltage Measurement Parameters

Table 34 Supply Voltage Signal Conditioning

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Measurement output voltage range @ VAREF5	V_{A5}	0	–	5	V	–	P_8.1.15
Measurement output voltage range @ VAREF1V2	V_{A1V2}	0	–	1.23	V	–	P_8.1.16
Battery / Supply Voltage Measurement							
Input to output voltage attenuation: V_S	ATT_{VS_1}	–	0.055	–		SFR setting 1	P_8.1.41
Nominal operating input voltage range V_S	$V_{S,range1}$	3	–	22	V	[1]SFR setting 1; Max. value corresponds to typ. ADC full scale input; 3V < V_S < 28V	P_8.1.1
Accuracy of V_S after calibration	$V_{S,range1}$	-312	–	312	mV	SFR setting 1, V_S = 5.5 V to 18V, T_j = -40..85°C	P_8.1.70
Input to output voltage attenuation: V_S	ATT_{VS_2}	–	0.039	–		SFR setting 2	P_8.1.42
Nominal operating input voltage range V_S	$V_{S,range2}$	3	–	31	V	[1]SFR setting 2; Max. value corresponds to typ. ADC full scale input 3V < V_S < 28V	P_8.1.40
Accuracy of V_S after calibration	$V_{S,range2}$	-440	–	440	mV	SFR setting 2, V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.44
Driver Supply Voltage Measurement V_{SD}							
Input to output voltage attenuation: V_{SD}	ATT_{VSD}	–	0.039	–		–	P_8.1.21
Nominal operating input voltage range V_{SD}	$V_{SD,range}$	2.5	–	31	V	[1]	P_8.1.2

29.9 ADC1 - VAREF

29.9.1 Electrical Characteristics VAREF

Table 37 Electrical Characteristics VAREF

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required buffer capacitance	C_{VAREF}	0.1	–	1	µF	ESR < 1Ω	P_9.1.1
Reference output voltage	V_{AREF}	4.95	5	5.05	V	V_S > 5.5V	P_9.1.2
DC supply voltage rejection	$DC_{PSRVAREF}$	30	–	–	dB	1) –	P_9.1.3
Supply voltage ripple rejection	$AC_{PSRVAREF}$	26	–	–	dB	1) V_S = 13.5V; f = 0 ... 1KHz; V_r = 2Vpp	P_9.1.4
Turn ON time	t_{so}	–	–	200	µs	1) C_{ext} = 100nF PD_N to 99.9% of final value	P_9.1.5
Input resistance at VAREF Pin	$R_{IN,VAREF}$	–	100	–	kΩ	1)input impedance in case of VAREF is applied from external	P_9.1.20

1) Not subject to production test, specified by design.