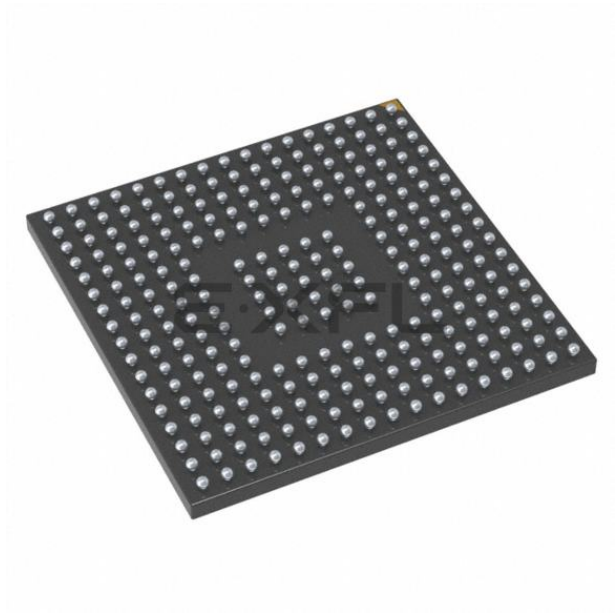

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 140 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 201-UFBGA |
| Supplier Device Package | 176+25UFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f437iih6 |

# 3 Functional overview

## 3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F43x family is compatible with all ARM tools and software.

*Figure 4* shows the general block diagram of the STM32F43x family.

*Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.*

## 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

## 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.22.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.22.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.22.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.23 Inter-integrated circuit interface ( $I^2C$)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 KHz), and fast (up to 400 KHz) modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 7*).

**Table 7. Comparison of I2C analog and digital filters**

| | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |

## 3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

## 3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 3.34 Universal serial bus on-the-go high-speed (OTG_HS)

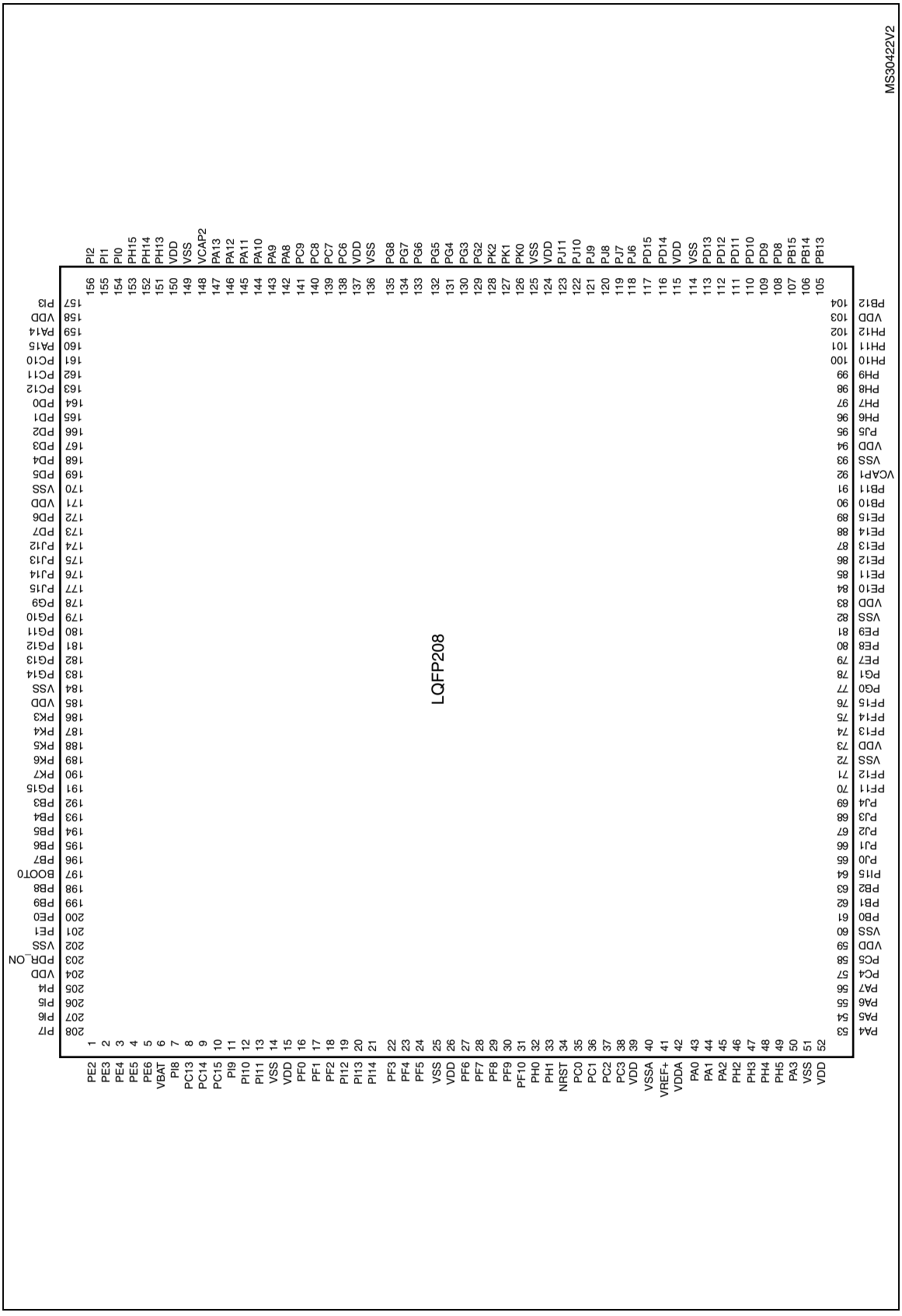
The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

**Figure 15. STM32F43x LQFP208 pinout**




1. The above figure shows the package top view.

**Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)**

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin type | I / O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | UFBGA176 | LQFP176 | WLCSP143 | LQFP208 | TFBGA216 | | | | | | |
| - | 10 | F2 | E2 | 16 | F11 | 16 | D2 | PF0 | I/O | FT | - | I2C2_SDA, FMC_A0, EVENTOUT | - |
| - | 11 | F3 | H3 | 17 | E9 | 17 | E2 | PF1 | I/O | FT | - | I2C2_SCL, FMC_A1, EVENTOUT | - |
| - | 12 | G5 | H2 | 18 | F10 | 18 | G2 | PF2 | I/O | FT | - | I2C2_SMBA, FMC_A2, EVENTOUT | - |
| - | - | - | - | - | - | 19 | E3 | PI12 | I/O | FT | - | LCD_HSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 20 | G3 | PI13 | I/O | FT | - | LCD_VSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 21 | H3 | PI14 | I/O | FT | | LCD_CLK, EVENTOUT | - |
| - | 13 | G4 | J2 | 19 | G11 | 22 | H2 | PF3 | I/O | FT | (5) | FMC_A3, EVENTOUT | ADC3_IN9 |
| - | 14 | G3 | J3 | 20 | F9 | 23 | J2 | PF4 | I/O | FT | (5) | FMC_A4, EVENTOUT | ADC3_ IN14 |
| - | 15 | H3 | K3 | 21 | F8 | 24 | K3 | PF5 | I/O | FT | (5) | FMC_A5, EVENTOUT | ADC3_ IN15 |
| 10 | 16 | G7 | G2 | 22 | H7 | 25 | H6 | $V_{SS}$ | S | - | - | - | - |
| 11 | 17 | G8 | G3 | 23 | - | 26 | H5 | $V_{DD}$ | S | - | - | - | - |
| - | 18 | NC (2) | K2 | 24 | G10 | 27 | K2 | PF6 | I/O | FT | (5) | TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, FMC_NIORD, EVENTOUT | ADC3_IN4 |
| - | 19 | NC (2) | K1 | 25 | F7 | 28 | K1 | PF7 | I/O | FT | (5) | TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, FMC_NREG, EVENTOUT | ADC3_IN5 |
| - | 20 | NC (2) | L3 | 26 | H11 | 29 | L3 | PF8 | I/O | FT | (5) | SPI5_MISO, SAI1_SCK_B, TIM13_CH1, FMC_NIOWR, EVENTOUT | ADC3_IN6 |

**Table 12. STM32F437xx and STM32F439xx alternate function mapping**

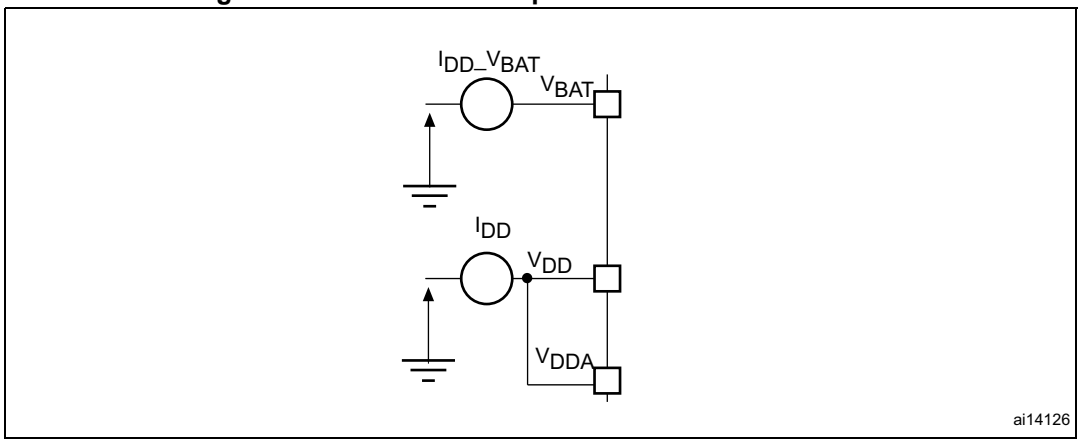
| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI3/USART1/2/3 | USART6/UART4/5/7/8 | CAN1/2/TIM12/13/14/LCD | OTG2_HS/OTG1_FS | ETH | FMC/SDIO/OTG2_FS | DCMI | LCD | SYS |
| Port A | PA0 | - | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS | UART4_TX | - | - | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | UART4_RX | - | - | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | - | EVENTOUT |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | - | - | - | ETH_MDIO | - | - | - | EVENTOUT |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | LCD_B5 | EVENTOUT |
| | PA4 | - | - | - | - | - | SPI1_NSS | SPI3_NSS/I2S3_WS | USART2_CK | - | - | - | - | OTG_HS_SOF | DCMI_HSYNC | LCD_VSYNC | EVENTOUT |
| | PA5 | - | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK | - | - | - | - | OTG_HS_ULPI_CK | - | - | - | - | EVENTOUT |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | - | SPI1_MISO | - | - | - | TIM13_CH1 | - | - | - | DCMI_PIXCLK | LCD_G2 | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI | - | - | - | TIM14_CH1 | - | ETH_MII_RX_DV/ETH_RMII_CRS_DV | - | - | - | EVENTOUT |
| | PA8 | MCO1 | TIM1_CH1 | - | - | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | - | - | - | LCD_R6 | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | - | - | USART1_TX | - | - | - | - | - | DCMI_D0 | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | - | DCMI_D1 | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | - | - | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | LCD_R4 | EVENTOUT |
| | PA12 | - | TIM1_ETR | - | - | - | - | - | USART1_RTS | - | CAN1_TX | OTG_FS_DP | - | - | - | LCD_R5 | EVENTOUT |

**Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI3/USART1/2/3 | USART6/UART4/5/7/8 | CAN1/2/TIM12/13/14/LCD | OTG2_HS/OTG1_FS | ETH | FMC/SDIO/OTG2_FS | DCMI | LCD | SYS |
| Port E | PE7 | - | TIM1_ETR | - | - | - | - | - | - | UART7_Rx | - | - | - | FMC_D4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | - | - | - | - | - | UART7_Tx | - | - | - | FMC_D5 | - | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | - | - | - | - | - | - | FMC_D6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | - | - | - | - | - | - | - | - | - | FMC_D7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | - | - | - | - | - | - | FMC_D8 | - | LCD_G3 | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | - | - | - | - | - | - | FMC_D9 | - | LCD_B4 | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | - | - | - | - | - | - | FMC_D10 | - | LCD_DE | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | - | - | FMC_D11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | | - | - | - | - | - | - | FMC_D12 | - | LCD_R7 | EVENTOUT |
| Port F | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENTOUT |
| | PF1 | - | | | | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENTOUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENTOUT |
| | PF3 | - | - | - | - | | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENTOUT |
| | PF4 | - | - | - | - | | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENTOUT |
| | PF5 | - | - | - | - | | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENTOUT |
| | PF6 | - | - | - | TIM10_CH1 | - | SPI5_NSS | SAI1_SD_B | - | UART7_Rx | - | - | - | FMC_NIORD | - | - | EVENTOUT |
| | PF7 | - | - | - | TIM11_CH1 | - | SPI5_SCK | SAI1_MCLK_B | - | UART7_Tx | - | - | - | FMC_NREG | - | - | EVENTOUT |

### 6.1.7 Current consumption measurement

**Figure 23. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

**Table 14. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD}$ and VBAT)(1) | − 0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT pins(2) | $V_{SS}$ − 0.3 | $V_{DD}$+4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on BOOT0 pin | $V_{SS}$ | 9.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins including $V_{REF-}$ | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.15: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.

**Table 18. Limitations depending on the operating power supply range**

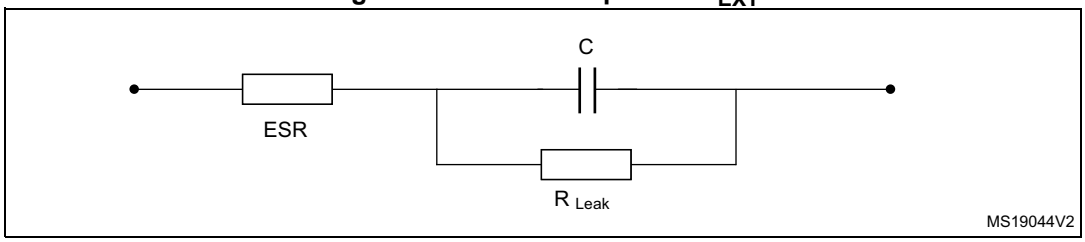
| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum HCLK frequency vs Flash memory wait states (1)(2) | I/O operation | Possible Flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz(4) | 168 MHz with 8 wait states and over-drive OFF | No I/O compensation | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1.2 Msps | 22 MHz | 180 MHz with 8 wait states and over-drive ON | No I/O compensation | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2.4 Msps | 24 MHz | 180 MHz with 7 wait states and over-drive ON | I/O compensation works | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(5) | Conversion time up to 2.4 Msps | 30 MHz | 180 MHz with 5 wait states and over-drive ON | I/O compensation works | 32-bit erase and program operations |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
4. Prefetch is not available.
5. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

## 6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor $C_{EXT}$ to the VCAP1/VCAP2 pins. $C_{EXT}$ is specified in *Table 19*.

**Figure 24. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

**Table 19. VCAP1/VCAP2 operating conditions(1)**

| Symbol | Parameter | Conditions |
|---|---|---|
| CEXT | Capacitance of external capacitor | 2.2 µF |
| ESR | ESR of external capacitor | < 2 Ω |

1. When bypassing the voltage regulator, the two 2.2 µF $V_{CAP}$ capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

**Table 24. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM(1)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All Peripherals enabled(3)(4) | 180 | 98 | 104(5) | 123 | 141(5) | mA |
| | | | 168 | 89 | 98(5) | 116 | 133(5) | |
| | | | 150 | 75 | 84 | 100 | 115 | |
| | | | 144 | 72 | 81 | 96 | 112 | |
| | | | 120 | 54 | 58 | 72 | 85 | |
| | | | 90 | 43 | 45 | 56 | 66 | |
| | | | 60 | 29 | 30 | 38 | 45 | |
| | | | 30 | 16 | 20 | 34 | 46 | |
| | | | 25 | 13 | 16 | 30 | 43 | |
| | | | 16 | 11 | 13 | 27 | 39 | |
| | | | 8 | 5 | 9 | 23 | 36 | |
| | | | 4 | 4 | 8 | 21 | 34 | |
| | | | 2 | 2 | 7 | 20 | 33 | |
| | | All Peripherals disabled(3) | 180 | 44 | 47(5) | 69 | 87(5) | |
| | | | 168 | 41 | 45(5) | 66 | 83(5) | |
| | | | 150 | 36 | 39 | 57 | 73 | |
| | | | 144 | 33 | 37 | 56 | 72 | |
| | | | 120 | 25 | 29 | 43 | 56 | |
| | | | 90 | 20 | 21 | 32 | 41 | |
| | | | 60 | 14 | 15 | 22 | 28 | |
| | | | 30 | 8 | 8 | 12 | 26 | |
| | | | 25 | 7 | 7 | 10 | 24 | |
| | | | 16 | 7 | 9 | 22 | 35 | |
| | | | 8 | 3 | 7 | 21 | 34 | |
| | | | 4 | 3 | 6 | 20 | 33 | |
| | | | 2 | 2 | 6 | 20 | 33 | |

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed by characterization.
3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. Guaranteed by test in production.

**Figure 25. Typical $V_{BAT}$ current consumption (LSE and RTC ON/backup RAM OFF)**

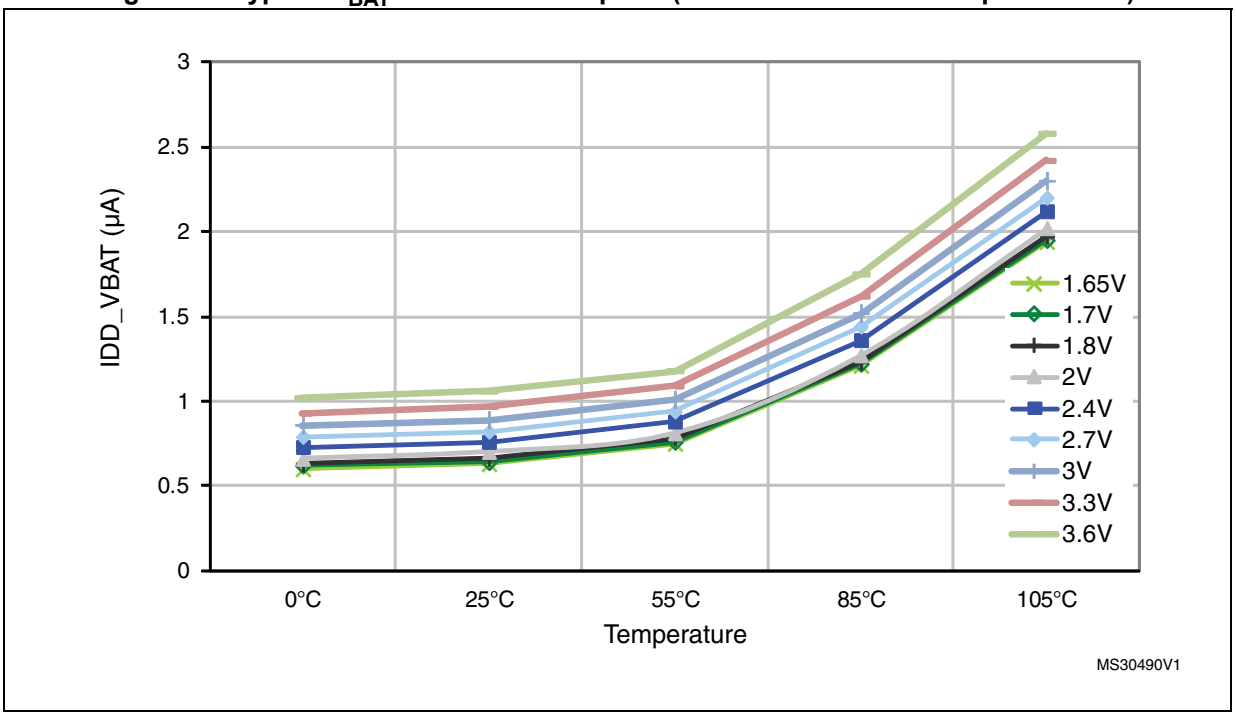



**Figure 26. Typical $V_{BAT}$ current consumption (LSE and RTC ON/backup RAM ON)**

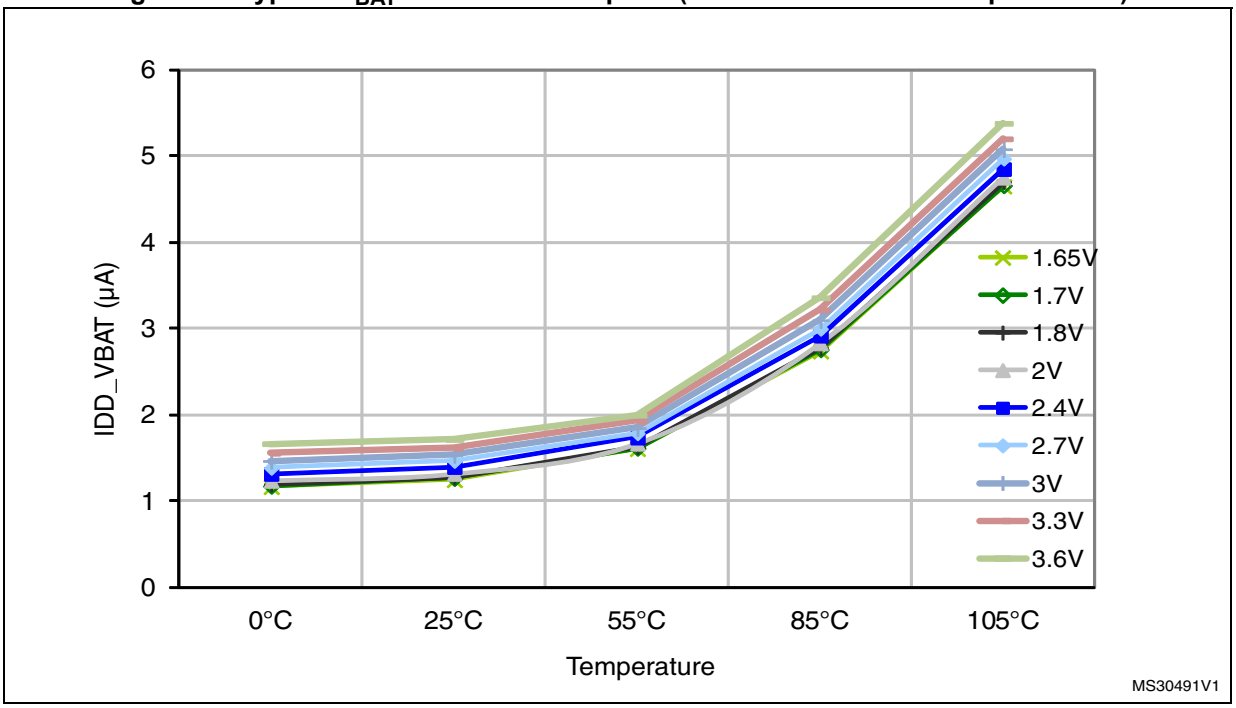


**Table 32. Typical current consumption in Sleep mode, regulator ON, $V_{DD}$=1.7 V(1)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | All Peripherals enabled | 168 | 65.5 | mA |
| | | | 150 | 55.5 | |
| | | | 144 | 53.5 | |
| | | | 120 | 39.0 | |
| | | | 90 | 31.6 | |
| | | | 60 | 21.7 | |
| | | | 30 | 9.8 | |
| | | | 25 | 8.8 | |
| | | All Peripherals disabled | 168 | 15.7 | |
| | | | 150 | 13.7 | |
| | | | 144 | 12.7 | |
| | | | 120 | 9.7 | |
| | | | 90 | 7.7 | |
| | | | 60 | 5.7 | |
| | | | 30 | 4.7 | |
| | | | 25 | 2.8 | |

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 56: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 50. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (6 suffix versions)<br>$T_A$ = –40 to +105 °C (7 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 10 kcycles(2) at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

## 6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

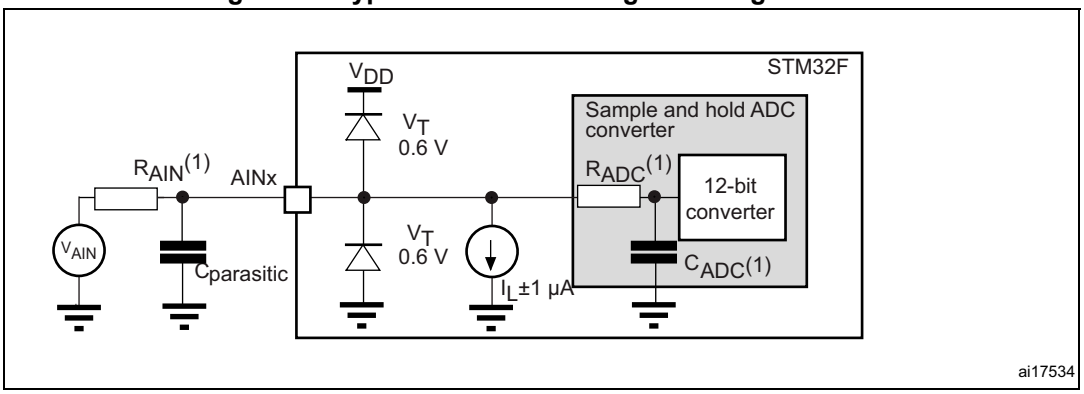
**Table 51. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ = +25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ =+25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 4A |

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

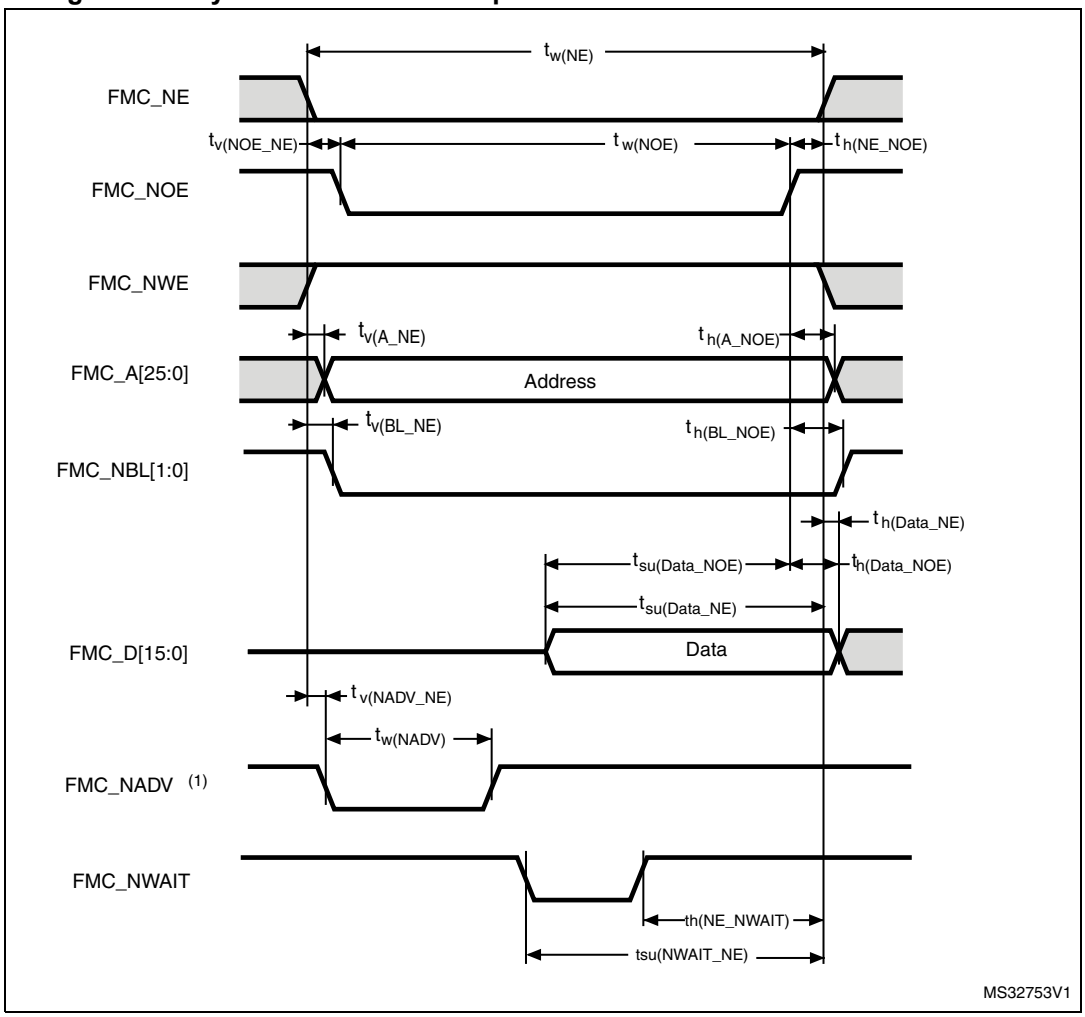
As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

**Figure 51. Typical connection diagram using the ADC**




1. Refer to *Table 74* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

**Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $2T_{HCLK} - 0.5$ | $2\ T_{HCLK}+0.5$ | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | 0 | 1 | ns |
| $t_{w(NOE)}$ | FMC_NOE low time | $2T_{HCLK}$ | $2T_{HCLK}+ 0.5$ | ns |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | ns |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 2 | ns |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | 0 | - | ns |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 2 | ns |
| $t_{h(BL\_NOE)}$ | FMC_BL hold time after FMC_NOE high | 0 | - | ns |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK} + 2.5$ | - | ns |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOEx high setup time | $T_{HCLK} +2$ | - | ns |

**Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $9T_{HCLK}$ | $9T_{HCLK}+0.5$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $7T_{HCLK}$ | $7T_{HCLK}+2$ | ns |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}+1.5$ | - | ns |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}-1$ | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

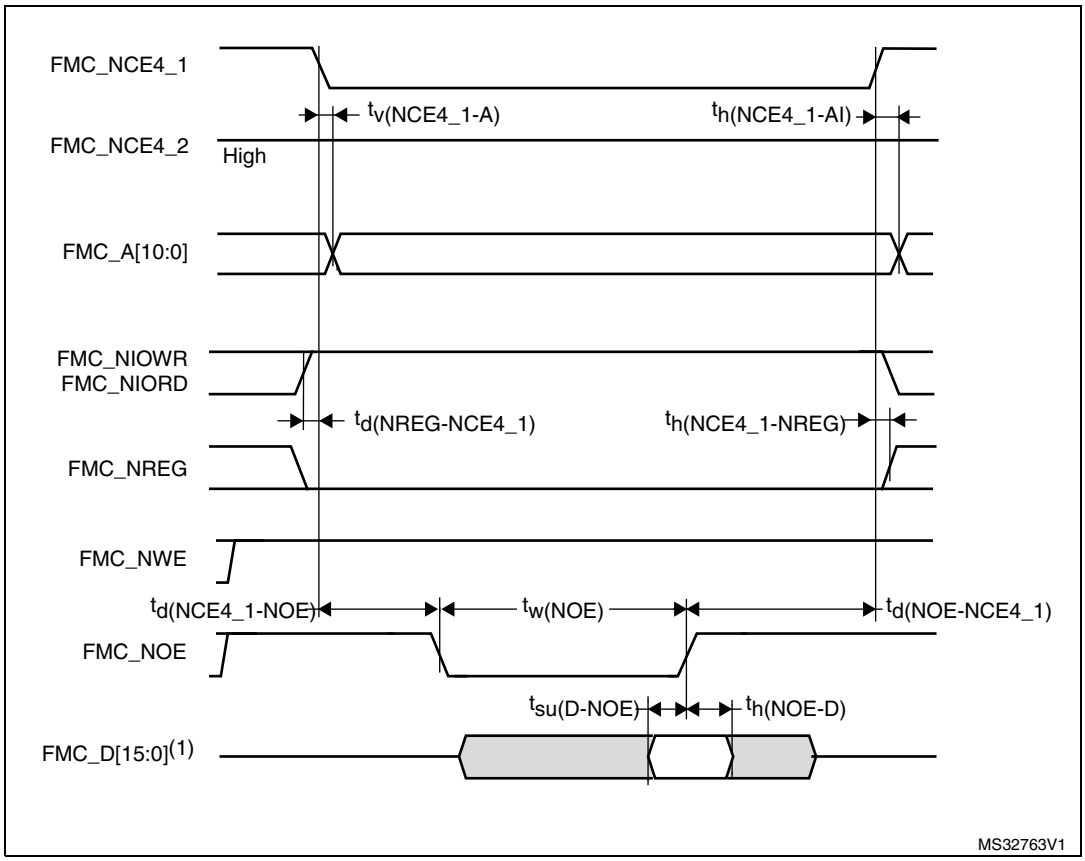
## Synchronous waveforms and timings

*Figure 59* through *Figure 62* represent synchronous waveforms and *Table 94* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the $T_{HCLK}$ is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

**Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access**




1. Only data bits 0...7 are read (bits 8...15 are disregarded).

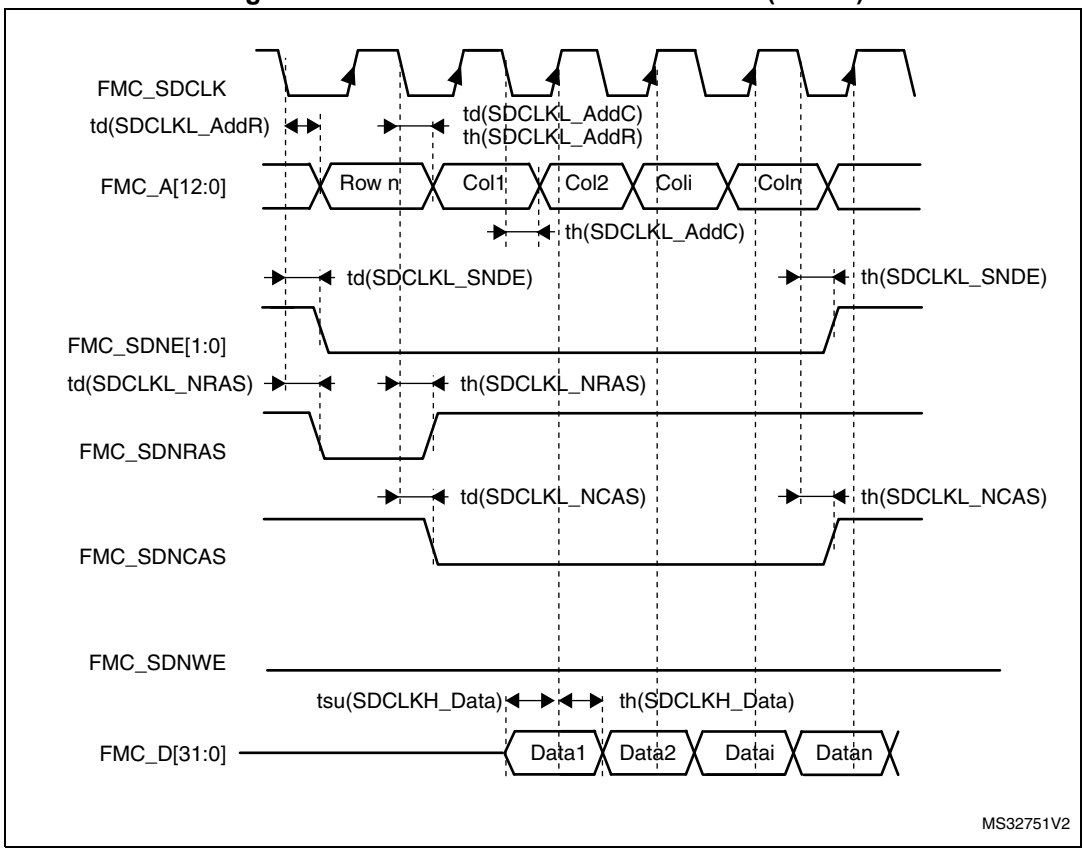
**Table 101. Switching characteristics for NAND Flash write cycles(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NWE)}$ | FMC_NWE low width | $4T_{HCLK}$ | $4T_{HCLK}+1$ | ns |
| $t_{v(NWE-D)}$ | FMC_NWE low to FMC_D[15-0] valid | 0 | - | ns |
| $t_{h(NWE-D)}$ | FMC_NWE high to FMC_D[15-0] invalid | $3T_{HCLK} - 1$ | - | ns |
| $t_{d(D-NWE)}$ | FMC_D[15-0] valid before FMC_NWE high | $5T_{HCLK} - 3$ | - | ns |
| $t_{d(ALE-NWE)}$ | FMC_ALE valid before FMC_NWE low | - | $3T_{HCLK}-0.5$ | ns |
| $t_{h(NWE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $3T_{HCLK} - 1$ | - | ns |

1. $C_L$ = 30 pF.

## SDRAM waveforms and timings

**Figure 73. SDRAM read access waveforms (CL = 1)**

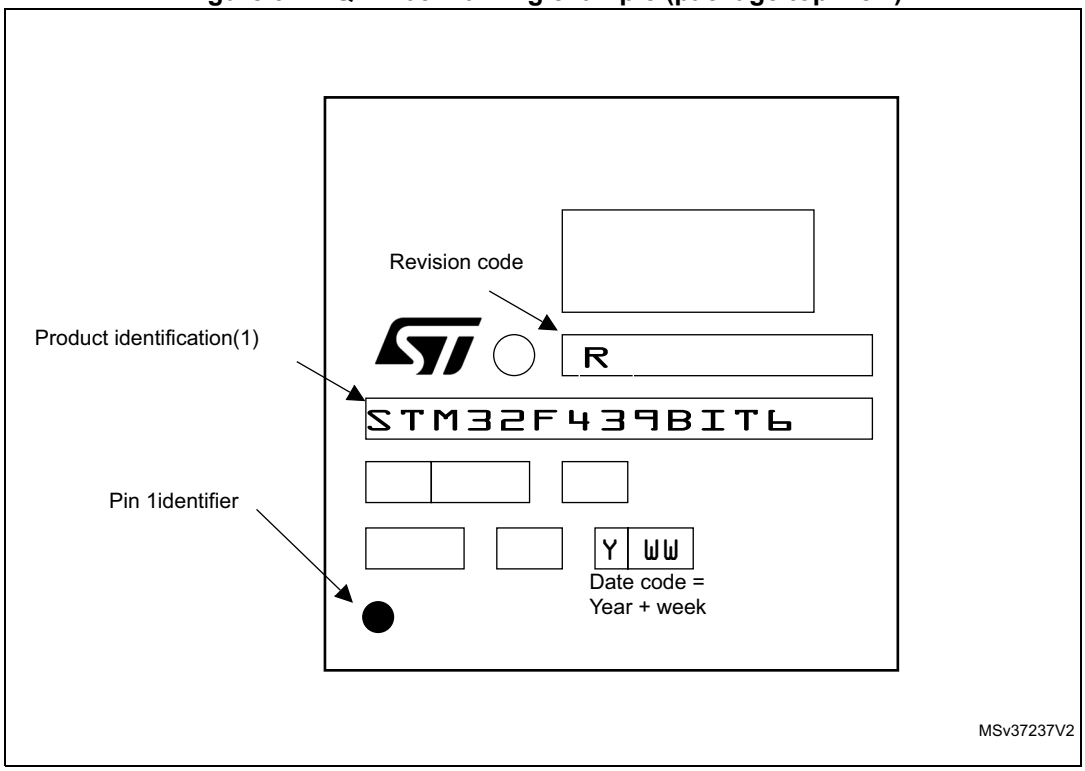


### Device marking for LQFP208

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

**Figure 94. LQFP208 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.