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STMicroelectronics - STM32F437VGT7TR Datasheet

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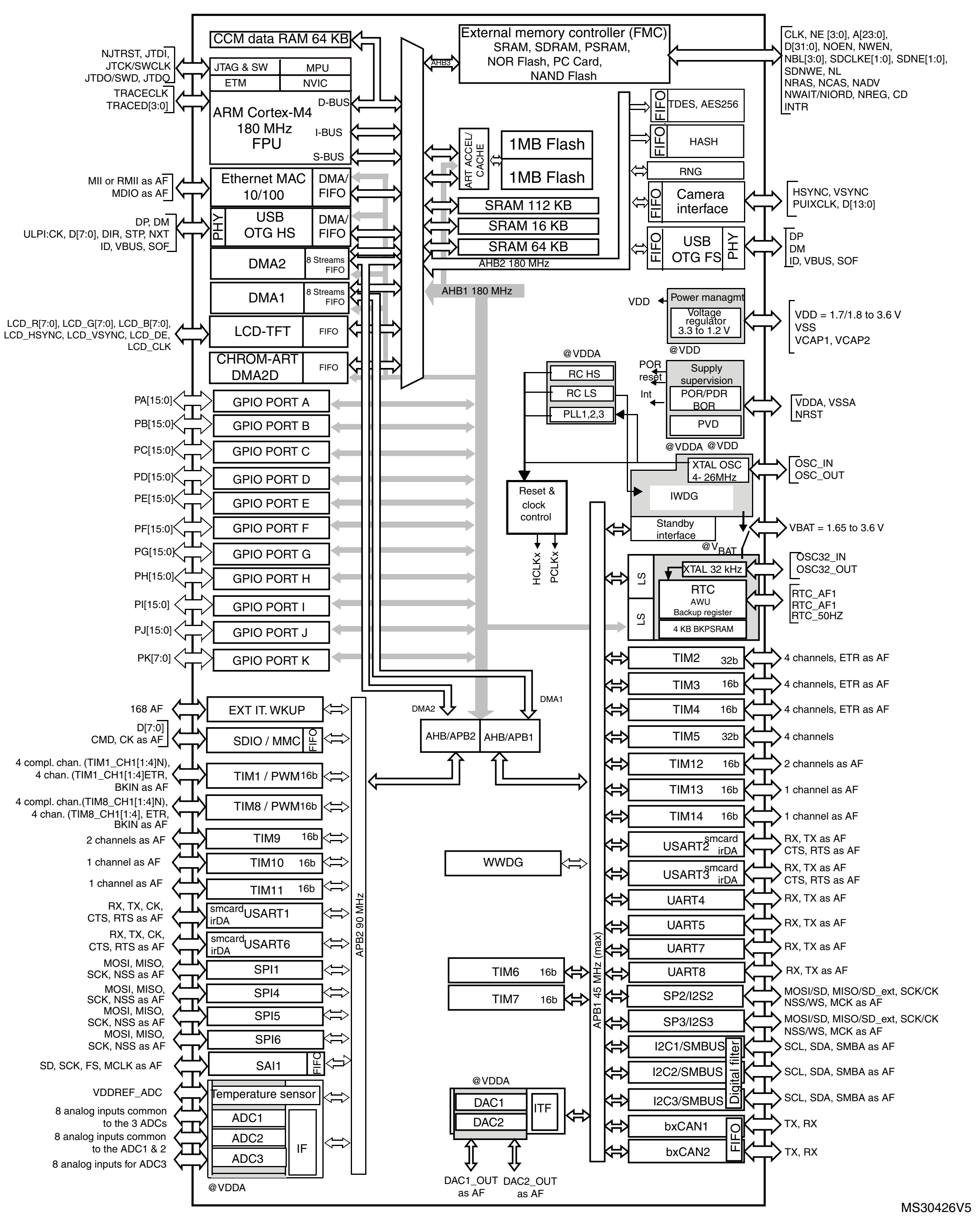
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

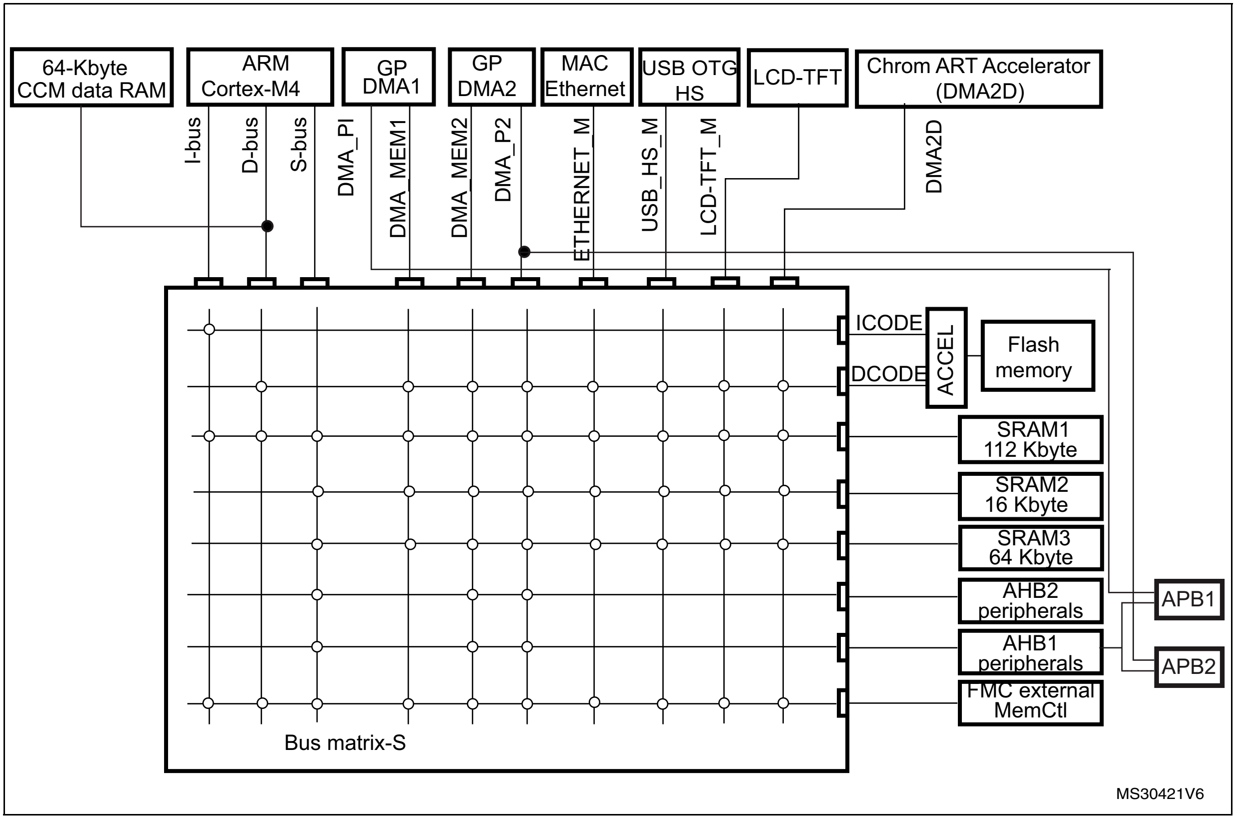
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f437vgt7tr

Figure 4. STM32F437xx and STM32F439xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.
2. The LCD-TFT is available only on STM32F439xx devices.

Figure 5. STM32F437xx and STM32F439xx Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

1. X = feature supported.

3.25 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.34 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.35 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.36 Cryptographic acceleration

The devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

- These algorithms consists of:

  Encryption/Decryption
  - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
  - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key

  Universal hash
  - SHA-1 and SHA-2 (secure hash algorithms)
  - MD5
  - HMAC

The cryptographic accelerator supports DMA request generation.

3.37 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.38 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

3.39 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

3.40 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.41 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
89	133	B6	A10	161	B7	192	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK/I2S3_CK, EVENTOUT	-
90	134	A6	A9	162	C7	193	A9	PB4 (NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, EVENTOUT	-
91	135	D5	A6	163	C8	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT	-
92	136	C5	B6	164	A8	195	B6	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	137	B5	B5	165	B8	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	138	A5	D6	166	C9	197	E6	BOOT0	I	B	-		V_{PP}
95	139	D4	A5	167	A9	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-

Table 13. STM32F437xx and STM32F439xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 22. reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis		-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis		-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	POR reset temporization		0.5	1.5	3.0	ms

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max[1]			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	All Peripherals enabled[2]	180	78	89[3]	110	130[3]	mA
			168	66	75[3]	93	110[3]	
			150	56	61	80	96	
			144	54	58	78	94	
			120	40	44	59	72	
			90	32	34	46	56	
			60	22	23	31	38	
			30	10	16	30	43	
			25	9	14	28	40	
			16	5	12	25	40	
			8	3	8	22	35	
			4	3	7	21	34	
			2	2	6.5	20	33	
		All Peripherals disabled	180	21	26[3]	54	76[3]	
			168	16	20[3]	41	58[3]	
			150	14	17	36	52	
			144	13	16.5	35	51	
			120	10	14	28	41	
			90	8	13	26	37	
			60	6	9	17	25	
			30	5	8	22	35	
			25	3	7	21	34	
			16	3	7	21	34	
			8	2	6	20	33	
			4	2	6	20	33	
			2	2	6	20	33	

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Based on characterization, tested in production.

Table 27. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max[1]			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.40	1.50	14.00	25.00	mA
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.35	1.50	14.00	25.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.29	1.10	10.00	18.00	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.23	1.10	10.00	18.00	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.19	0.50	6.00	9.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.10	0.40	4.00	7.00	

1. Data based on characterization, tested in production.

Additional current consumption

The MCU is placed under the following conditions:

- All I/O pins are configured in analog mode.
- The Flash memory access time is adjusted to fHCLK frequency.
- The voltage scaling is adjusted to fHCLK frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 120$ MHz,
  - Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- HSE crystal clock frequency is 25 MHz.
- When the regulator is OFF, V12 is provided externally as described in *Table 17: General operating conditions*
- T_A= 25 °C .

Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), V_{DD}=1.7 V[1]

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Unit
I_{DD}	Supply current in RUN mode from V_{DD} supply	All Peripheral enabled	168	88.2	mA
			150	74.3	
			144	71.3	
			120	52.9	
			90	42.6	
			60	28.6	
			30	15.7	
			25	12.3	
		All Peripheral disabled	168	40.6	
			150	30.6	
			144	32.6	
			120	24.7	
			90	19.7	
			60	13.6	
			30	7.7	
			25	6.7	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherls (such as ADC, or DAC) is not included.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART accelerator is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 180 MHz (Scale1 + over-drive ON), f_{HCLK} = 144 MHz (Scale 2), f_{HCLK} = 120 MHz (Scale 3)"
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 35. Peripheral current consumption

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 180 MHz)	GPIOA	2.50	2.36	2.08	µA/MHz
	GPIOB	2.56	2.36	2.08	
	GPIOC	2.44	2.29	2.00	
	GPIOD	2.50	2.36	2.08	
	GPIOE	2.44	2.29	2.00	
	GPIOF	2.44	2.29	2.00	
	GPIOG	2.39	2.22	2.00	
	GPIOH	2.33	2.15	1.92	
	GPIOI	2.39	2.22	2.00	
	GPIOJ	2.33	2.15	1.92	
	GPIOK	2.33	2.15	1.92	
	OTG_HS+ULPI	27.00	24.86	21.92	
	CRC	0.44	0.42	0.33	
	BKPSRAM	0.78	0.69	0.58	
	DMA1	25.33	23.26	20.50	
	DMA2	24.72	22.71	20.00	
	DMA2D	28.50	26.32	23.33	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	21.56	20.07	17.75	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 58. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	4	MHz
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	2	
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	8	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	4	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	25	MHz
			C_L = 50 pF, $V_{DD} \geq 1.8$ V	-	-	12.5	
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	10	ns
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	6	
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, $V_{DD} \geq 2.7$ V	-	-	50(4)	MHz
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	100(4)	
			C_L = 40 pF, $V_{DD} \geq 1.7$ V	-	-	25	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, $V_{DD} \geq 2.7$ V	-	-	6	ns
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	4	
			C_L = 40 pF, $V_{DD} \geq 1.7$ V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	6	

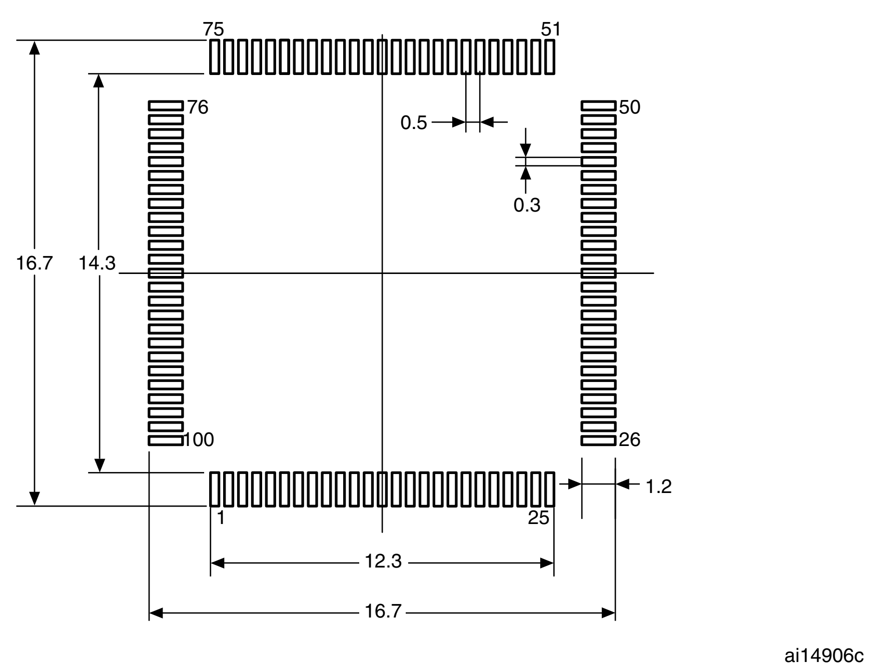
6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 74* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

Table 74. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA} - V_{REF+} < 1.2$ V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance		-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Figure 81. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

7.6 UFBGA169 package information

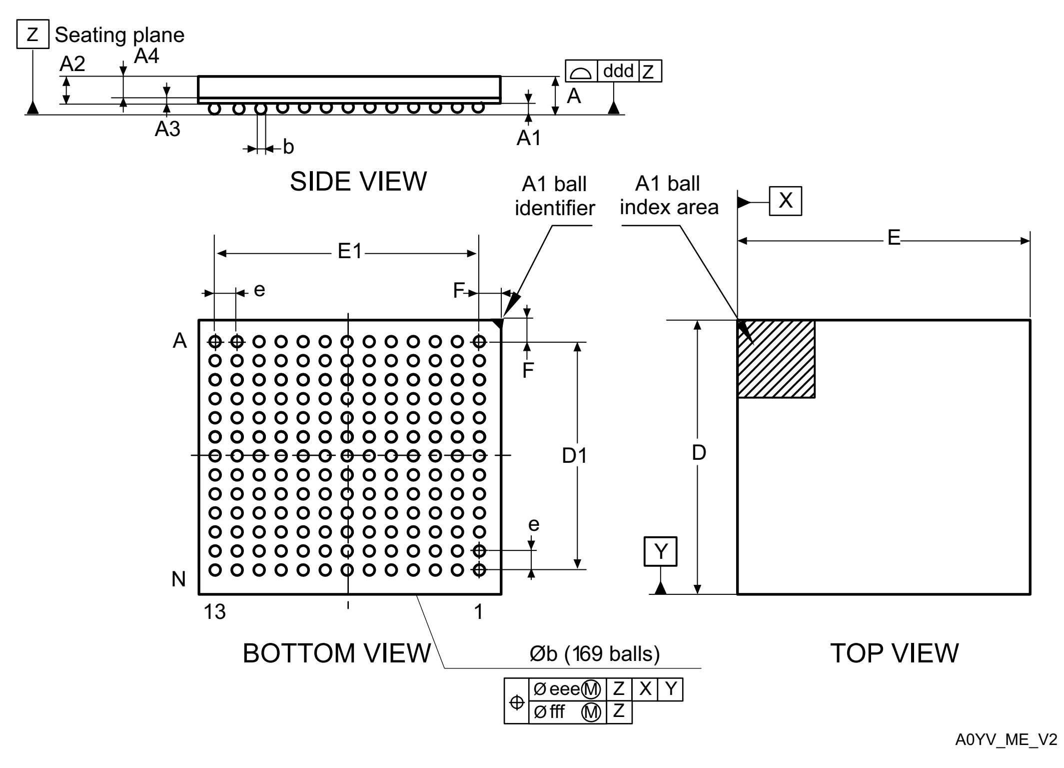


Figure 95. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline

1. Drawing is not to scale.

Table 116. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-

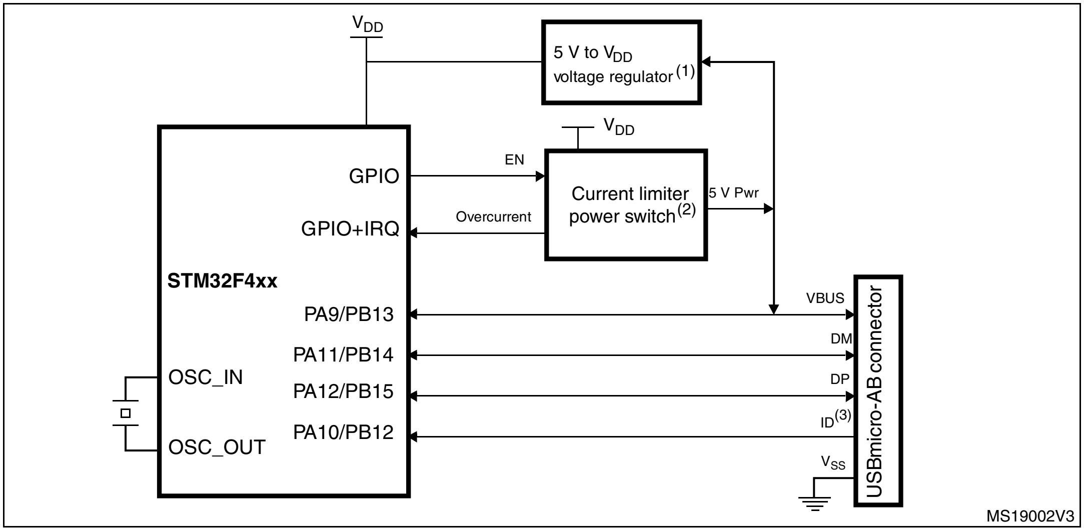


Figure 105. USB controller configured in dual mode and used in full speed mode

1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.