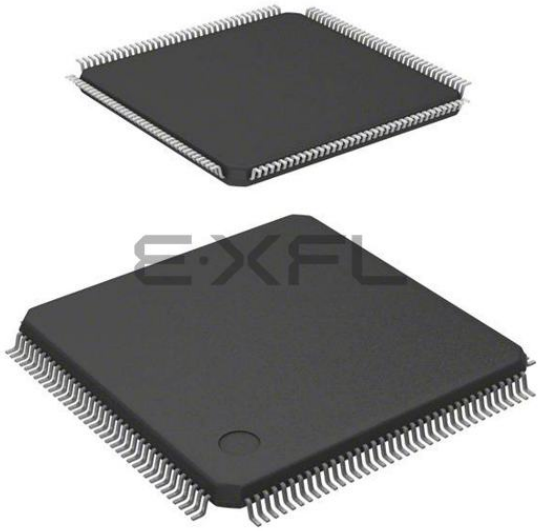

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f437zgt6

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F43x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F43x family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All devices embed:

- Up to 256Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC
- SAI1.

3.9 Flexible memory controller (FMC)

All devices embed an FMC. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- 8-,16-, 32-bit data bus width
- Read FIFO for SDRAM controller
- Write FIFO
- Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 LCD-TFT controller (available only on STM32F439xx)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
4	4	D1	B2	4	D9	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	D2	B3	5	E8	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	V_{SS}	S	-	-	-	-
-	-	-	-	-	-	-	F5	V_{DD}	S	-	-	-	-
6	6	E5	C1	6	C11	6	C1	V_{BAT}	S	-	-	-	-
-	-	NC (2)	D2	7	-	7	C2	PI8	I/O	FT	(3) (4)	EVENTOUT	TAMP_2
7	7	E4	D1	8	D10	8	D1	PC13	I/O	FT	(3) (4)	EVENTOUT	TAMP_1
8	8	E1	E1	9	D11	9	E1	PC14-OSC32_IN (PC14)	I/O	FT	(3) (4)	EVENTOUT	OSC32_IN (5)
9	9	F1	F1	10	E11	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(3) (4)	EVENTOUT	OSC32_OUT[5]
-	-	-	-	-	-	-	G5	V_{DD}	S	-	-	-	-
-	-	E2	D3	11	-	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	E3	12	-	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	NC (2)	E4	13	-	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F6	F2	14	E7	14	F2	V_{SS}	S	-	-	-	-
-	-	F4	F3	15	E10	15	F4	V_{DD}	S	-	-	-	-

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
96	140	C4	B4	168	B9	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	B4	A4	169	B10	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_RX, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A4	A3	170	A10	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	F5	D5	-	-	202	F6	V_{SS}	S		-		-
-	143	C3	C6	171	A11	203	E5	PDR_ON	S		-		-
100	144	K6	C5	172	D7	204	E7	V_{DD}	S		-		-
-	-	B3	D4	173	-	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A3	C4	174	-	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A2	C3	175	-	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	C2	176	-	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. Function availability depends on the chosen device.
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).

Table 11. FMC pin definition (continued)

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	D8	DA8	D8	D8
PE12	D9	D9	DA9	D9	D9
PE13	D10	D10	DA10	D10	D10
PE14	D11	D11	DA11	D11	D11
PE15	D12	D12	DA12	D12	D12
PD8	D13	D13	DA13	D13	D13
PD9	D14	D14	DA14	D14	D14
PD10	D15	D15	DA15	D15	D15
PH8		D16			D16
PH9		D17			D17
PH10		D18			D18
PH11		D19			D19
PH12		D20			D20
PH13		D21			D21
PH14		D22			D22
PH15		D23			D23
PI0		D24			D24
PI1		D25			D25
PI2		D26			D26
PI3		D27			D27
PI6		D28			D28
PI7		D29			D29
PI9		D30			D30
PI10		D31			D31
PD7		NE1	NE1	NCE2	
PG9		NE2	NE2	NCE3	
PG10	NCE4_1	NE3	NE3		
PG11	NCE4_2				
PG12		NE4	NE4		
PD3		CLK	CLK		
PD4	NOE	NOE	NOE	NOE	
PD5	NWE	NWE	NWE	NWE	
PD6	NWAIT	NWAIT	NWAIT	NWAIT	
PB7		NL(NADV)	NL(NADV)		

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port C	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	LCD_R2	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVENTOUT

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port G	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FMC_NE2/FMC_NCE3	DCMI_VSYNC (1)	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_NCE4_1/FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_NCE4_2	DCMI_D3	LCD_B3	EVENTOUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	-	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	-	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	FMC_SDNE1	DCMI_D8	-	-

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port J	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVEN TOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVEN TOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVEN TOUT
	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4	EVEN TOUT
	PJ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B0	EVEN TOUT
	PJ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B1	EVEN TOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVEN TOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVEN TOUT
Port K	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5	EVEN TOUT
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6	EVEN TOUT
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7	EVEN TOUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVEN TOUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVEN TOUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVEN TOUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVEN TOUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVEN TOUT

1. The DCMI_VSYNC alternate function on PG9 is only available on silicon revision 3.

Table 13. STM32F437xx and STM32F439xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 6C00- 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 5C00 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 23: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 120$ MHz
  - Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 4 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A =+25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Figure 49. Ethernet MII timing diagram

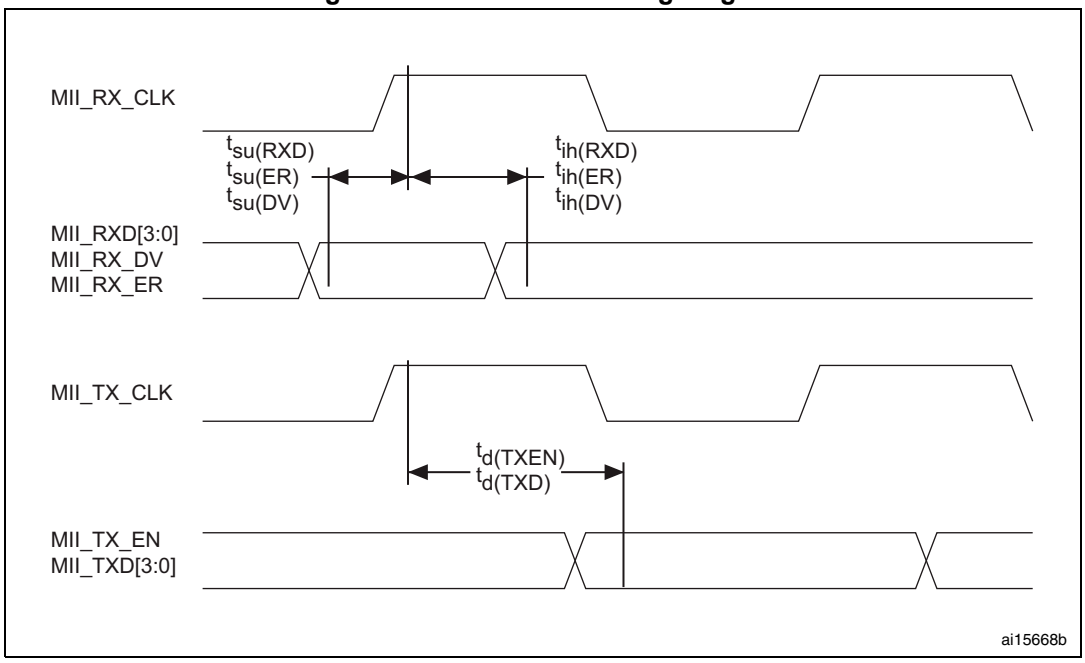


Table 73. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1.71 V < V_{DD} < 3.6 V	9	-	-	ns
$t_{ih(RXD)}$	Receive data hold time		10	-	-	
$t_{su(DV)}$	Data valid setup time		9	-	-	
$t_{ih(DV)}$	Data valid hold time		8	-	-	
$t_{su(ER)}$	Error setup time		6	-	-	
$t_{ih(ER)}$	Error hold time		8	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	2.7 V < V_{DD} < 3.6 V	8	10	14	
		1.71 V < V_{DD} < 3.6 V	8	10	16	
$t_{d(TXD)}$	Transmit data valid delay time	2.7 V < V_{DD} < 3.6 V	7.5	10	15	
		1.71 V < V_{DD} < 3.6 V	7.5	10	17	

1. Guaranteed by characterization results.

CAN (controller area network) interface

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 74* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

Table 74. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA}-V_{REF+} < 1.2$ V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance		-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode		-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 74*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 75. ADC static accuracy at f_{ADC} = 18 MHz

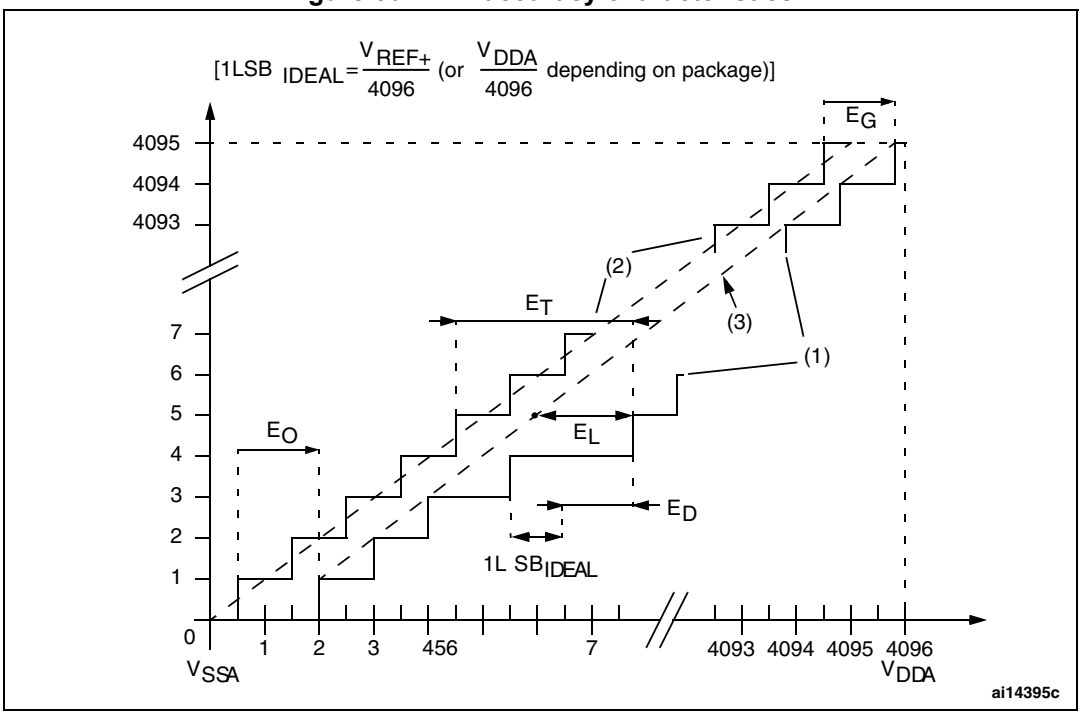
Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.17* does not affect the ADC accuracy.

Figure 50. ADC accuracy characteristics



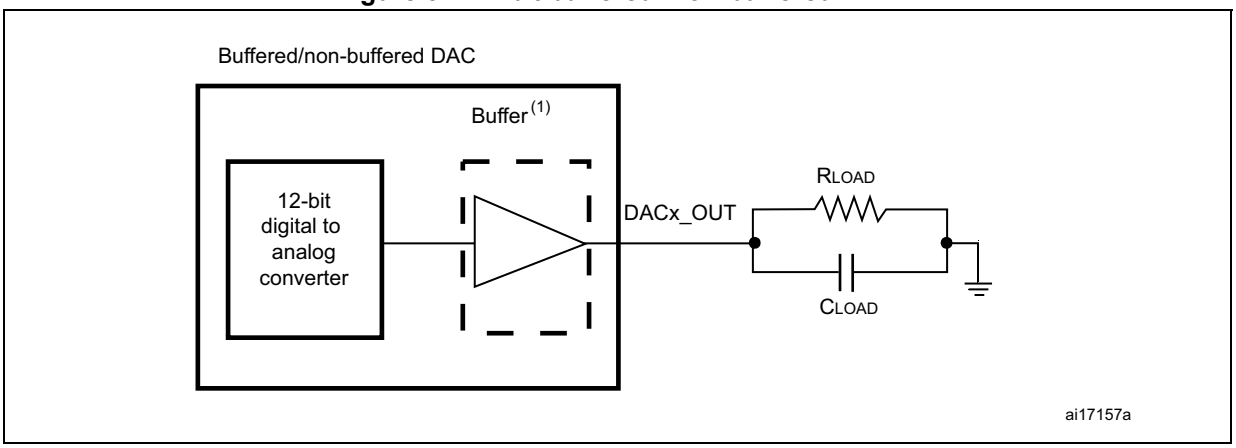
1. See also *Table 76*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

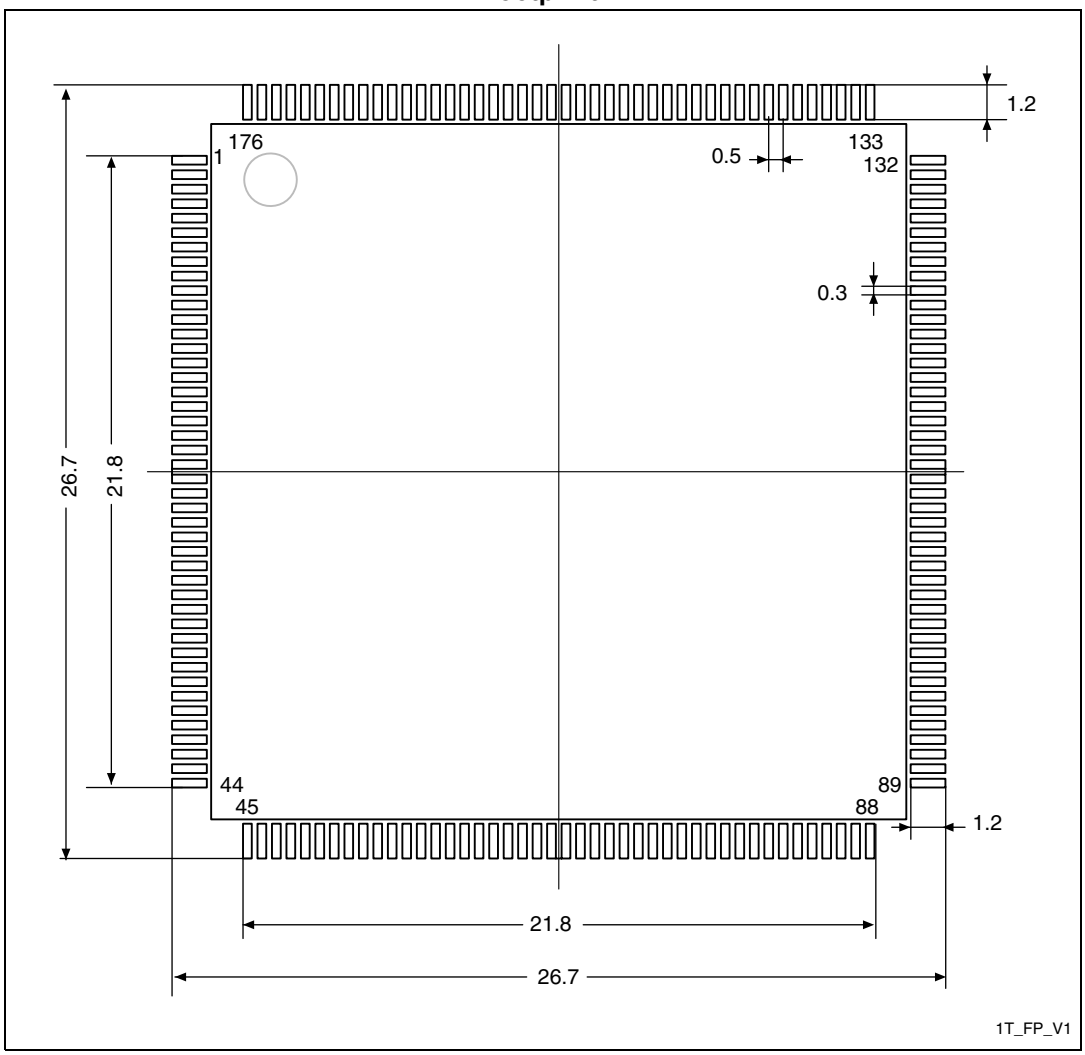
1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 54. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

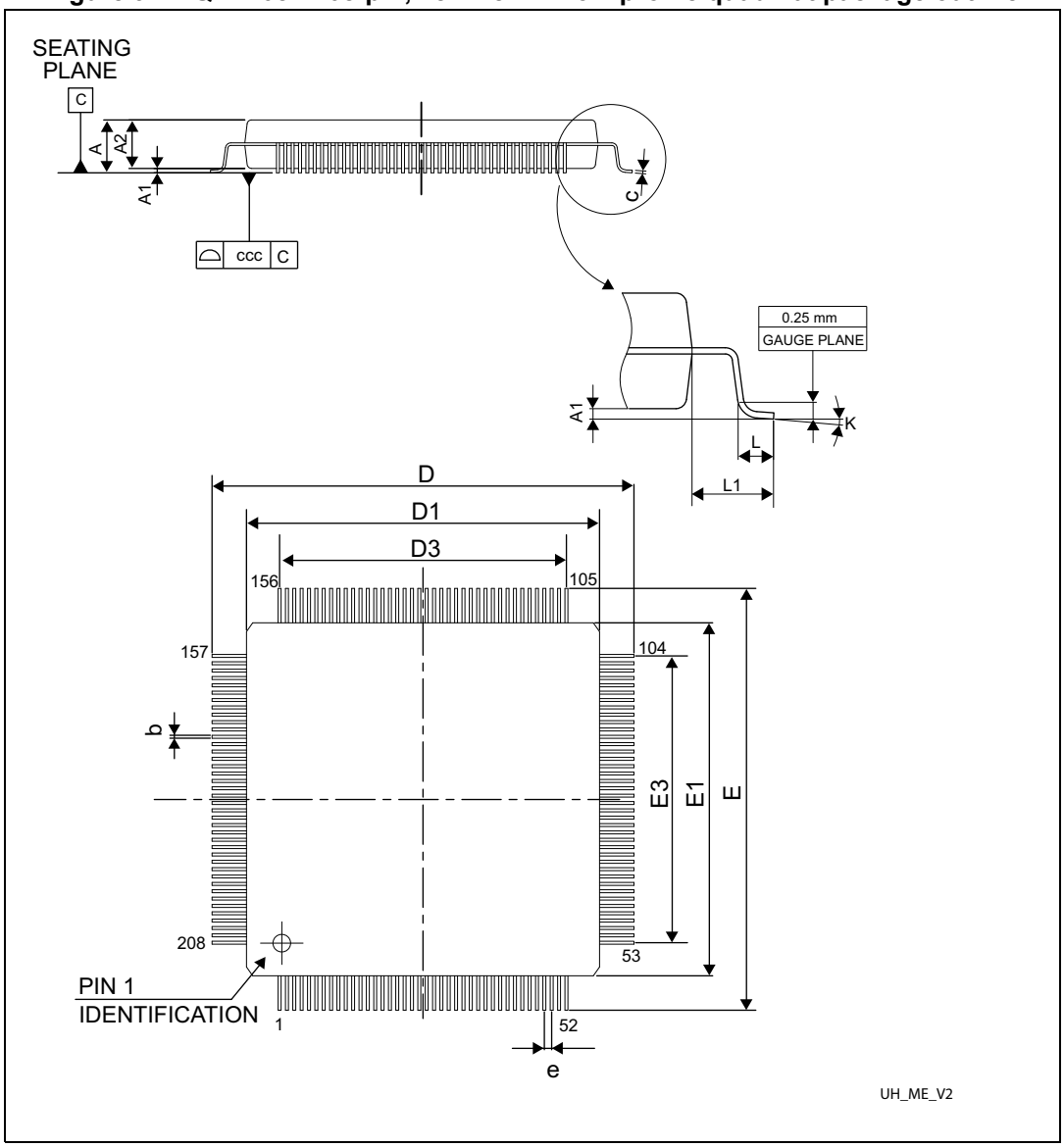
Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

7.5 LQFP208 package information

Figure 92. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline

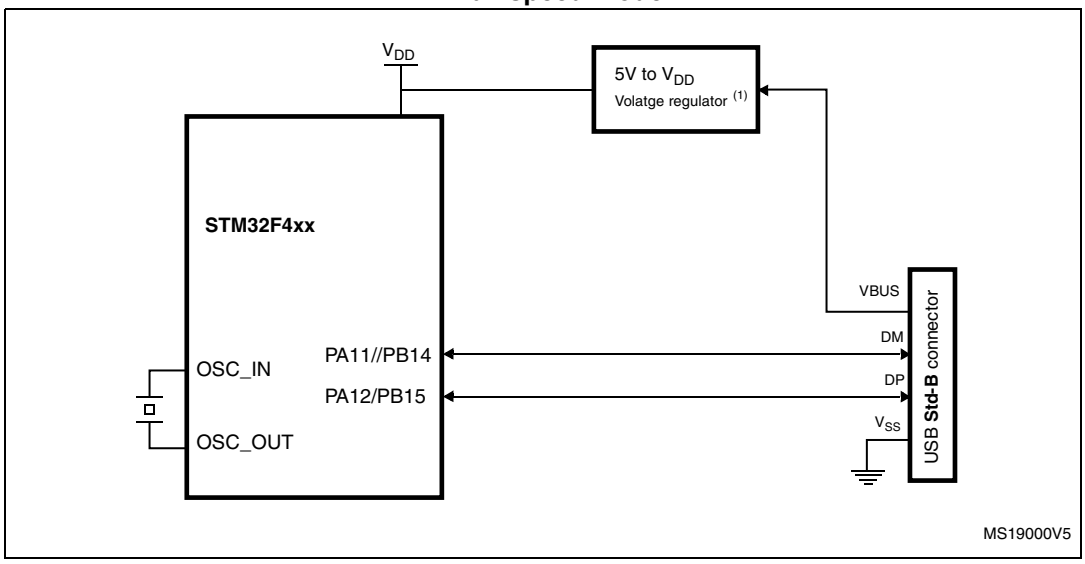


1. Drawing is not to scale.

Appendix B Application block diagrams

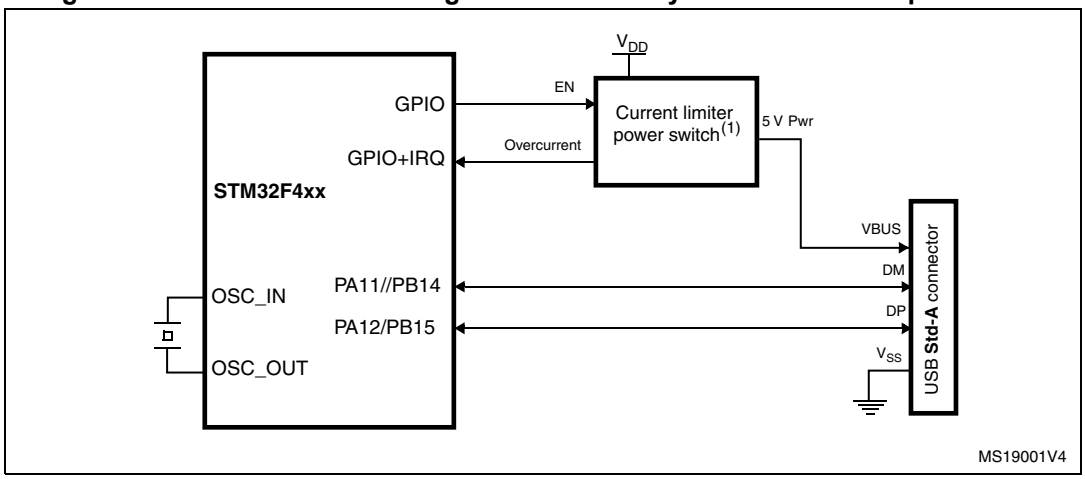
B.1 USB OTG full speed (FS) interface solutions

Figure 103. USB controller configured as peripheral-only and used in Full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 104. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.