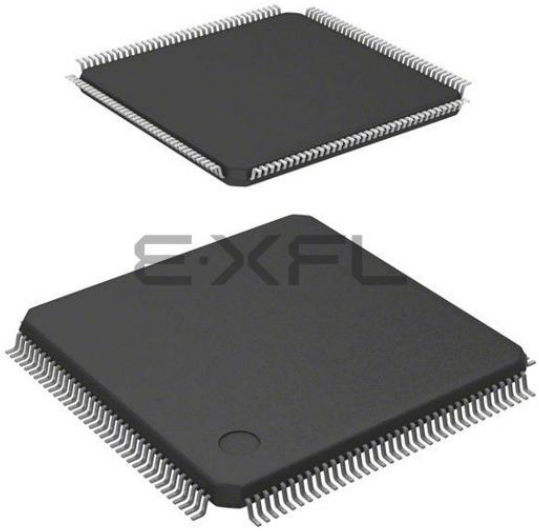

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f437zit7

Contents

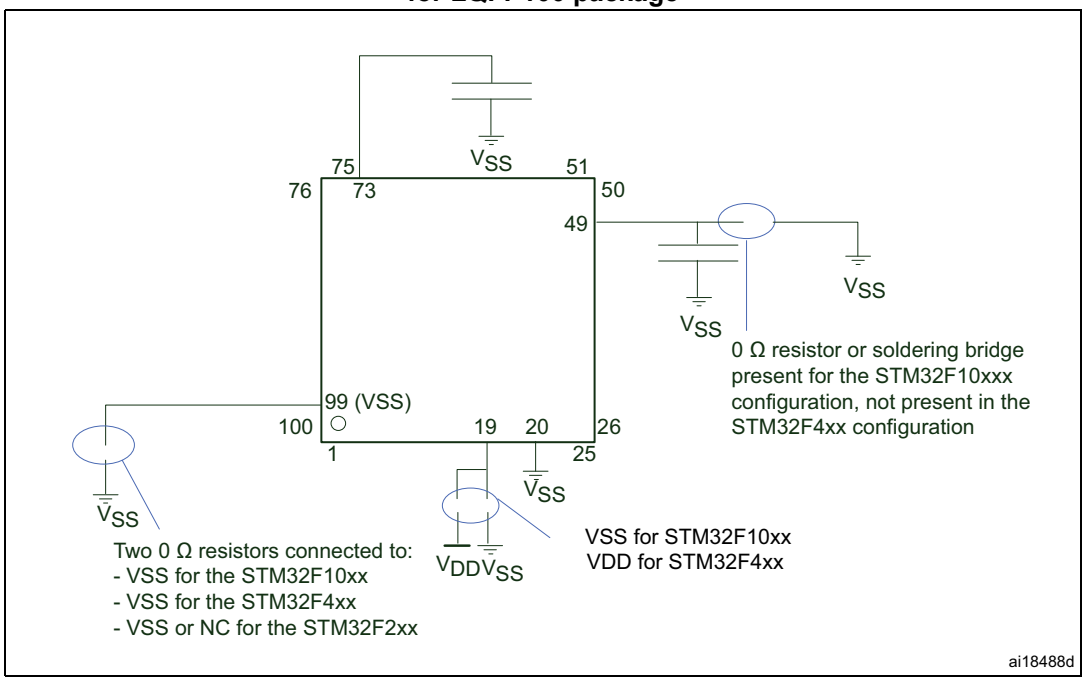
2.1 Full compatibility throughout the family

The STM32F437xx and STM32F439xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F437xx and STM32F439xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F437xx and STM32F439xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F43x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2*, and *Figure 3*, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package



3.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All devices embed:

- Up to 256Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

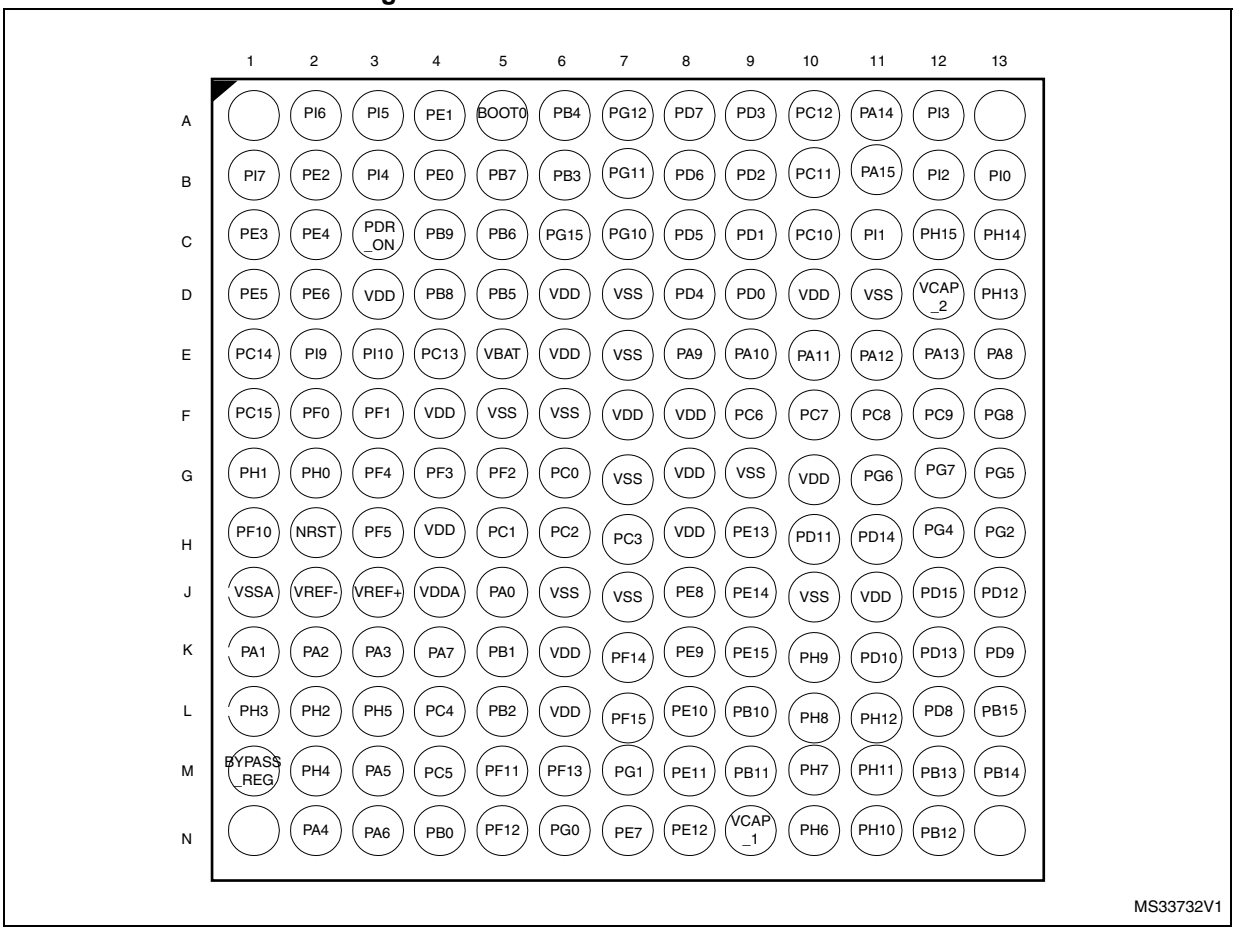
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 16. STM32F43x UFBGA169 ballout



1. The above figure shows the package top view.
2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	-	C11	D14	132	-	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK(7), FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	C14	133	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	A12	C13	134	-	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D11	D9	135	F5	-	F9	V_{SS}	S		-	-	-
-	-	D3	C9	136	A1	158	E10	V_{DD}	S		-	-	-
76	109	A11	A14	137	B1	159	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK/ EVENTOUT	-
77	110	B11	A13	138	C2	160	A13	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
78	111	C10	B14	139	A2	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B10	B13	140	B2	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, SDIO_D3, DCMI_D4, EVENTOUT	-
80	113	A10	A12	141	C3	163	A12	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT	-
81	114	D9	B12	142	B3	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port G	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FMC_NE2/FMC_NCE3	DCMI_VSYNC (1)	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_NCE4_1/FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_NCE4_2	DCMI_D3	LCD_B3	EVENTOUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	-	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	-	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	FMC_SDNE1	DCMI_D8	-	-

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	All Peripherals enabled(2)	180	78	89(3)	110	130(3)	mA
			168	66	75(3)	93	110(3)	
			150	56	61	80	96	
			144	54	58	78	94	
			120	40	44	59	72	
			90	32	34	46	56	
			60	22	23	31	38	
			30	10	16	30	43	
			25	9	14	28	40	
			16	5	12	25	40	
			8	3	8	22	35	
			4	3	7	21	34	
			2	2	6.5	20	33	
		All Peripherals disabled	180	21	26(3)	54	76(3)	
			168	16	20(3)	41	58(3)	
			150	14	17	36	52	
			144	13	16.5	35	51	
			120	10	14	28	41	
			90	8	13	26	37	
			60	6	9	17	25	
			30	5	8	22	35	
			25	3	7	21	34	
			16	3	7	21	34	
			8	2	6	20	33	
			4	2	6	20	33	
			2	2	6	20	33	

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Based on characterization, tested in production.

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 27*.

The characteristics given in *Table 37* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 37. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Output voltage levels

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 56: I/O static characteristics*).

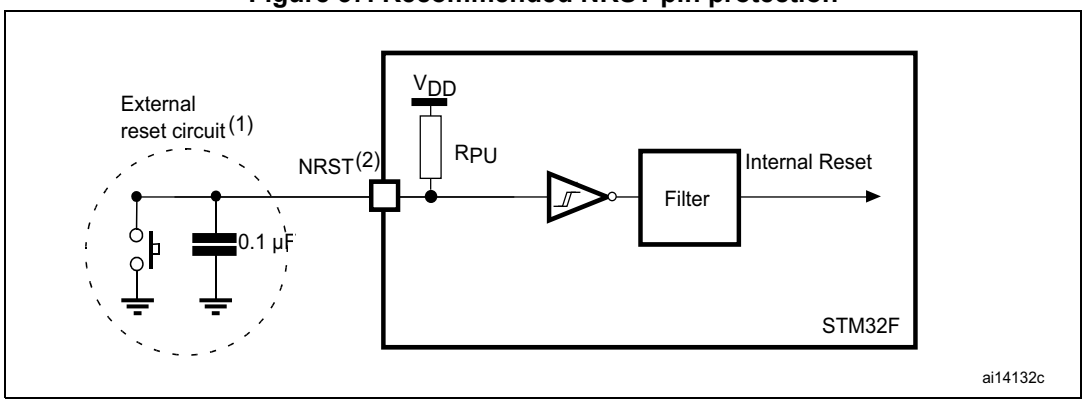
Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.

Figure 38. SPI timing diagram - slave mode and CPHA = 0

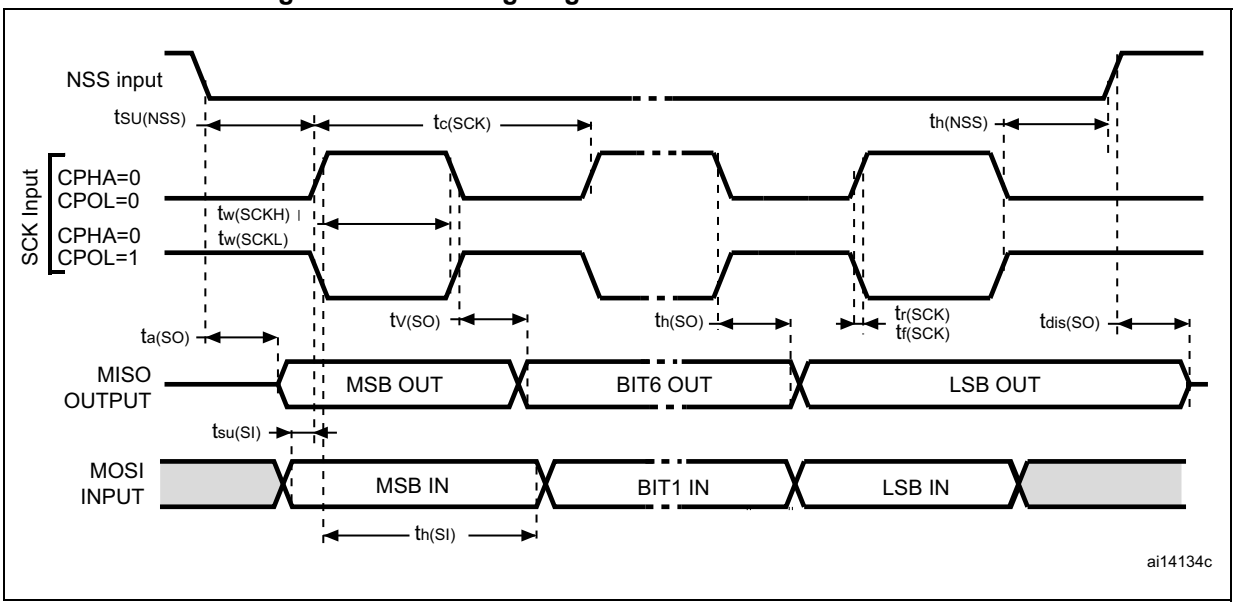
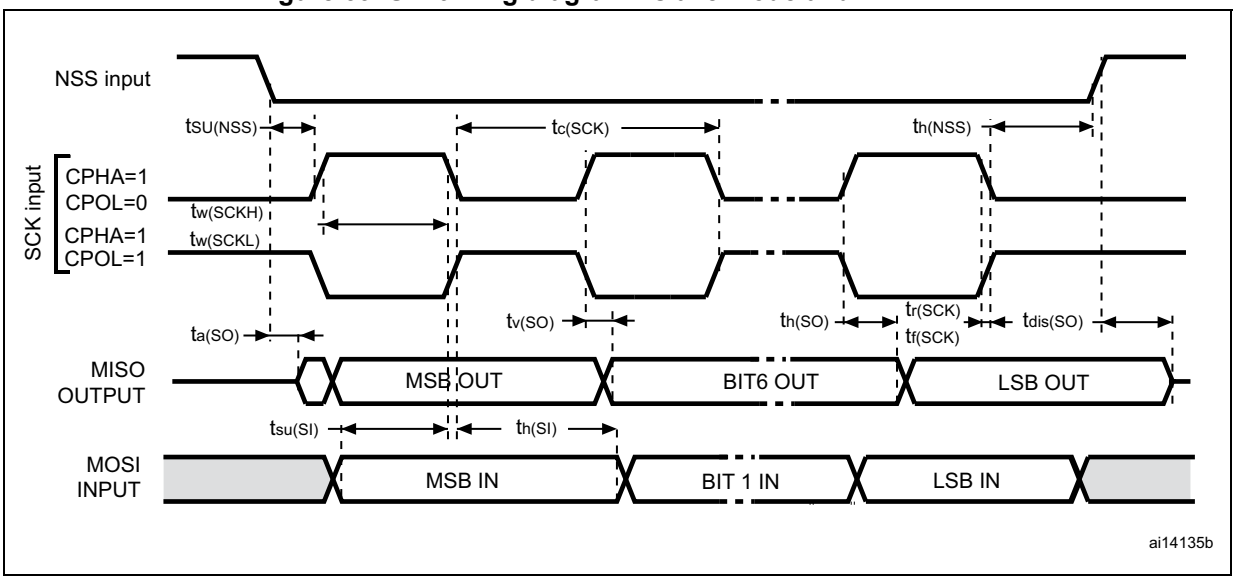


Figure 39. SPI timing diagram - slave mode and CPHA = 1



6.3.23 V_{BAT} monitoring characteristics

Table 82. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Reference voltage

The parameters given in *Table 83* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 83. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage		10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient		-	30	50	ppm/°C
t_{START}(2)	Startup time		-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

Table 84. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C $_{VDDA}$ = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+1$	$8T_{HCLK}+2$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK} - 1$	$6T_{HCLK}+2$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$		ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 57. Asynchronous multiplexed PSRAM/NOR read waveforms

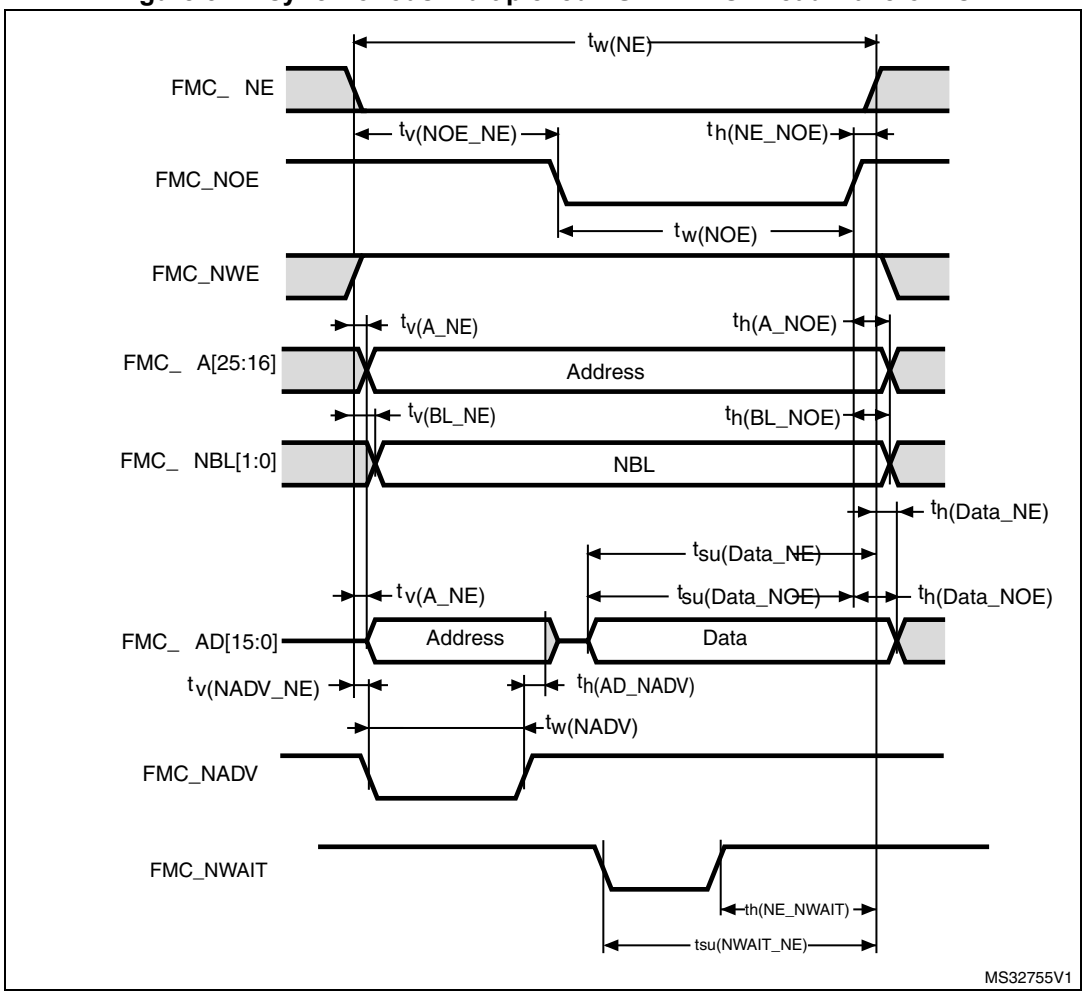


Table 90. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	ns
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK}+1$	ns
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	2	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	ns
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	0	-	ns
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	ns
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}+1.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK}+1$	-	ns
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 91. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK}+1.5$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}+1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$		ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 95. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	ns
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}	-	ns
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	ns
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	ns
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK}-0.5$	-	ns
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	ns
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	ns
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK}-0.5$	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 99. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(NIOWR)	FMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
tv(NIOWR-D)	FMC_NIOWR low to FMC_D[15:0] valid	-	0	ns
th(NIOWR-D)	FMC_NIOWR high to FMC_D[15:0] invalid	$9T_{HCLK} - 2$	-	ns
td(NCE4_1-NIOWR)	FMC_NCE4_1 low to FMC_NIOWR valid	-	$5T_{HCLK}$	ns
th(NCEx-NIOWR)	FMC_NCEx high to FMC_NIOWR invalid	$5T_{HCLK}$	-	ns
td(NIORD-NCEx)	FMC_NCEx low to FMC_NIORD valid	-	$5T_{HCLK}$	ns
th(NCEx-NIORD)	FMC_NCEx high to FMC_NIORD) valid	$6T_{HCLK}+2$	-	ns
tw(NIORD)	FMC_NIORD low width	$8T_{HCLK} - 0.5$	$8T_{HCLK}+0.5$	ns
tsu(D-NIORD)	FMC_D[15:0] valid before FMC_NIORD high	T_{HCLK}	-	ns
td(NIORD-D)	FMC_D[15:0] valid after FMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 69 through *Figure 72* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

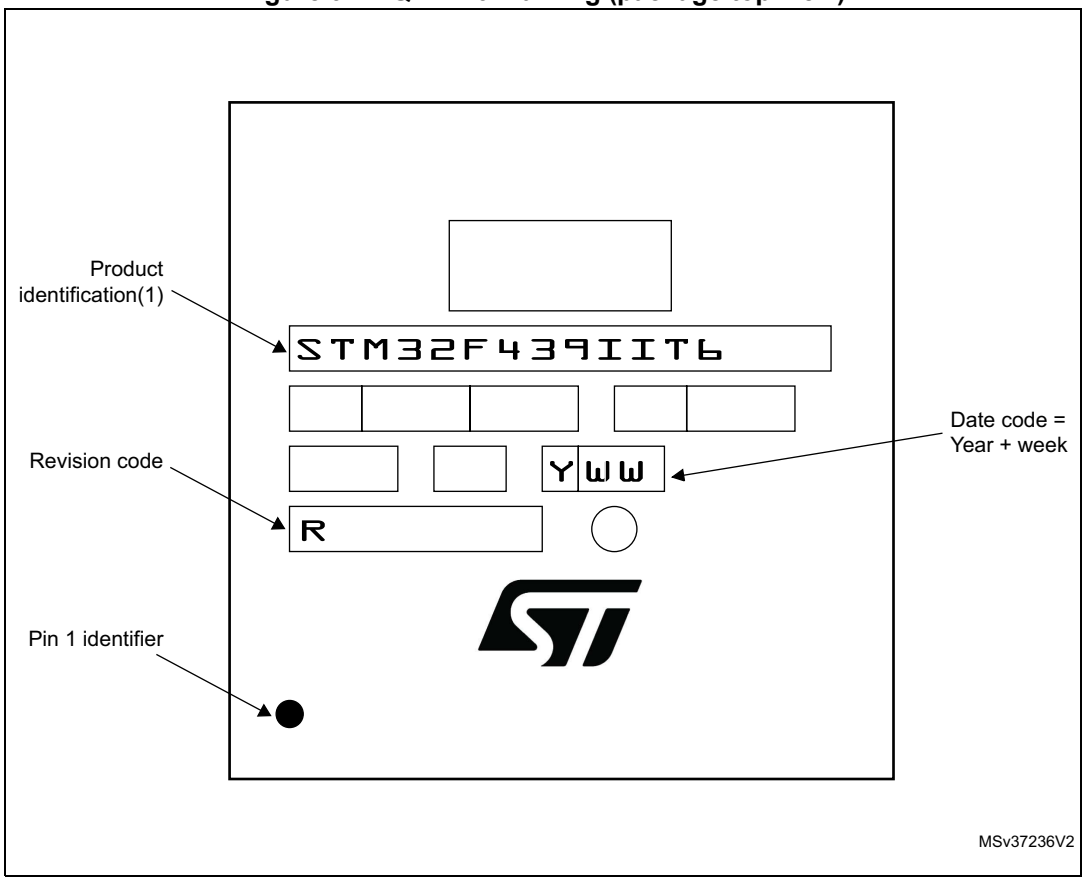
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Device marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

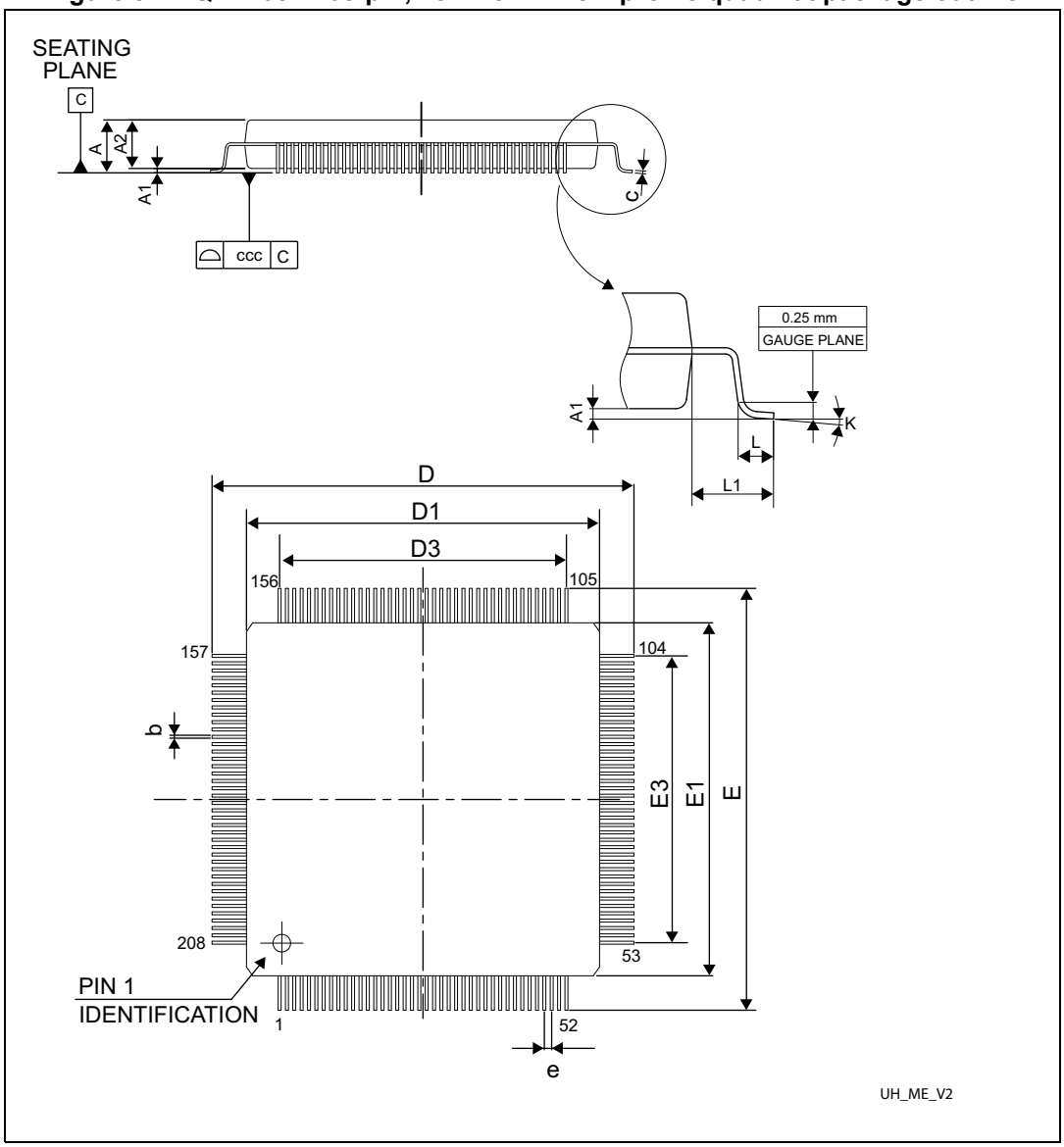
Figure 91. LQFP176 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 LQFP208 package information

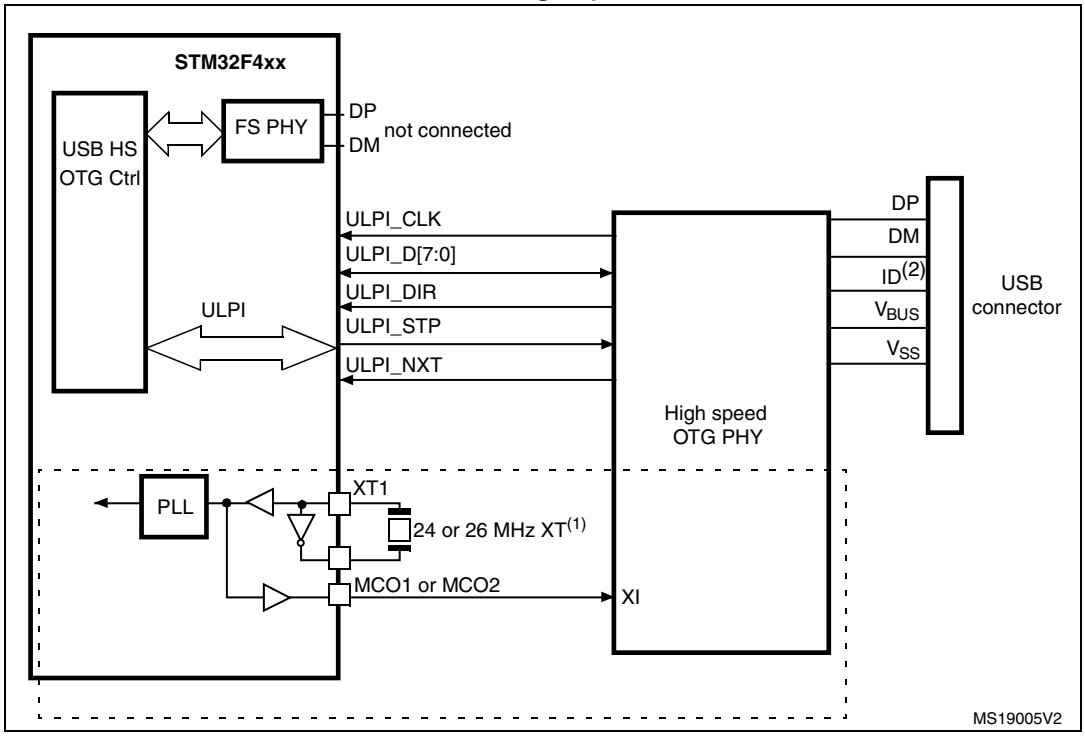
Figure 92. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline



1. Drawing is not to scale.

B.2 USB OTG high speed (HS) interface solutions

Figure 106. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F43x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.