STMicroelectronics - STM32F439AIH6 Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f439aih6

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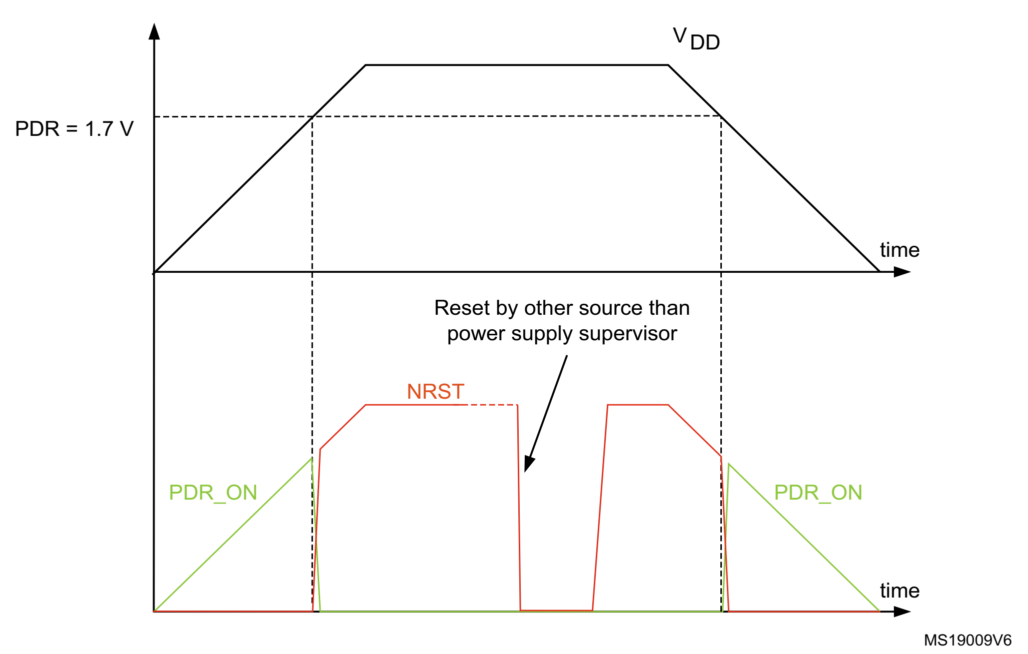


3.18 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

3.18.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode
    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.34 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

3.39 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

3.40 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.41 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.42 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.43 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F43x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

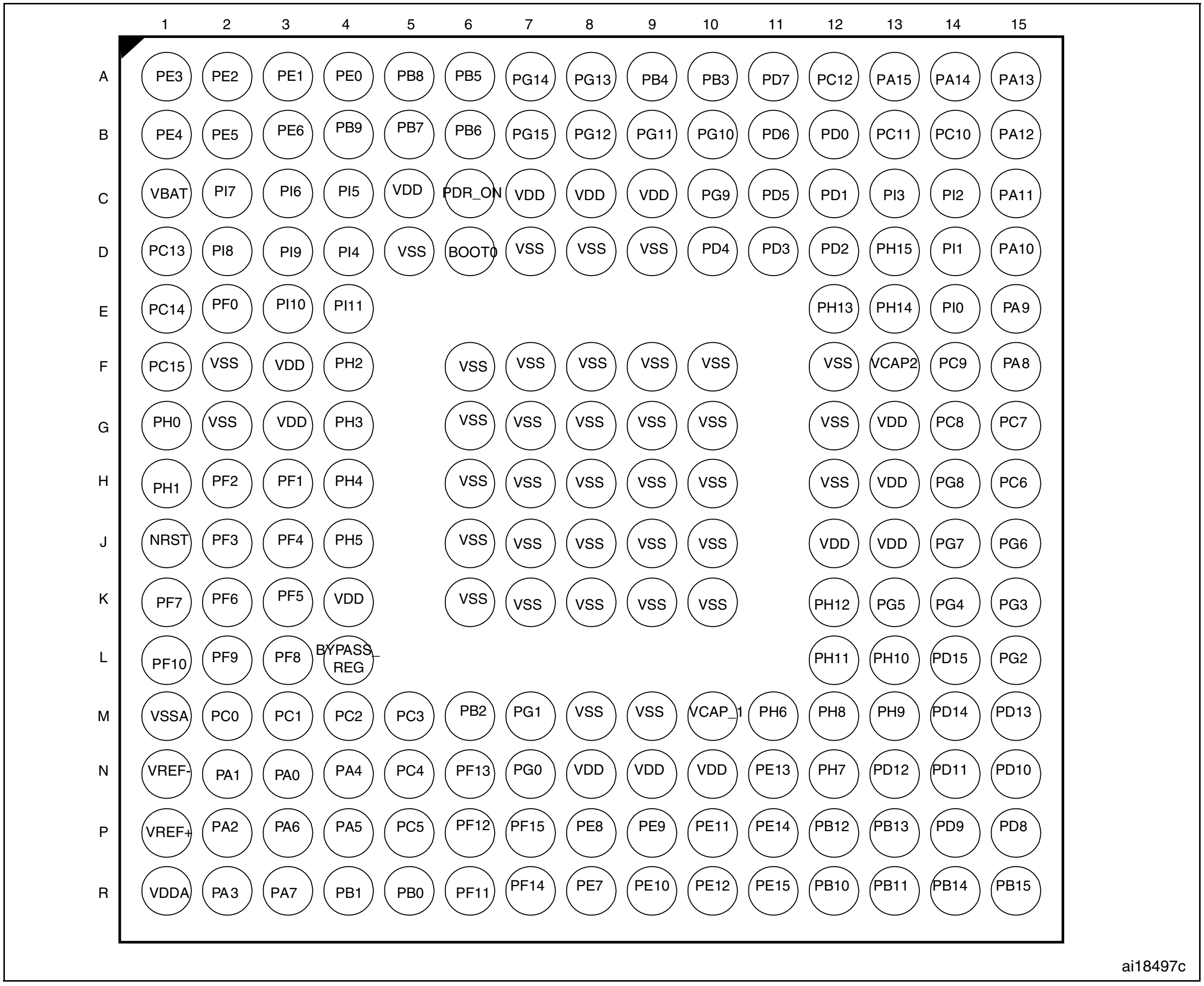
Figure 12. STM32F43x WLCSP143 ballout

	11	10	9	8	7	6	5	4	3	2	1
A	PDR_ON	PE1	PB8	PB6	PG15	PG12	PD7	PD5	PD2	PC10	VDD
B	PE4	PE0	PB9	PB7	PB3	PG11	PD4	PD3	PD0	PC11	PA14
C	VBAT	PE3	BOOT0	PB5	PB4	PG10	VDD	PD1	PC12	PA15	VDD
D	PC14	PC13	PE5	PE2	VDD	PG13	PA10	PA11	PA13	VSS	VCAP_2
E	PC15	VDD	PF1	PE6	VSS	VDD	PG9	PC8	PC9	PA9	PA12
F	PF0	PF2	PF4	PF5	PF7	PG14	VSS	PD6	PC7	PC6	PA8
G	PF3	PF6	PF10	PF9	VDD	PG5	PG4	PG6	PG3	PG8	VDD
H	PF8	PH1	NRST	PC0	VSS	PD12	PD13	PD10	VSS	VSS	PG7
J	PH0	PC2	PC3	VDD	VDD	VDD	VDD	PE10	PB15	PD14	PG2
K	PC1	VSSA	PA0	PA1	PB1	PF13	PG1	PE11	PB14	PD11	PD15
L	VREF+	VDDA	PA2	PA7	PB2	PF14	PE7	PE12	PE15	PD8	VDD
M	PA3	PA4	PA5	PC4	PF11	PF15	PE8	PE14	PB10	PB12	PD9
N	BYPASS_REG	PA6	PC5	PB0	PF12	PG0	PE9	PE13	PB11	VCAP_1	PB13

MS31855V2

1. The above figure shows the package bump view.

Figure 17. STM32F43x UFBGA176 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP2	PC9	PA8
G	PH0	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	BYPASS_REG								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

1. The above figure shows the package top view.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	-	M1	L4	48	N11	-	L5	BYPASS_REG	I	FT	-	-	-
28	39	J11	K4	49	J8	52	K5	V_{DD}	S	-	-	-	-
29	40	N2	N4	50	M10	53	N4	PA4	I/O	TTa	(5)	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4 /DAC_OUT1
30	41	M3	P4	51	M9	54	P4	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_IN5/DAC_OUT2
31	42	N3	P3	52	N10	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6
32	43	K4	R3	53	L8	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
33	44	L4	N5	54	M8	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_RMII_RXD0, EVENTOUT	ADC12_IN14
34	45	M4	P5	55	N9	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_RMII_RXD1, EVENTOUT	ADC12_IN15
-	-	-	-	-	J7	59	L7	V_{DD}	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{IN}	Input voltage on RST and FT pins(7)	$2\ V \leq V_{DD} \leq 3.6\ V$	− 0.3	-	5.5	V
		$V_{DD} \leq 2\ V$	− 0.3	-	5.2	
	Input voltage on TTa pins		− 0.3	-	V_{DDA}+ 0.3	
	Input voltage on BOOT0 pin		0	-	9	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(8)	LQFP100	-	-	465	mW
		WLCSP143	-	-	641	
		LQFP144	-	-	500	
		UFBGA169	-	-	385	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40		85	°C
		Low power dissipation(9)	− 40		105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40		105	°C
		Low power dissipation(9)	− 40		125	
TJ	Junction temperature range	6 suffix version	− 40		105	°C
		7 suffix version	− 40		125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
3. When the ADC is used, refer to *Table 74: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. The over-drive mode is not supported when the internal regulator is OFF.
7. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 22. reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are sbject to general operating conditions for T_A.

Table 23. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

Table 33. Tyical current consumption in Sleep mode, regulator OFF(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	
I_{DD12}/I_{DD}	Supply current in Sleep mode from V_{12} and V_{DD} supply	All Peripherals enabled	180	61.5	1.4	-	-	mA
			168	59.4	1.3	59.4	1.0	
			150	53.9	1.3	53.9	1.0	
			144	49.0	1.3	49.0	1.0	
			120	38.0	1.2	38.0	0.9	
			90	29.3	1.4	29.3	1.1	
			60	20.2	1.2	20.2	0.9	
			30	11.9	1.2	11.9	0.9	
			25	10.4	1.2	10.4	0.9	
		All Peripherals disabled	180	14.9	1.4	-	-	
			168	14.0	1.3	14.0	1.0	
			150	12.6	1.3	12.6	1.0	
			144	11.5	1.3	11.5	1.0	
			120	8.7	1.2	8.7	0.9	
			90	7.1	1.4	7.1	1.1	
			60	5.0	1.2	5.0	0.9	
			30	3.1	1.2	3.1	0.9	
			25	2.8	1.2	2.8	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 38* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 38. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 27. High-speed external clock source AC timing diagram

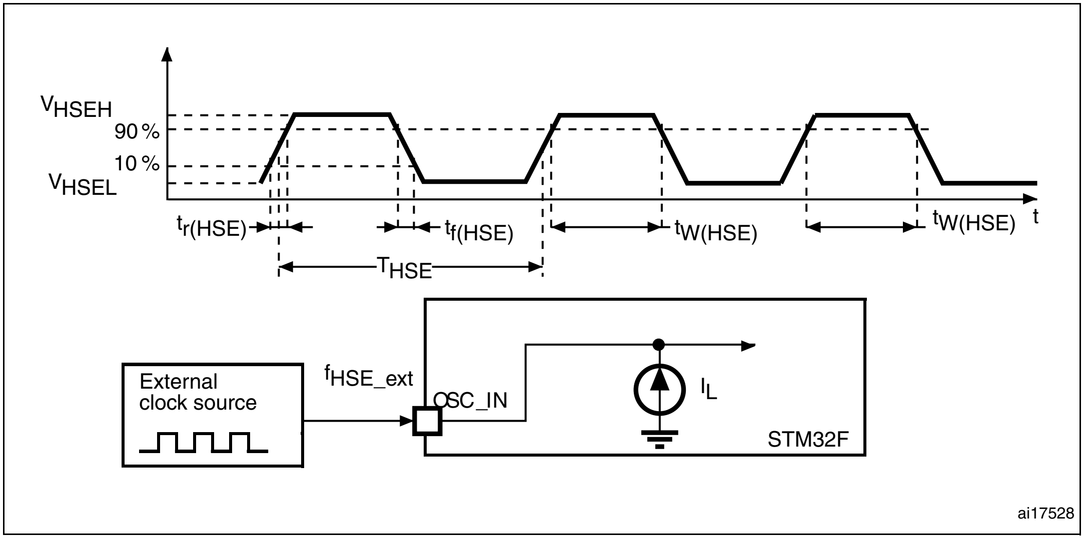
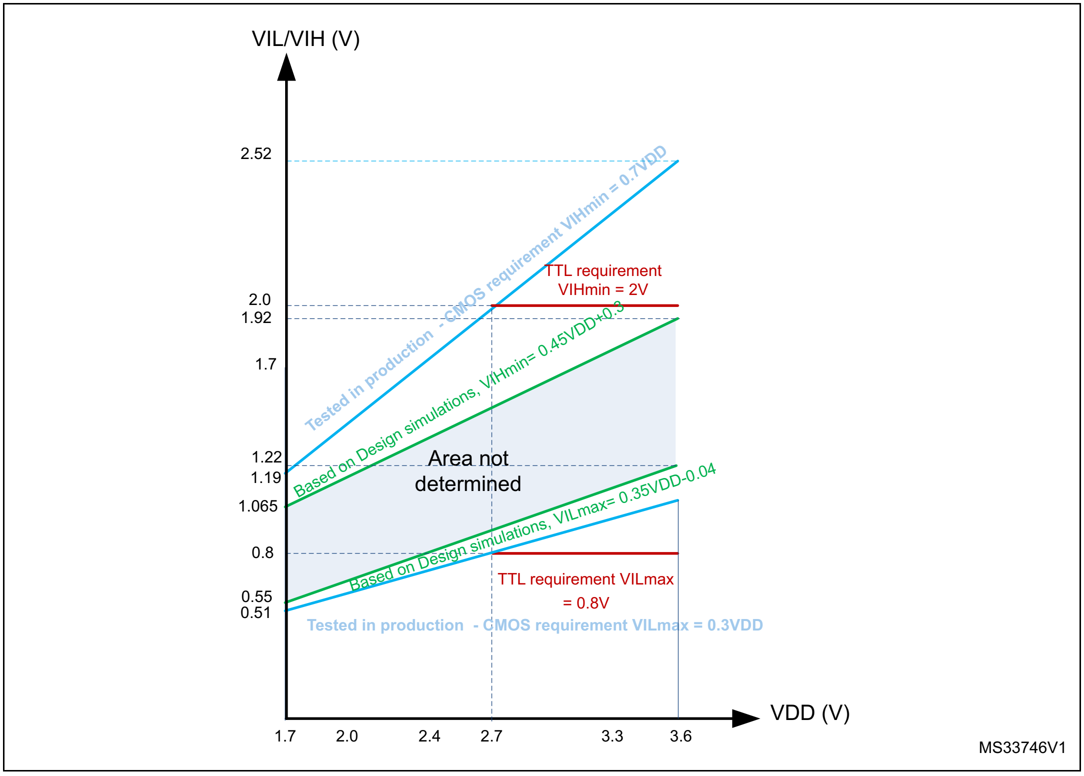


Figure 35. FT I/O input characteristics



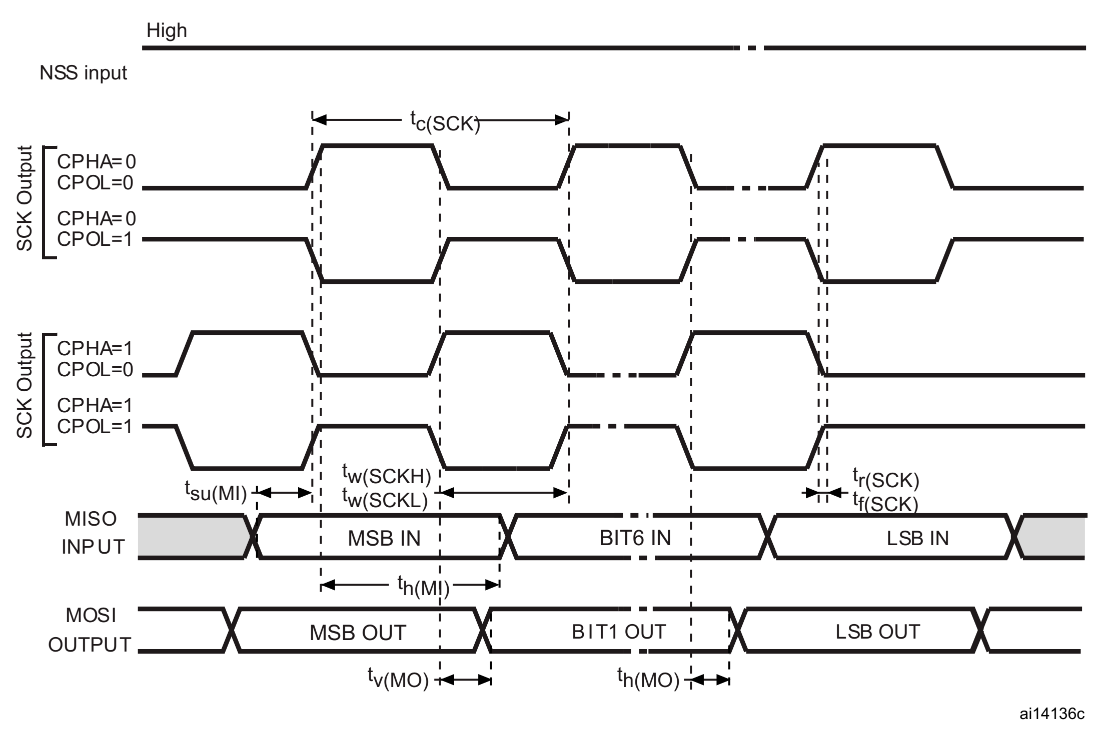
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 15*).

Figure 40. SPI timing diagram - master mode



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 65. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

Table 66. USB OTG full speed DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG full speed transceiver operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

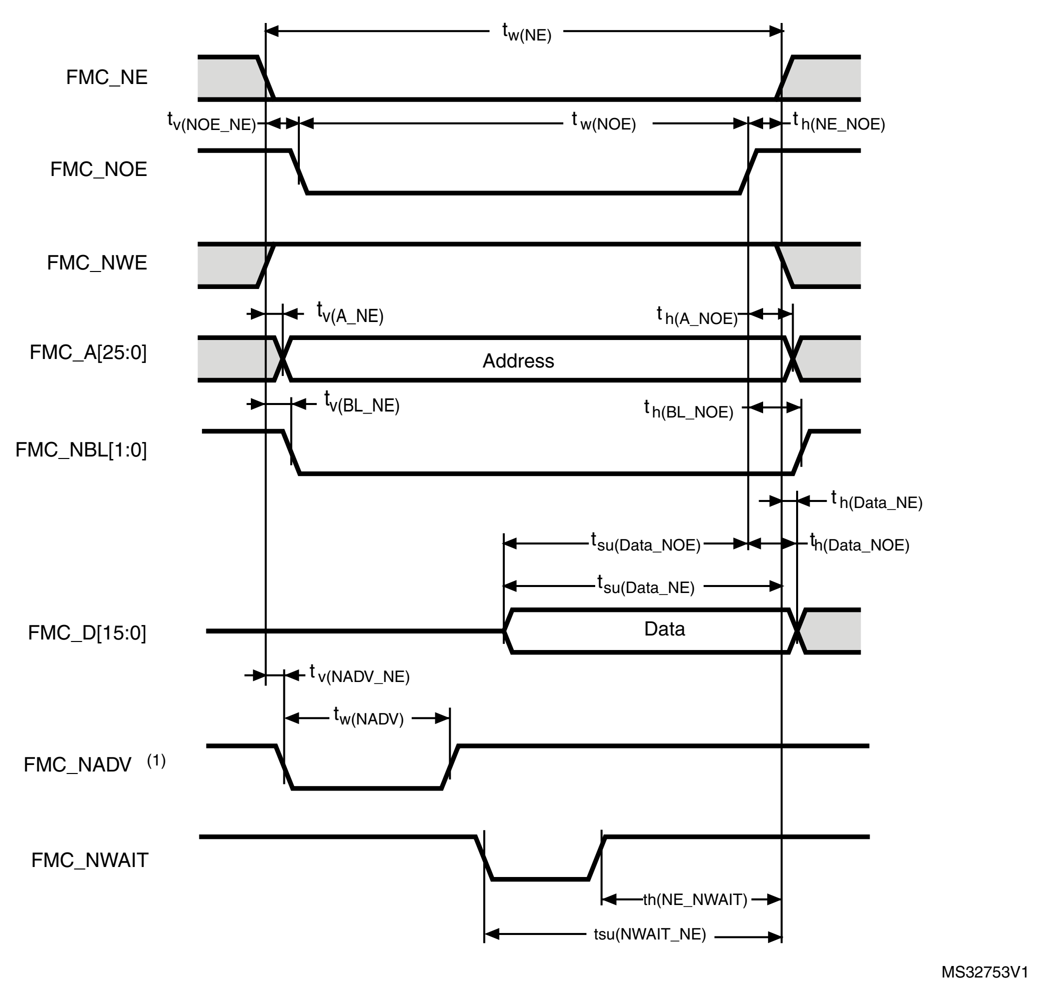
Note: *When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.*

6.3.25 DAC electrical characteristics

Table 85. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	-		1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	-		1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	-		0	-	0	V	-
R_{LOAD}(2)	Resistive load	DAC output buffer ON	R_{LOAD} connected to V_{SSA}	5	-	-	kΩ	-
			R_{LOAD} connected to V_{DDA}	25				-
R_O(2)	Impedance output with buffer OFF	-		-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-		-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	-		0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-		-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-		-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-		-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-		-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 0.5$	$2\ T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	ns
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$	$2T_{HCLK}+ 0.5$	ns
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 2.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} +2$	-	ns

Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}–1$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 59 through *Figure 62* represent synchronous waveforms and *Table 94* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

Table 104. SDRAM write timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	3.5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	1	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_\ SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	
$t_{d(SDCLKL\_NBL)}$	NBL valid time	-	0.5	
$t_{h(SDCLKL\_NBL)}$	NBLoutput time	0	-	

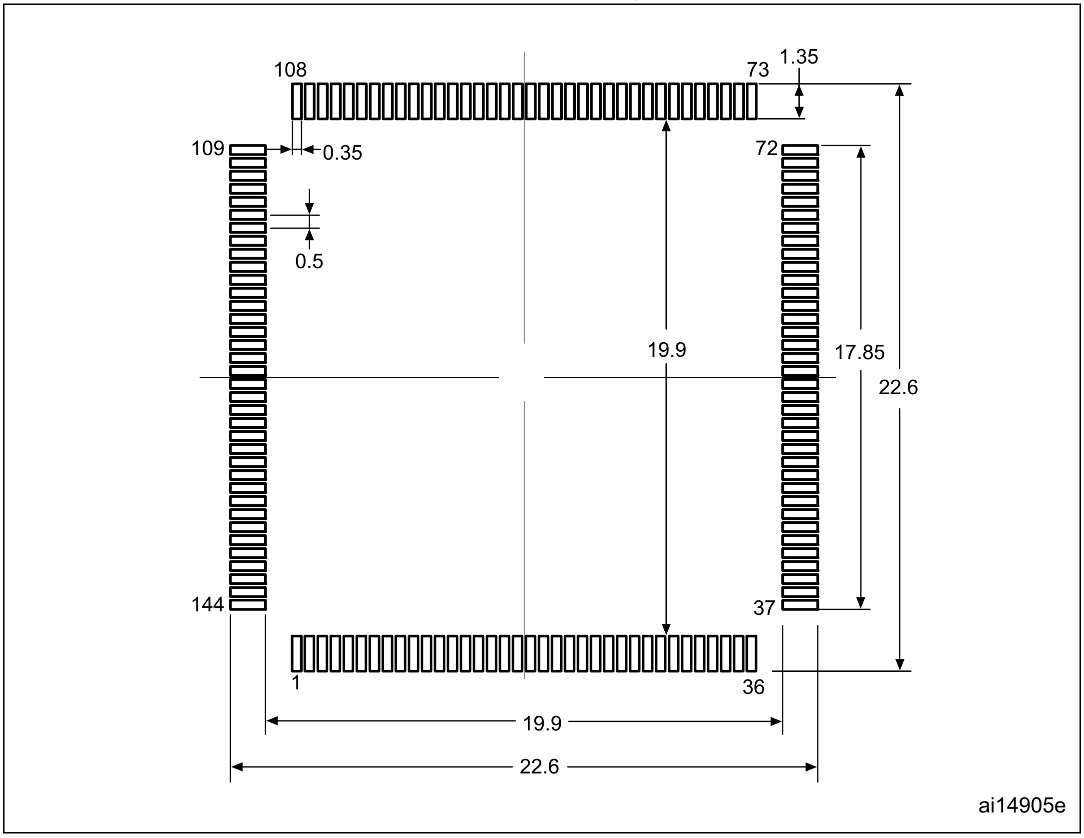
1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.
2. Guaranteed by characterization results.

Table 105. LPSDR SDRAM write timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	2	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.8	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	1	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	1.5	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	1.5	-	
$t_{d(SDCLKL\_NBL)}$	NBL valid time	-	1.5	
$t_{h(SDCLKL-NBL)}$	NBL output time	1.5	-	

1. CL = 10 pF.
2. Guaranteed by characterization results.

Figure 87. LQPF144- 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.