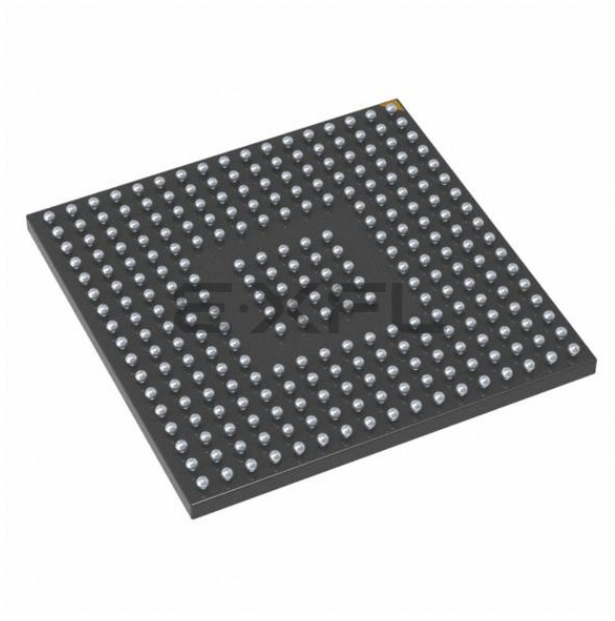

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f439iih6tr

The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

– In Stop modes

The MR can be configured in two ways during stop mode:

MR operates in normal mode (default mode of MR in stop mode)

MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:

  – LPR operates in normal mode (default mode when LPR is ON)

  – LPR operates in under-drive mode (reduced leakage mode).

- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 22: Power supply scheme* and *Table 19: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

3.18.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 17: General operating conditions*.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 22: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
35	46	N4	R5	56	N8	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
36	47	K5	R4	57	K7	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
37	48	L5	M6	58	L7	63	M5	PB2-BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	M5	R6	59	M7	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	N5	P6	60	N7	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	51	G9	M8	61	-	72	K7	V_{SS}	S		-	-	-
-	52	D10	N8	62	-	73	L8	V_{DD}	S		-	-	-
-	53	M6	N6	63	K6	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	54	K7	R7	64	L6	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	55	L7	P7	65	M6	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	56	N6	N7	66	N6	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	M7	67	K5	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
51	73	N12	P12	92	M2	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	M12	P13	93	N1	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	M13	R14	94	K3	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	76	L13	R15	95	J3	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	77	L12	P15	96	L2	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
56	78	K13	P14	97	M1	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	79	K11	N15	98	H4	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-

Table 12. STM32F437xx and STM32F439xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port F	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	-	TIM13_CH1	-	-	FMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	-	TIM14_CH1	-	-	FMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INTR	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	-	-	FMC_SDNRAS	DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INT2	DCMI_D12	LCD_R7	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT3	DCMI_D13	LCD_CLK	EVENTOUT
	PG8	-	-	-	-	-	SPI6_NSS	-	-	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK	-	-	EVENTOUT

6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 36* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

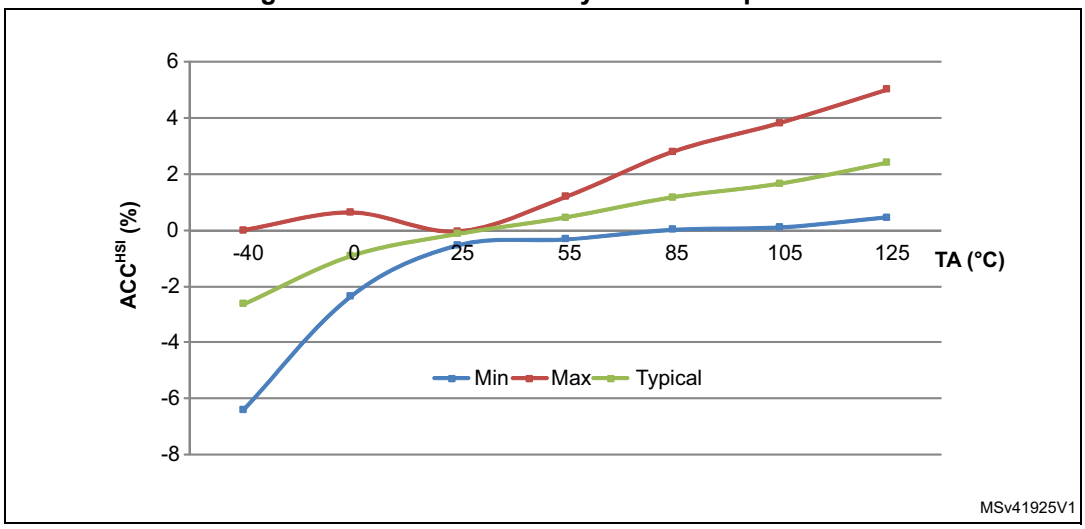
All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	6	-	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	13.6	-	µs
		Main regulator is ON and Flash memory in Deep power down mode	93	111	
		Low power regulator is ON	22	32	
		Low power regulator is ON and Flash memory in Deep power down mode	103	126	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	105	128	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	125	155	
tWUSTDBY (2)(3)	Wakeup from Standby mode		318	412	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3. $t_{WUSTDBY}$ maximum value is given at –40 °C.

Figure 31. ACCHSI accuracy versus temperature



1. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Table 43. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 44. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)			0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock			-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output			100	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps

Table 48. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{BE}	Bank erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
t_{BE}	Bank erase time		-	6.9	-	s
V_{prog}	Programming voltage		2.7	-	3.6	V
V_{PP}	V_{PP} voltage range		7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin		10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied		-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 55: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 55: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 35*.

Output voltage levels

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(5)	-	

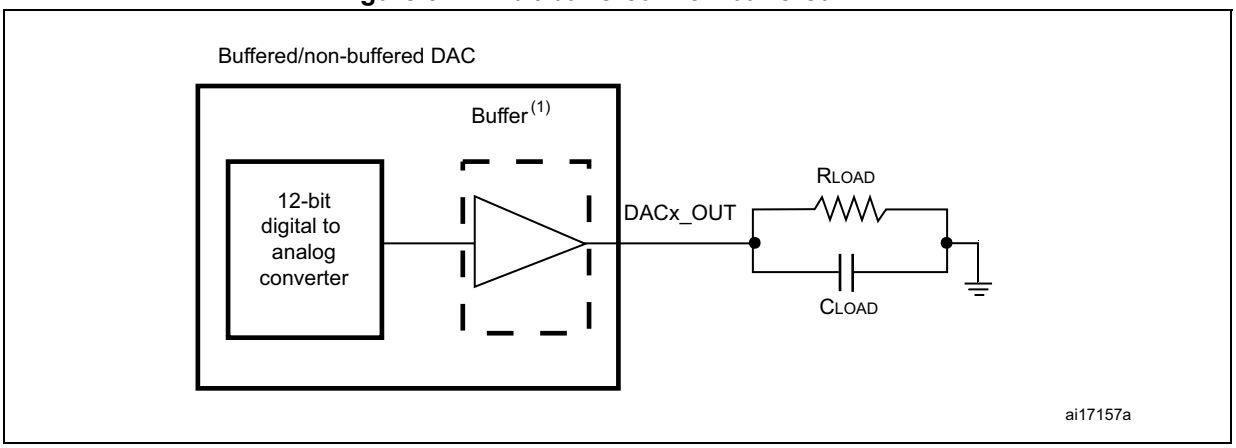
1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 54. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms

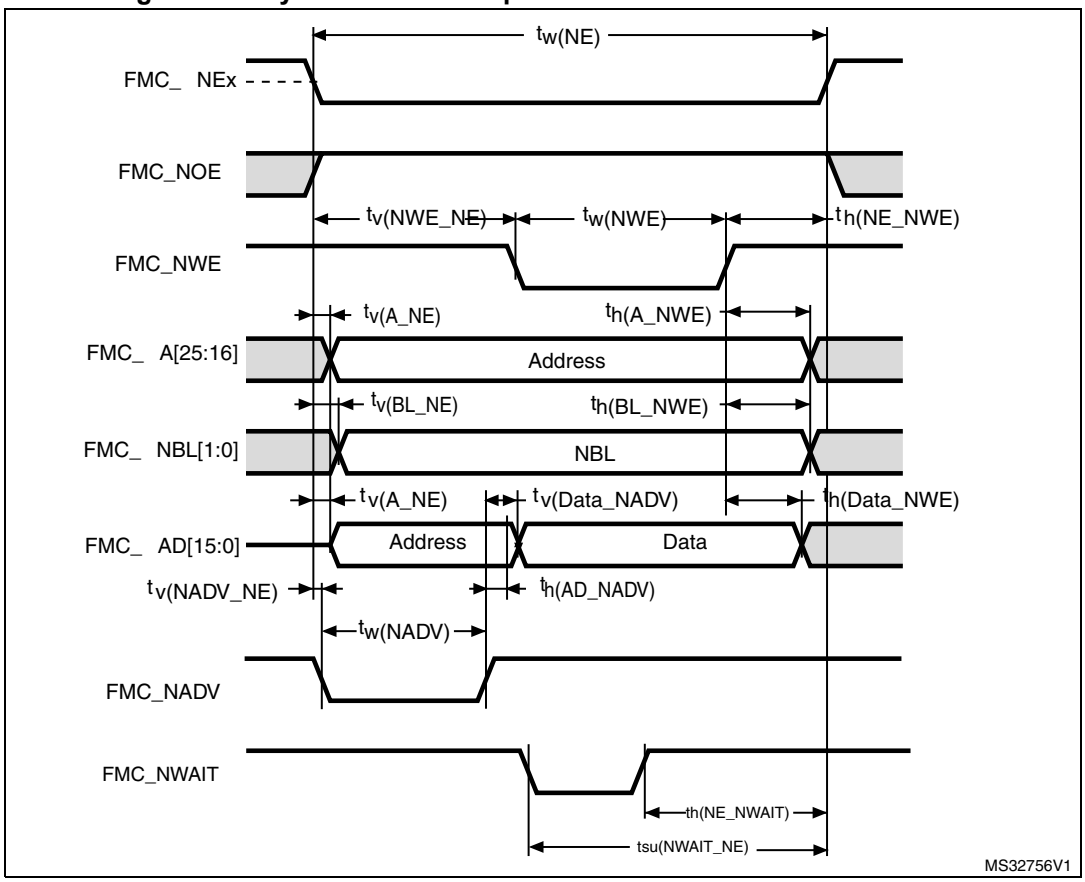


Table 92. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{HCLK} - 2$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK}+1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 97. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	ns
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	ns
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}−0.5	-	ns
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	2.5	ns
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	ns
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}−0.5	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4		
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0		

1. C_L = 30 pF.
2. Guaranteed by characterization results.

PC Card/CompactFlash controller waveforms and timings

Figure 63 through *Figure 68* represent synchronous waveforms, and *Table 98* and *Table 99* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x04;
- COM.FMC_WaitSetupTime = 0x07;
- COM.FMC_HoldSetupTime = 0x04;
- COM.FMC_HiZSetupTime = 0x00;
- ATT.FMC_SetupTime = 0x04;
- ATT.FMC_WaitSetupTime = 0x07;
- ATT.FMC_HoldSetupTime = 0x04;
- ATT.FMC_HiZSetupTime = 0x00;
- IO.FMC_SetupTime = 0x04;
- IO.FMC_WaitSetupTime = 0x07;
- IO.FMC_HoldSetupTime = 0x04;
- IO.FMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 102. SDRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

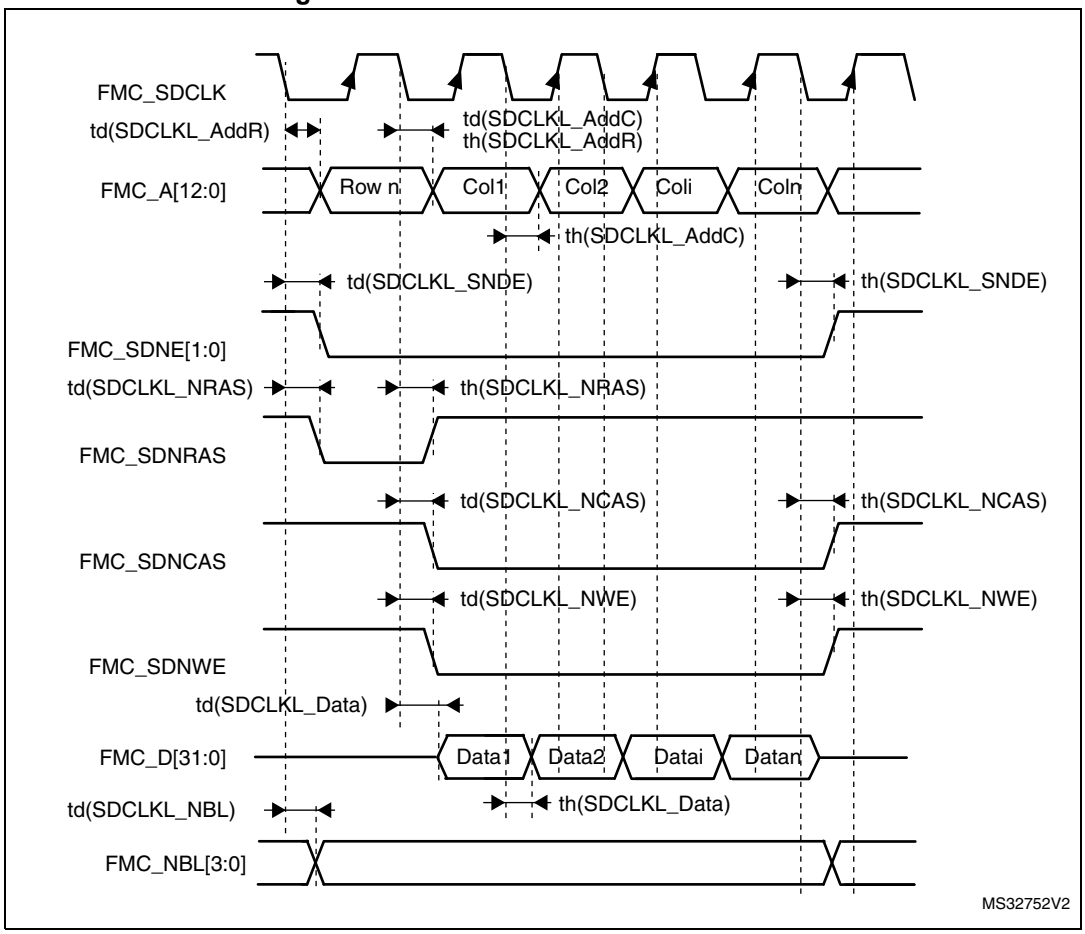
1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.
2. Guaranteed by characterization results.

Table 103. LPSDR SDRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	1	-	

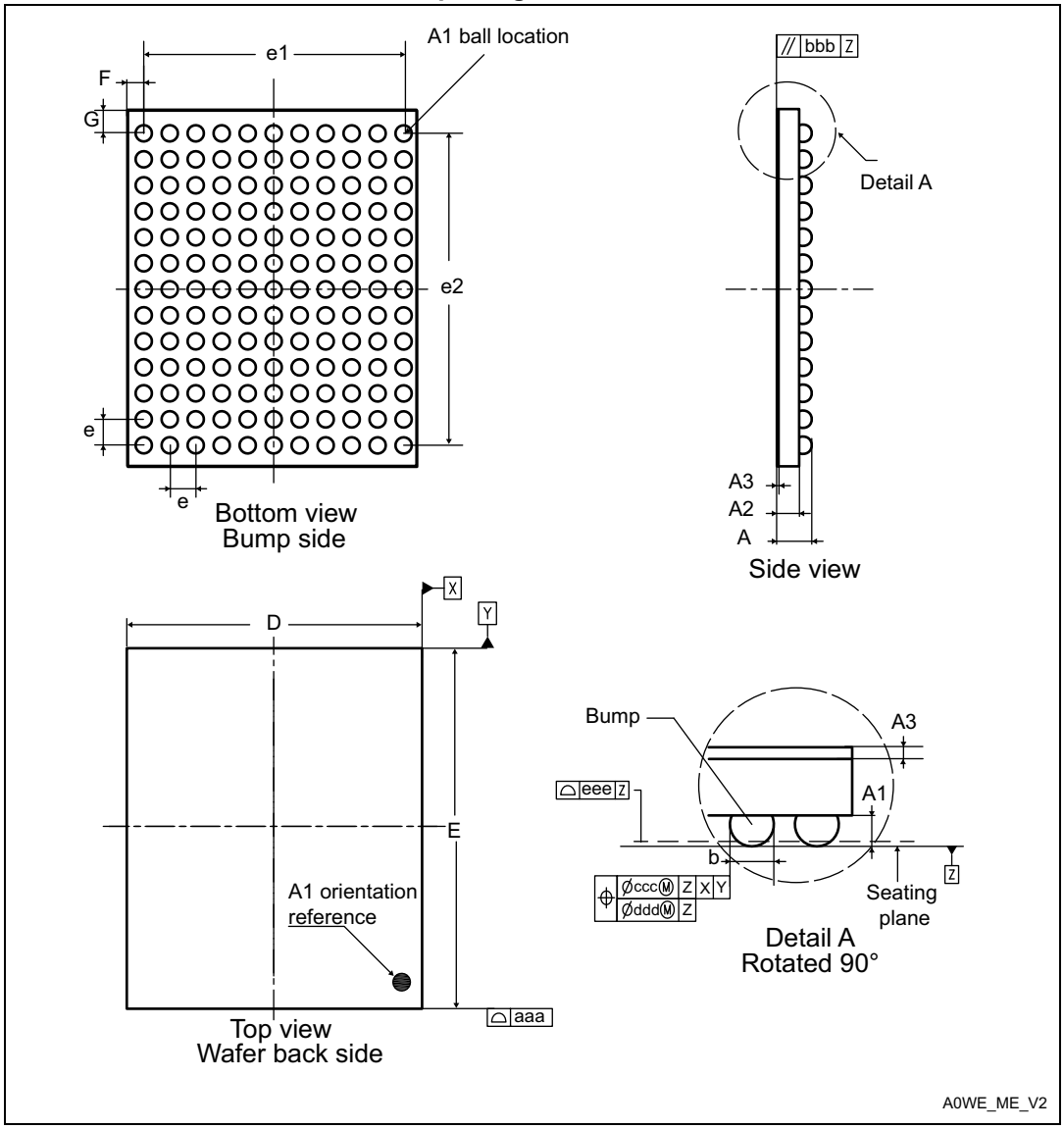
1. CL = 10 pF.
2. Guaranteed by characterization results.

Figure 74. SDRAM write access waveforms



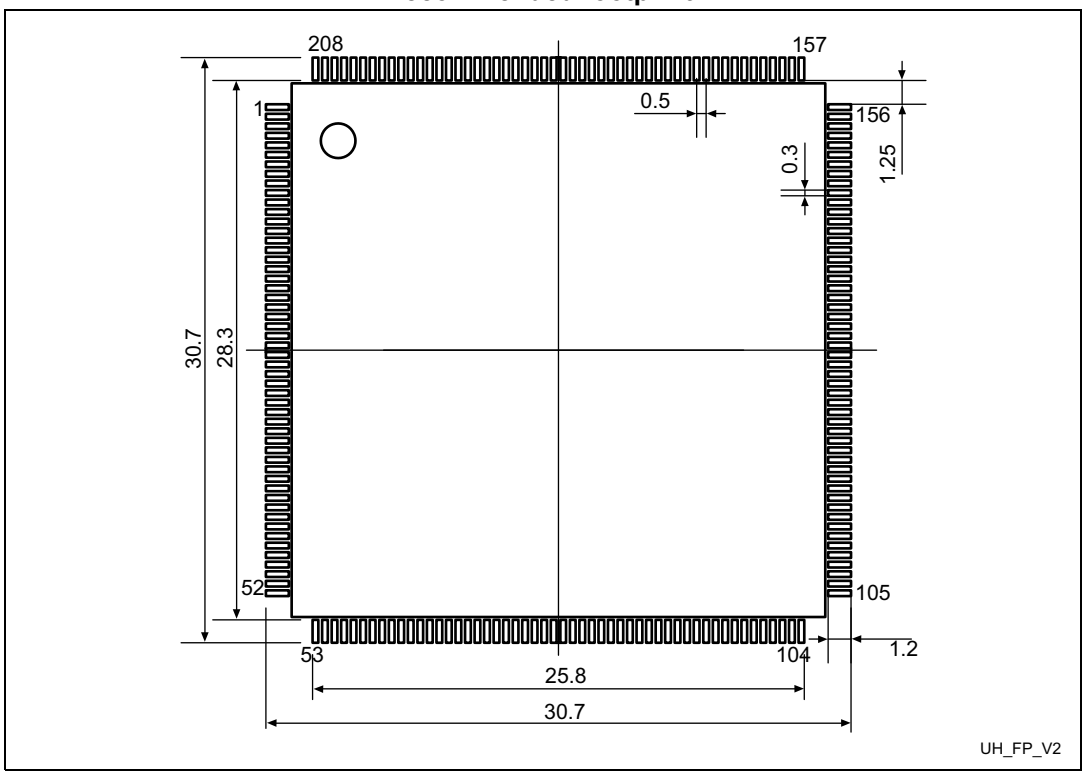
7.2 WLCSP143 package information

Figure 83. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 99. UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

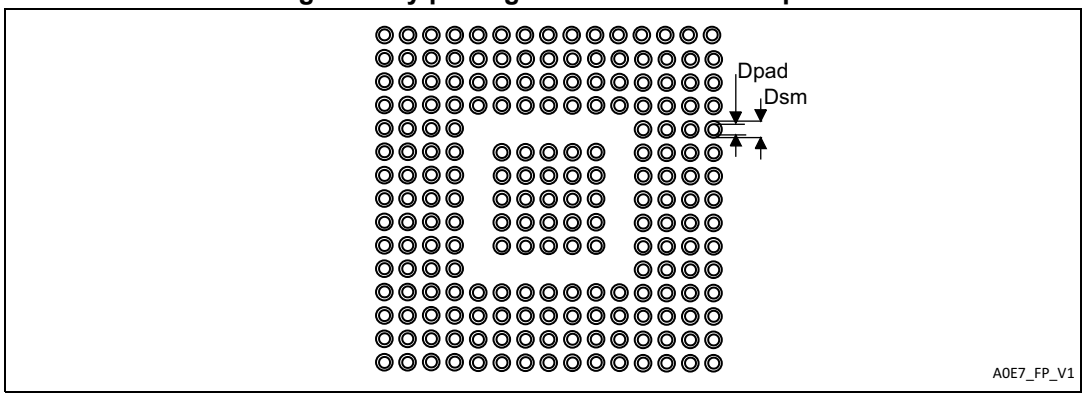
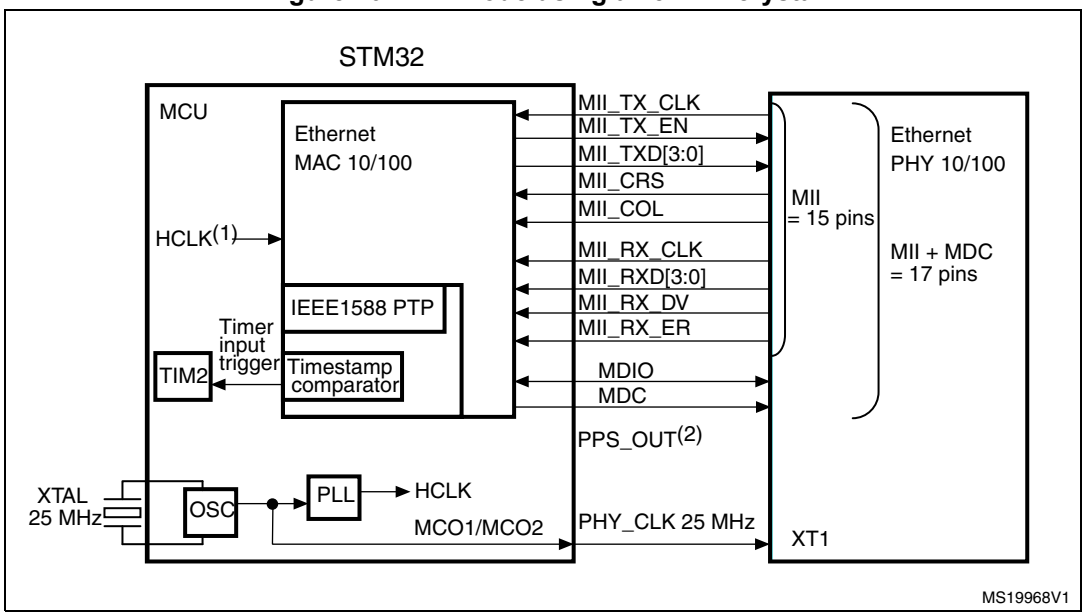


Table 119. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

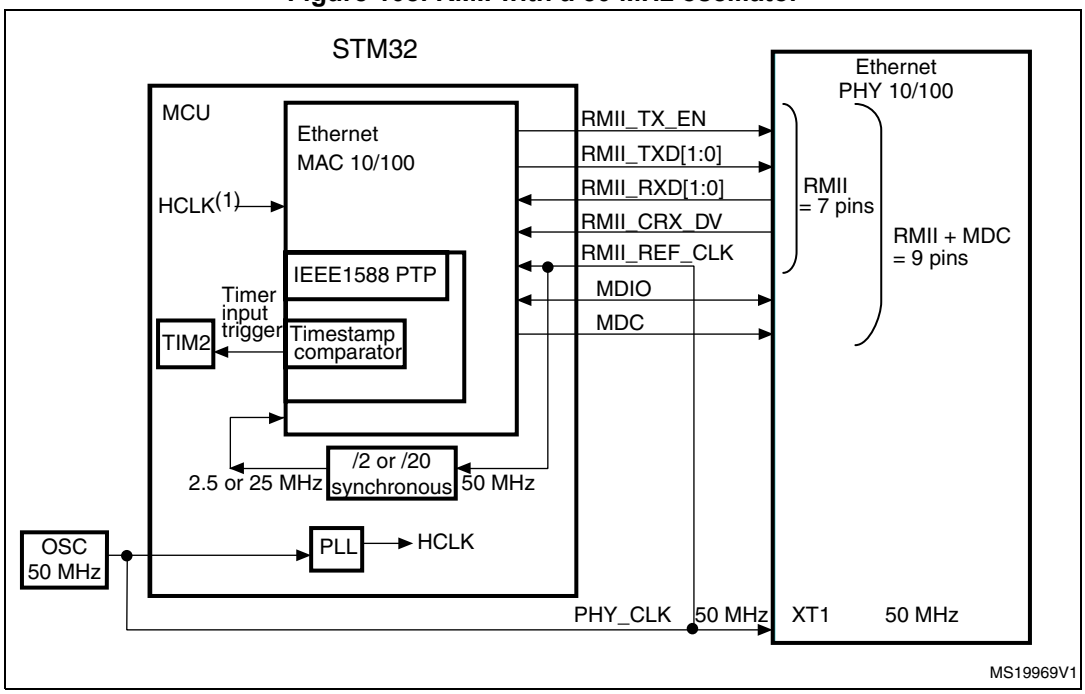
B.3 Ethernet interface solutions

Figure 107. MII mode using a 25 MHz crystal



1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 108. RMII with a 50 MHz oscillator



1. f_{HCLK} must be greater than 25 MHz.