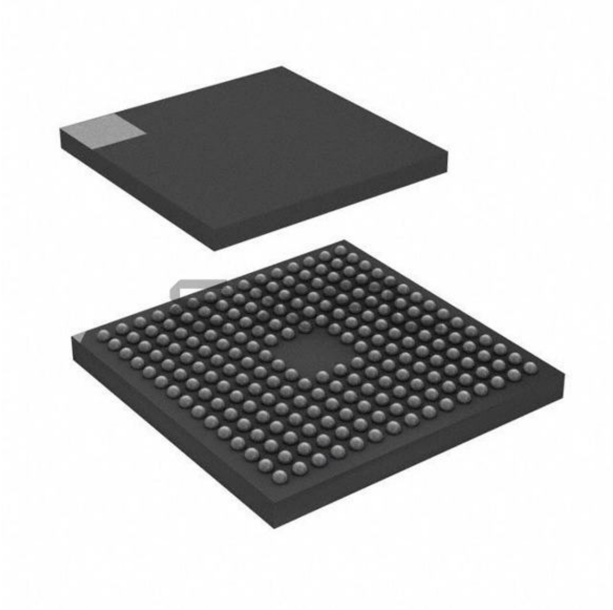
STMicroelectronics - STM32F439NGH6 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f439ngh6

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  - Normal mode (default mode when MR or LPR is enabled)
  - Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

  The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F437xx and STM32F439xx pin and ball definitions

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
1	1	B2	A2	1	D8	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	C1	A1	2	C10	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	3	C2	B1	3	B11	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
38	58	N7	R8	68	L5	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, FMC_D4, EVENTOUT	-
39	59	J8	P8	69	M5	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, FMC_D5, EVENTOUT	-
40	60	K8	P9	70	N5	81	P9	PE9	I/O	FT	-	TIM1_CH1, FMC_D6, EVENTOUT	-
-	61	J6	M9	71	H3	82	K8	V_{SS}	S		-		-
-	62	G10	N9	72	J5	83	L9	V_{DD}	S		-		-
41	63	L8	R9	73	J4	84	R9	PE10	I/O	FT	-	TIM1_CH2N, FMC_D7, EVENTOUT	-
42	64	M8	P10	74	K4	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, FMC_D8, LCD_G3, EVENTOUT	-
43	65	N8	R10	75	L4	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, FMC_D9, LCD_B4, EVENTOUT	-
44	66	H9	N11	76	N4	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, FMC_D10, LCD_DE, EVENTOUT	-
45	67	J9	P11	77	M4	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, FMC_D11, LCD_CLK, EVENTOUT	-
46	68	K9	R11	78	L3	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
47	69	L9	R12	79	M3	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
48	70	M9	R13	80	N3	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-

Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port G	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FMC_NE2/FMC_NCE3	DCMI_VSYNC(1)	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_NCE4_1/FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_NCE4_2	DCMI_D3	LCD_B3	EVENTOUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	-	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	-	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	FMC_SDNE1	DCMI_D8	-	-

Table 28. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	2.80	3.00	3.60	7.00	19.00	36.00	µA
		Backup SRAM OFF, low-speed oscillator (LSE) and RTC ON	2.30	2.60	3.10	6.00	16.00	31.00	
		Backup SRAM ON, RTC and LSE OFF	2.30	2.50	2.90	6.00(3)	18.00(3)	35.00(3)	
		Backup SRAM OFF, RTC and LSE OFF	1.70	1.90	2.20	5.00(3)	15.00(3)	30.00(3)	

1. The typical current consumption values are given with PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 29. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions(1)	Typ			Max(2)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	1.28	1.40	1.62	6	11	µA
		Backup SRAM OFF, low-speed oscillator (LSE) and RTC ON	0.66	0.76	0.97	3	5	
		Backup SRAM ON, RTC and LSE OFF	0.70	0.72	0.74	5	10	
		Backup SRAM OFF, RTC and LSE OFF	0.10	0.10	0.10	2	4	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

Table 34. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I_{DDIO}	I/O switching Current	V_{DD} = 3.3 V C= C_{INT}(2)	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	
I_{DDIO}	I/O switching Current	V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.18	mA
			8 MHz	0.67	
			25 MHz	2.09	
			50 MHz	3.6	
			60 MHz	4.5	
			84 MHz	7.8	
			90 MHz	9.8	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.26	
			8 MHz	1.01	
			25 MHz	3.14	
			50 MHz	6.39	
			60 MHz	10.68	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + Cext + C_S	2 MHz	0.33	
			8 MHz	1.29	
			25 MHz	4.23	
			50 MHz	11.02	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP176 package pin (pad removal).

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 45 MHz)	TIM2	17.56	16.42	14.47	µA/MHz
	TIM3	14.22	13.36	11.80	
	TIM4	14.89	13.64	12.13	
	TIM5	17.33	16.42	14.47	
	TIM6	2.89	2.53	2.47	
	TIM7	3.11	2.81	2.47	
	TIM12	7.33	6.97	6.13	
	TIM13	4.89	4.47	4.13	
	TIM14	5.56	5.31	4.80	
	PWR	11.11	10.31	9.13	
	USART2	4.22	3.92	3.47	
	USART3	4.44	4.19	3.80	
	UART4	4.00	3.92	3.47	
	UART5	4.00	3.92	3.47	
	UART7	4.00	3.92	3.47	
	UART8	3.78	3.92	3.47	
	I2C1	4.00	3.92	3.47	
	I2C2	4.00	3.92	3.47	
	I2C3	4.00	3.92	3.47	
	SPI2[3]	3.11	3.08	2.80	
	SPI3[3]	3.56	3.36	3.13	
	I2S2	2.89	2.81	2.47	
	I2S3	3.33	3.08	2.80	
	CAN1	6.89	6.42	5.80	
	CAN2	6.67	6.14	5.47	
	DAC[4]	2.89	2.25	2.13	
	WWDG	0.89	0.86	0.80	

6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 36* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	6	-	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	13.6	-	µs
		Main regulator is ON and Flash memory in Deep power down mode	93	111	
		Low power regulator is ON	22	32	
		Low power regulator is ON and Flash memory in Deep power down mode	103	126	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	105	128	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	125	155	
tWUSTDBY (2)(3)	Wakeup from Standby mode		318	412	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3. $t_{WUSTDBY}$ maximum value is given at –40 °C.

Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

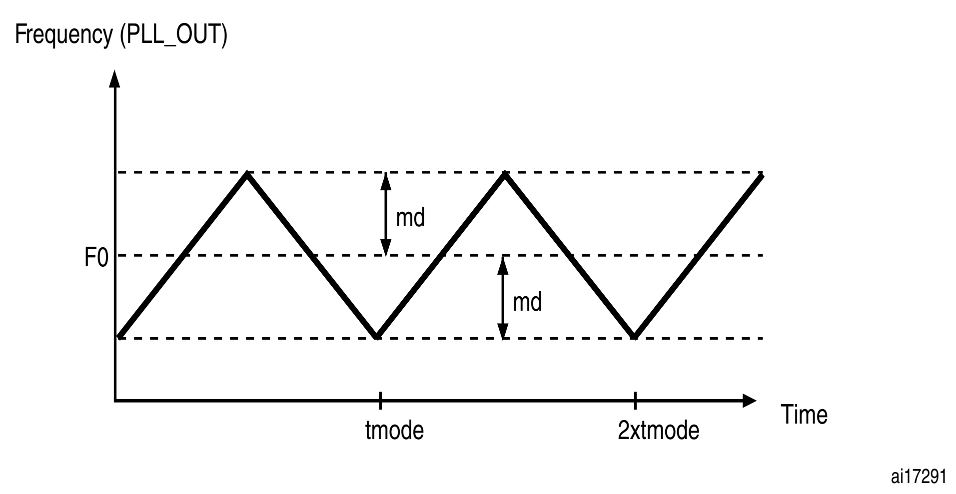
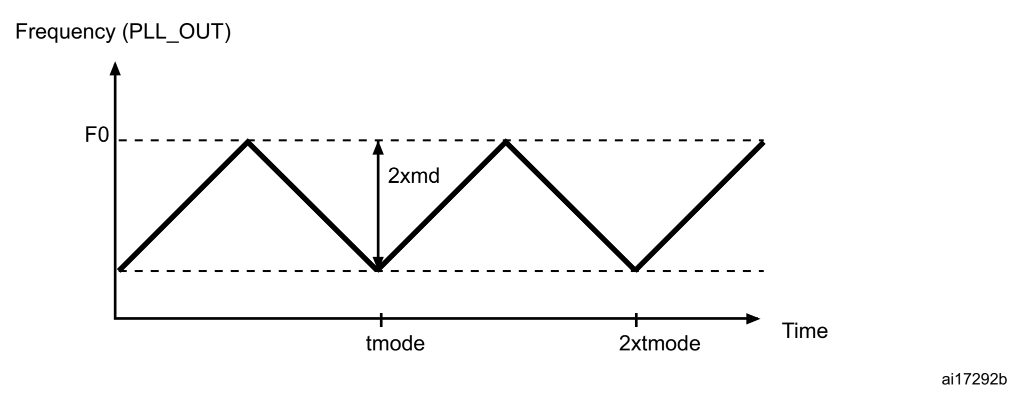


Figure 34. PLL output clock waveforms in down spread mode



6.3.13 Memory characteristics

Flash memory

The characteristics are given at TA = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 47. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 48. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

Table 62. SPI dynamic characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, 2.7 V≤V_{DD}≤3.6 V	$T_{PCLK}-0.5$	T_{PCLK}	$T_{PCLK}+0.5$	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, 1.7 V≤V_{DD}≤3.6 V	$T_{PCLK}-2$	T_{PCLK}	$T_{PCLK}+2$	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$			
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	0	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	0.5	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, SPI presc = 2	0	-	$4T_{PCLK}$	
$t_{dis(SO)}$	Data output disable time	Slave mode, SPI1/4/5/6, 2.7 V≤V_{DD}≤3.6 V	0	-	8.5	
		Slave mode, SPI1/2/3/4/5/6 and 1.7 V≤V_{DD}≤3.6 V	0	-	16.5	
$t_{v(SO)}$ $t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge), SPI1/4/5/6 and 2.7V ≤ V_{DD} ≤ 3.6V	-	11	13	ns
		Slave mode (after enable edge), SPI2/3, 2.7 V≤V_{DD}≤3.6 V	-	14	15	
		Slave mode (after enable edge), SPI1/4/5/6, 1.7 V≤V_{DD}≤3.6 V	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, 1.7 V≤V_{DD}≤3.6 V	-	15.5	17.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge), SPI1/4/5/6, 2.7 V≤V_{DD}≤3.6 V	-	-	2.5	
		Master mode (after enable edge), SPI1/2/3/4/5/6, 1.7 V≤V_{DD}≤3.6 V	-	-	4.5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 43. SAI master timing waveforms

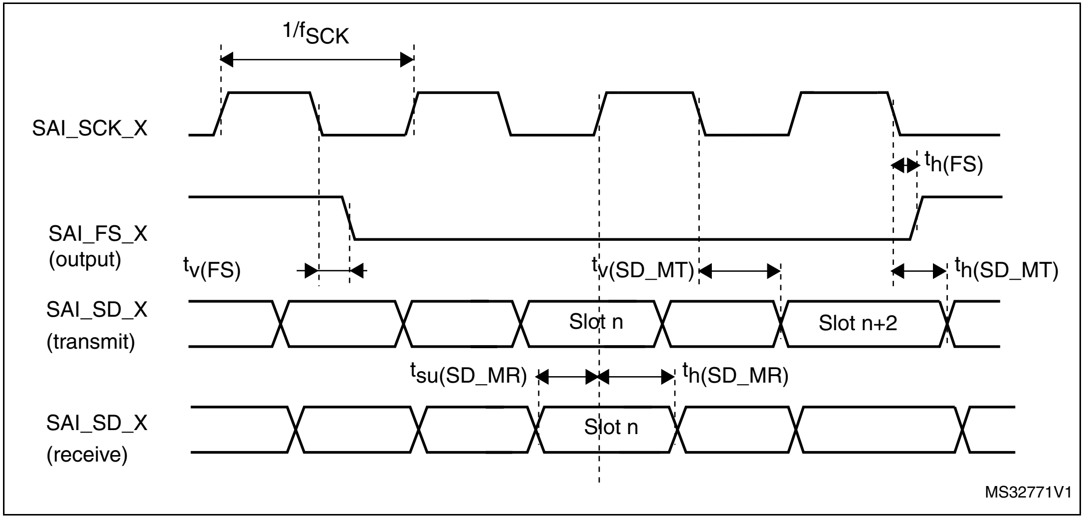
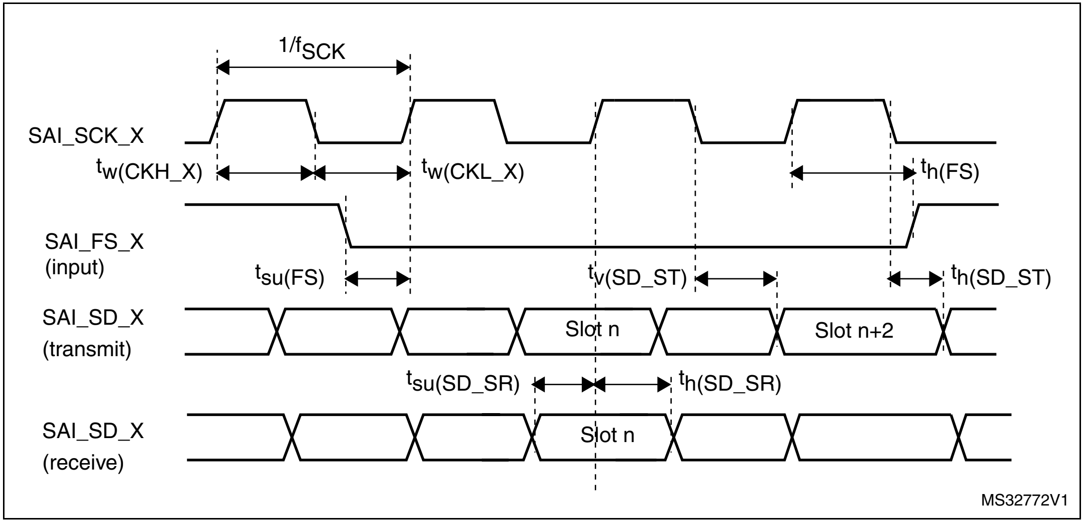


Figure 44. SAI slave timing waveforms



Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 71*, *Table 72* and *Table 73* for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 17* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF for 2.7 V < V_{DD} < 3.6 V
- Capacitive load C = 20 pF for 1.71 V < V_{DD} < 3.6 V
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 71 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 47* shows the corresponding timing diagram.

Figure 47. Ethernet SMI timing diagram

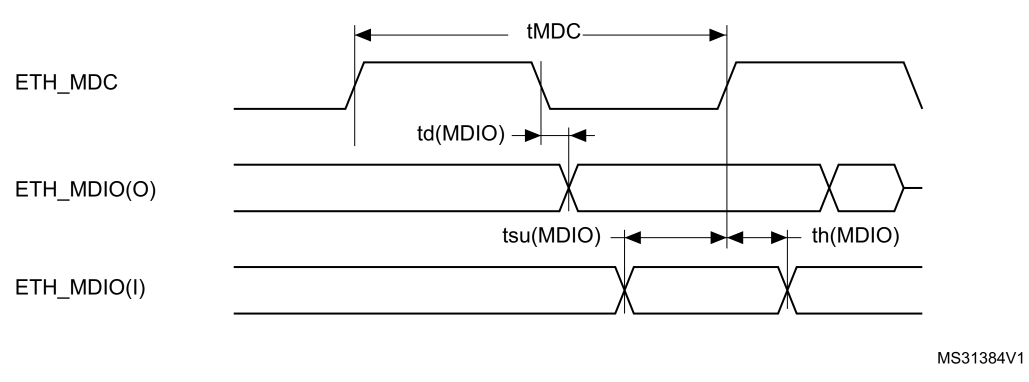
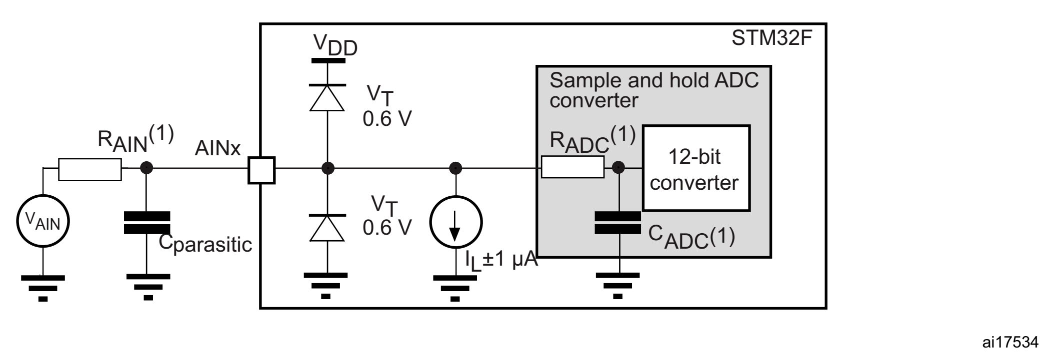


Table 71. Dynamics characteristics: Ethernet MAC signals for SMI[1]

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_{d(MDIO)}$	Write data valid time	6	10	13	
$t_{su(MDIO)}$	Read data setup time	12	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

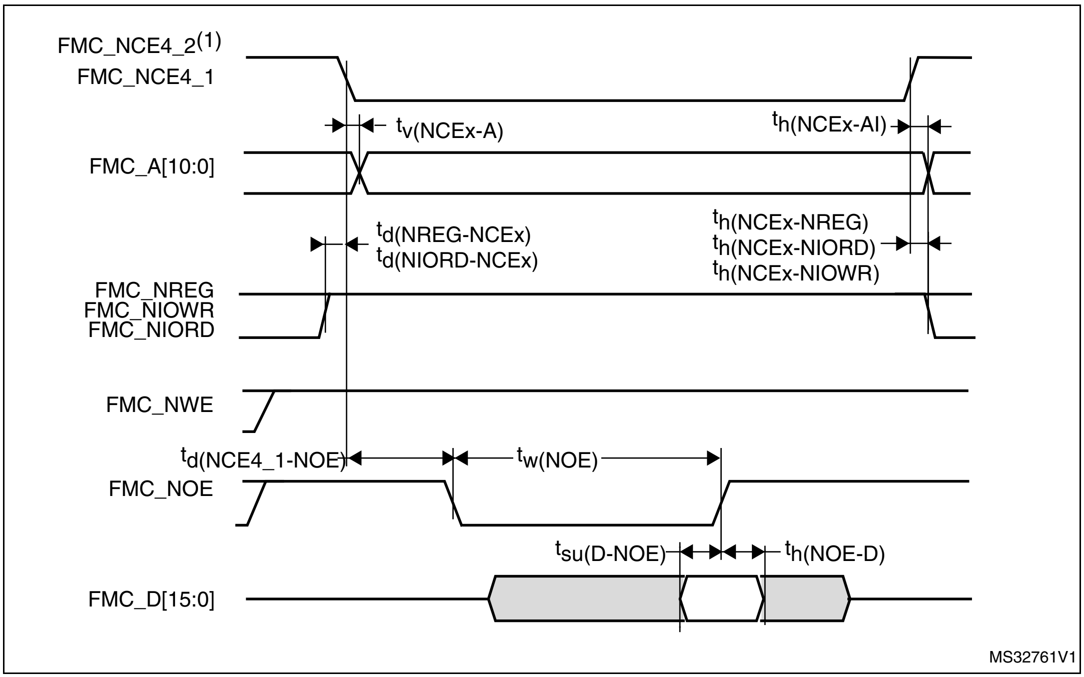
1. Guaranteed by characterization results.

Figure 51. Typical connection diagram using the ADC



1. Refer to *Table 74* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 63. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 64. PC Card/CompactFlash controller waveforms for common memory write access

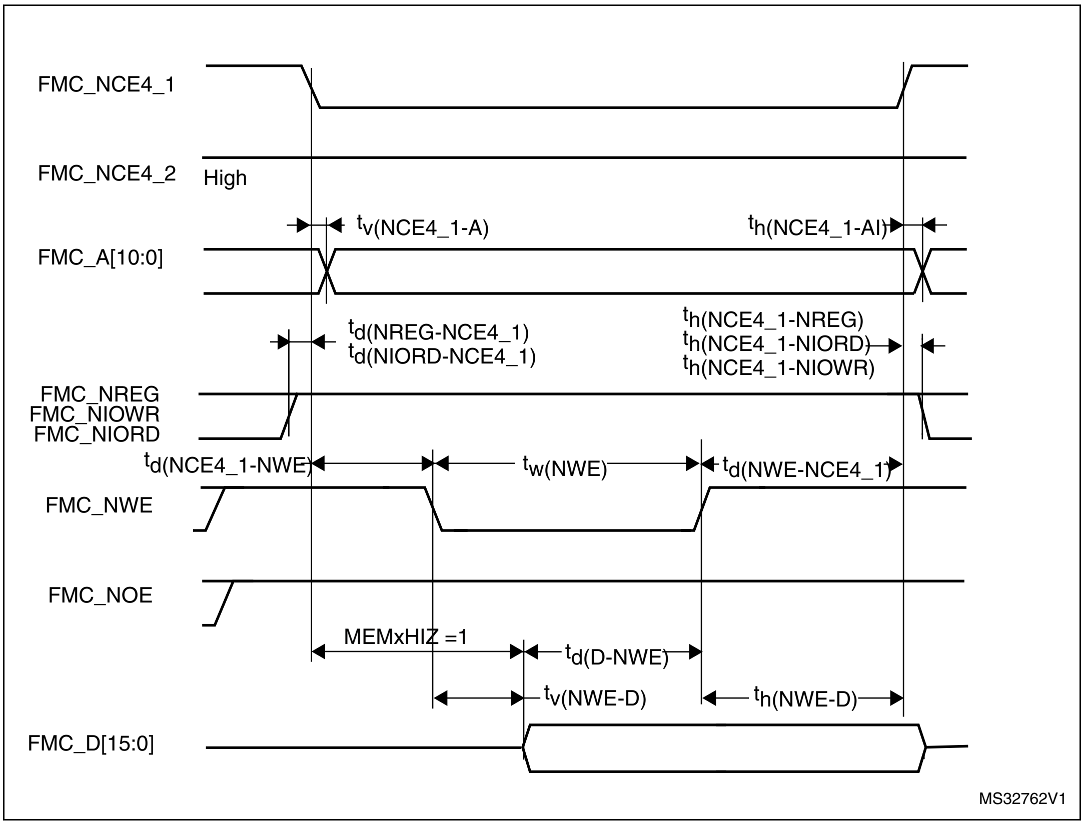


Table 102. SDRAM read timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.
2. Guaranteed by characterization results.

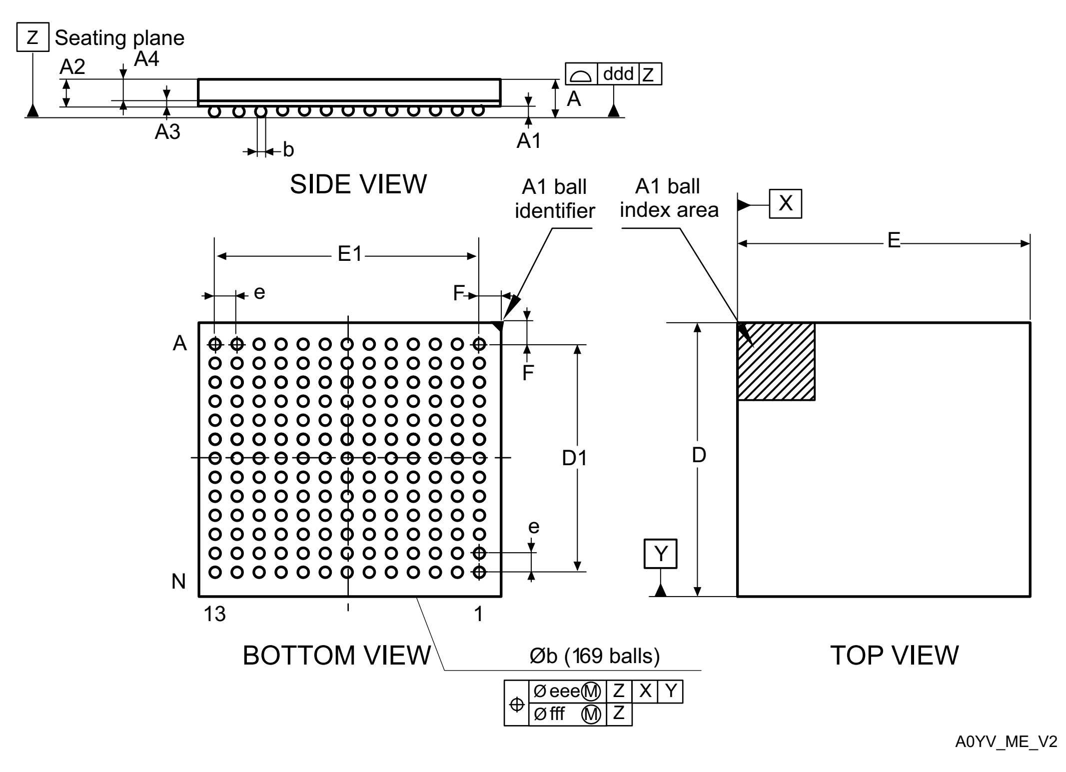
Table 103. LPSDR SDRAM read timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	1	-	

1. CL = 10 pF.
2. Guaranteed by characterization results.

7.6 UFBGA169 package information

Figure 95. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline



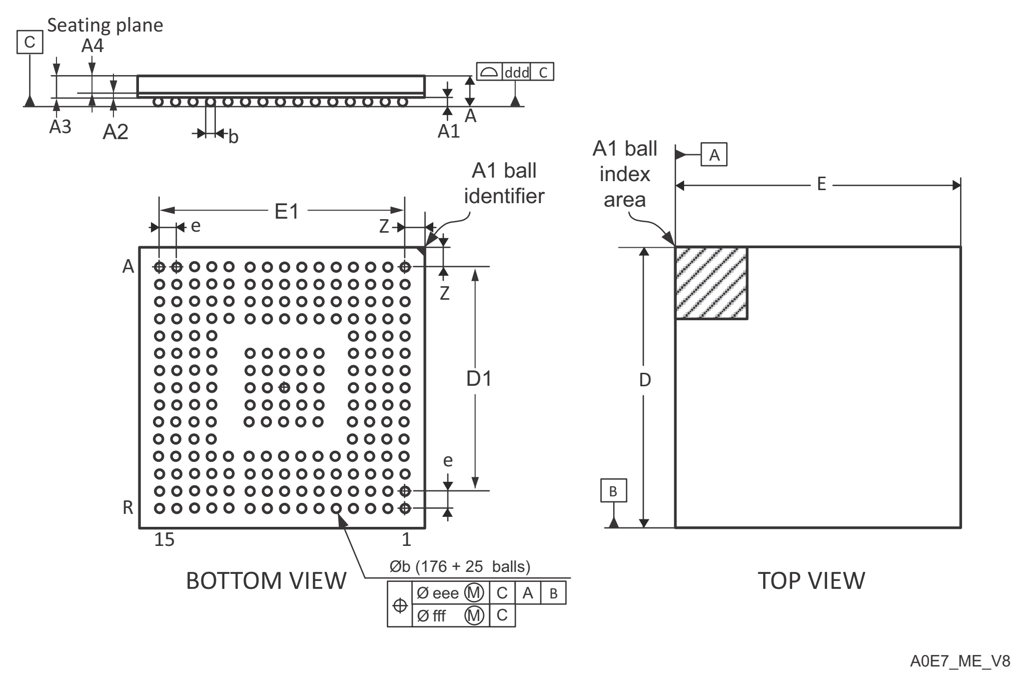
1. Drawing is not to scale.

Table 116. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-

7.7 UFBGA176+25 package information

Figure 98. UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline



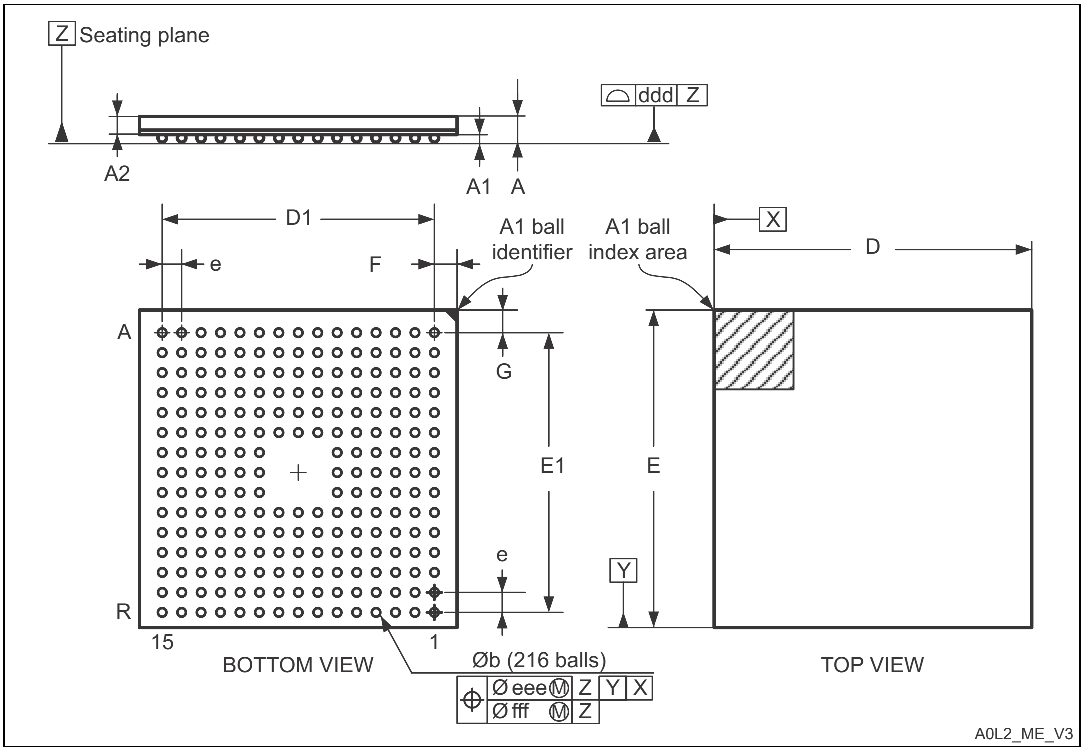
1. Drawing is not to scale.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

7.8 TFBGA216 package information

Figure 101. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039

Table 124. Document revision history (continued)

Date	Revision	Changes
28-Sep-2015	7	Updated notes related to the minimum and maximum values guaranteed by design, characterization or test in production. Updated $I_{DD\_STOP\_UDM}$ in *Table 27: Typical and maximum current consumptions in Stop mode*. Removed note related to tests in production in *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM* and *Table 26: Typical and maximum current consumption in Sleep mode*. Updated *Table 41: HSI oscillator characteristics*. *Figure 31* renamed *ACCHSI accuracy versus temperature* and updated. Updated *Figure 38: SPI timing diagram - slave mode and CPHA = 0*. Updated *Section : Ethernet characteristics*. Updated *Table 43: Main PLL characteristics*, *Table 44: PLLI2S (audio PLL) characteristics* and *Table 45: PLLISAI (audio and LCD-TFT PLL) characteristics*. Removed note 1 in *Table 75: ADC static accuracy at fADC = 18 MHz*, *Table 76: ADC static accuracy at fADC = 30 MHz* and *Table 77: ADC static accuracy at fADC = 36 MHz*. Updated $t_{d(SDCLKL\_Data)}$ and $t_{h(SDCLKL\_Data)}$ in *Table 104: SDRAM write timings*. Updated note below marking schematics. Added *Figure 96: UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint* and *Table 117: UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 99: UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint* and *Table 119: UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)*.
30-Nov-2015	8	Updated $\|V_{SSX} - V_{SS}\|$ in *Table 14: Voltage characteristics* to add V_{REF-}. Updated $t_{d(TXEN)}$ and $t_{d(TXD)}$ minimum value in *Table 72: Dynamics characteristics: Ethernet MAC signals for RMII* and *Table 73: Dynamics characteristics: Ethernet MAC signals for MII*. Added V_{REF-} in *Table 74: ADC characteristics*. Added A1 minimum and maximum values in *Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data*. Updated *Figure 86: LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline*.Updated *Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline* and *Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data*. Updated *Figure 101: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline* and *Table 120: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data*.