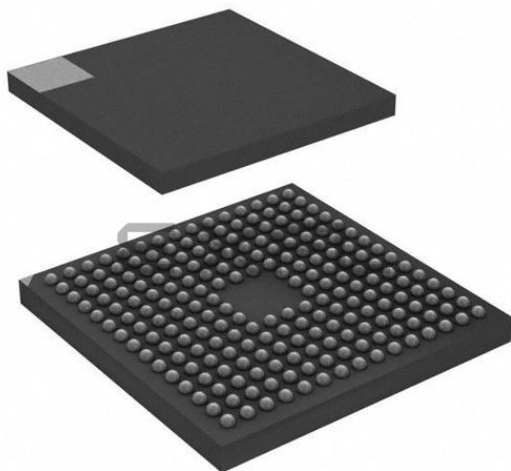




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f439nih6

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3 Functional overview

3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F43x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F43x family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F43x devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F43x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

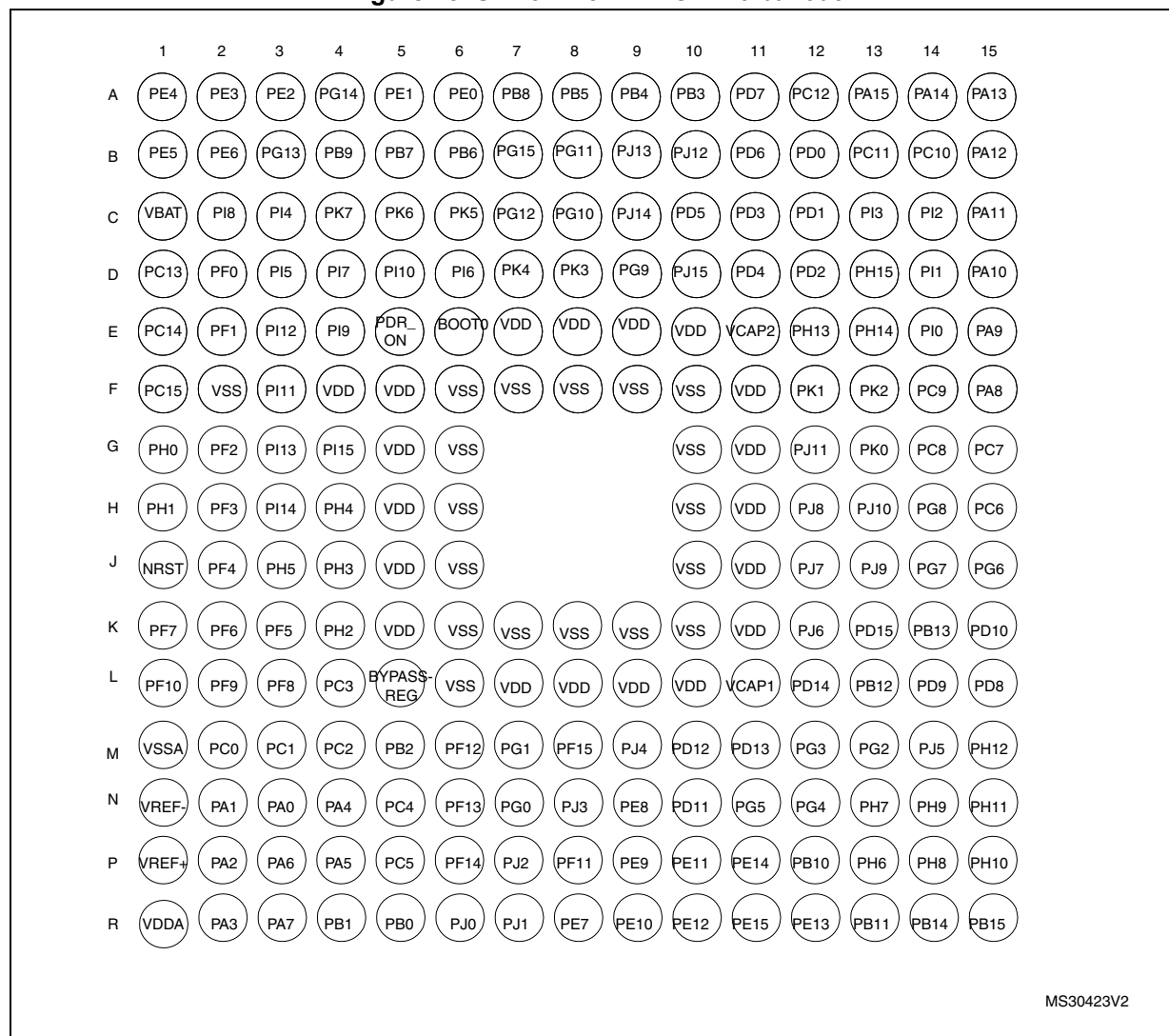
These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.22.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Figure 18. STM32F43x TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
35	46	N4	R5	56	N8	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_ IN8
36	47	K5	R4	57	K7	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_ IN9
37	48	L5	M6	58	L7	63	M5	PB2-BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	M5	R6	59	M7	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	N5	P6	60	N7	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	51	G9	M8	61	-	72	K7	V _{SS}	S		-	-	-
-	52	D10	N8	62	-	73	L8	V _{DD}	S		-	-	-
-	53	M6	N6	63	K6	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	54	K7	R7	64	L6	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	55	L7	P7	65	M6	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	56	N6	N7	66	N6	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	M7	67	K5	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-



Table 12. STM32F437xx and STM32F439xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port G	PG9	-	-	-	-	-	-	-	-	USART6_ RX	-	-	-	FMC_NE2/ FMC_ NCE3	DCMI_ VSYNC (1)	-	EVEN TOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_ NCE4_1/ FMC_NE3	DCMI_ D2	LCD_B2	EVEN TOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ TX_EN/ ETH_RMII_ TX_EN	FMC_ NCE4_2	DCMI_ D3	LCD_B3	EVEN TOUT
	PG12	-	-	-	-	-	SPI6_ MISO	-	-	USART6_ RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVEN TOUT
	PG13	-	-	-	-	-	SPI6_ SCK	-	-	USART6_ CTS	-	-	ETH_MII_ TXD0/ ETH_RMII_ TXD0	FMC_A24	-	-	EVEN TOUT
	PG14	-	-	-	-	-	SPI6_ MOSI	-	-	USART6_ TX	-	-	ETH_MII_ TXD1/ ETH_RMII_ TXD1	FMC_A25	-	-	EVEN TOUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	FMC_ SDNCAS	DCMI_ D13	-	EVEN TOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ CRS	FMC_ SDCKE0	-	LCD_R0	EVEN TOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ COL	FMC_SDN E0	-	LCD_R1	EVEN TOUT
	PH4	-	-	-	-	I2C2_ SCL	-	-	-	-	-	OTG_HS_ ULPI_NXT	-	-	-	-	EVEN TOUT
	PH5	-	-	-	-	I2C2_ SDA	SPI5_N SS	-	-	-	-	-	-	FMC_SDN WE	-	-	EVEN TOUT
	PH6	-	-	-	-	I2C2_ SMBA	SPI5_ SCK	-	-	-	TIM12_CH1	-	-	FMC_ SDNE1	DCMI_ D8	-	-

6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	$\mu s/V$
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 21. Operating conditions at power-up / power-down (regulator OFF)⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	$\mu s/V$
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Table 33. Typical current consumption in Sleep mode, regulator OFF⁽¹⁾

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	
I _{DD12} /I _{DD}	Supply current in Sleep mode from V ₁₂ and V _{DD} supply	All Peripherals enabled	180	61.5	1.4	-	-	mA
			168	59.4	1.3	59.4	1.0	
			150	53.9	1.3	53.9	1.0	
			144	49.0	1.3	49.0	1.0	
			120	38.0	1.2	38.0	0.9	
			90	29.3	1.4	29.3	1.1	
			60	20.2	1.2	20.2	0.9	
			30	11.9	1.2	11.9	0.9	
			25	10.4	1.2	10.4	0.9	
		All Peripherals disabled	180	14.9	1.4	-	-	
			168	14.0	1.3	14.0	1.0	
			150	12.6	1.3	12.6	1.0	
			144	11.5	1.3	11.5	1.0	
			120	8.7	1.2	8.7	0.9	
			90	7.1	1.4	7.1	1.1	
			60	5.0	1.2	5.0	0.9	
			30	3.1	1.2	3.1	0.9	
			25	2.8	1.2	2.8	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 52: EMI characteristics](#)). It is available only on the main PLL.

Table 46. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL_IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

If $f_{\text{PLL_IN}} = 1 \text{ MHz}$, and $f_{\text{MOD}} = 1 \text{ kHz}$, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLL_N} / (100 \times 5 \times \text{MODEPER})]$$

$f_{\text{VCO_OUT}}$ must be expressed in MHz.

With a modulation depth (md) = $\pm 2\%$ (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240 / (100 \times 5 \times 250)] = 126 \text{md(quantized)\%}$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLL_N})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	k Ω
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
$C_{IO}^{(8)}$	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to [Table 55: I/O current injection susceptibility](#)
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 55: I/O current injection susceptibility](#)
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 35](#).

SAI characteristics

Unless otherwise specified, the parameters given in [Table 64](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V_{DD}

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 64. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f _{MCKL}	SAI Main clock output	-	256 x 8K	256xFs ⁽²⁾	MHz
F _{SCK}	SAI clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D _{SCK}	SAI clock frequency duty cycle	Slave receiver	30	70	%
t _{v(FS)}	FS valid time	Master mode	8	22	ns
t _{su(FS)}	FS setup time	Slave mode	2	-	
t _{h(FS)}	FS hold time	Master mode	8	-	
		Slave mode	0	-	
t _{su(SD_MR)}	Data input setup time	Master receiver	5	-	
t _{su(SD_SR)}		Slave receiver	3	-	
t _{h(SD_MR)}	Data input hold time	Master receiver	0	-	
t _{h(SD_SR)}		Slave receiver	0	-	
t _{v(SD_ST)}	Data output valid time	Slave transmitter (after enable edge)	-	22	
t _{h(SD_ST)}		Master transmitter (after enable edge)	-	20	
t _{v(SD_MT)}	Data output hold time	Master transmitter (after enable edge)	8	-	
t _{h(SD_MT)}		Master transmitter (after enable edge)	8	-	

1. Guaranteed by characterization results.

2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

Table 70. Dynamic characteristics: USB ULPI⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time		2	-	-	ns
t _{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time		0.5	-	-	
t _{SD}	Data in setup time		1.5	-	-	
t _{HD}	Data in hold time		2	-	-	
t _{DC} /t _{DD}	Data/control output delay	2.7 V < V _{DD} < 3.6 V, C _L = 15 pF and OSPEEDRy[1:0] = 11	-	9	9.5	
		2.7 V < V _{DD} < 3.6 V, C _L = 20 pF and OSPEEDRy[1:0] = 10	-	12	15	
		1.7 V < V _{DD} < 3.6 V, C _L = 15 pF and OSPEEDRy[1:0] = 11	-			

1. Guaranteed by characterization results.

Ethernet characteristics

Unless otherwise specified, the parameters given in [Table 71](#), [Table 72](#) and [Table 73](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 17](#) with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF for $2.7\text{ V} < V_{DD} < 3.6\text{ V}$
- Capacitive load $C = 20$ pF for $1.71\text{ V} < V_{DD} < 3.6\text{ V}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

[Table 71](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 47](#) shows the corresponding timing diagram.

Figure 47. Ethernet SMI timing diagram

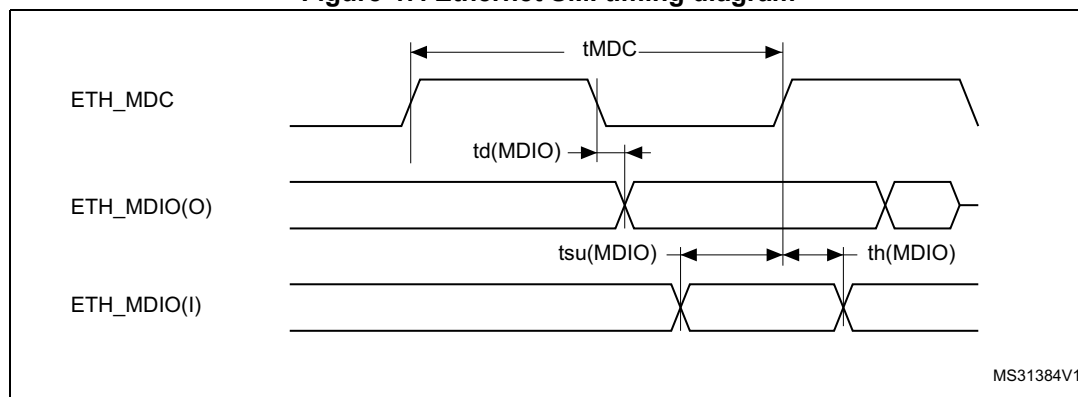


Table 71. Dynamics characteristics: Ethernet MAC signals for SMI⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_d(MDIO)$	Write data valid time	6	10	13	
$t_{su}(MDIO)$	Read data setup time	12	-	-	
$t_h(MDIO)$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Table 90. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 0.5$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	ns
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	ns
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	2	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	ns
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	ns
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	ns
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	ns
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 1.5$	-	ns
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK} + 1$	-	ns
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	ns
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	ns

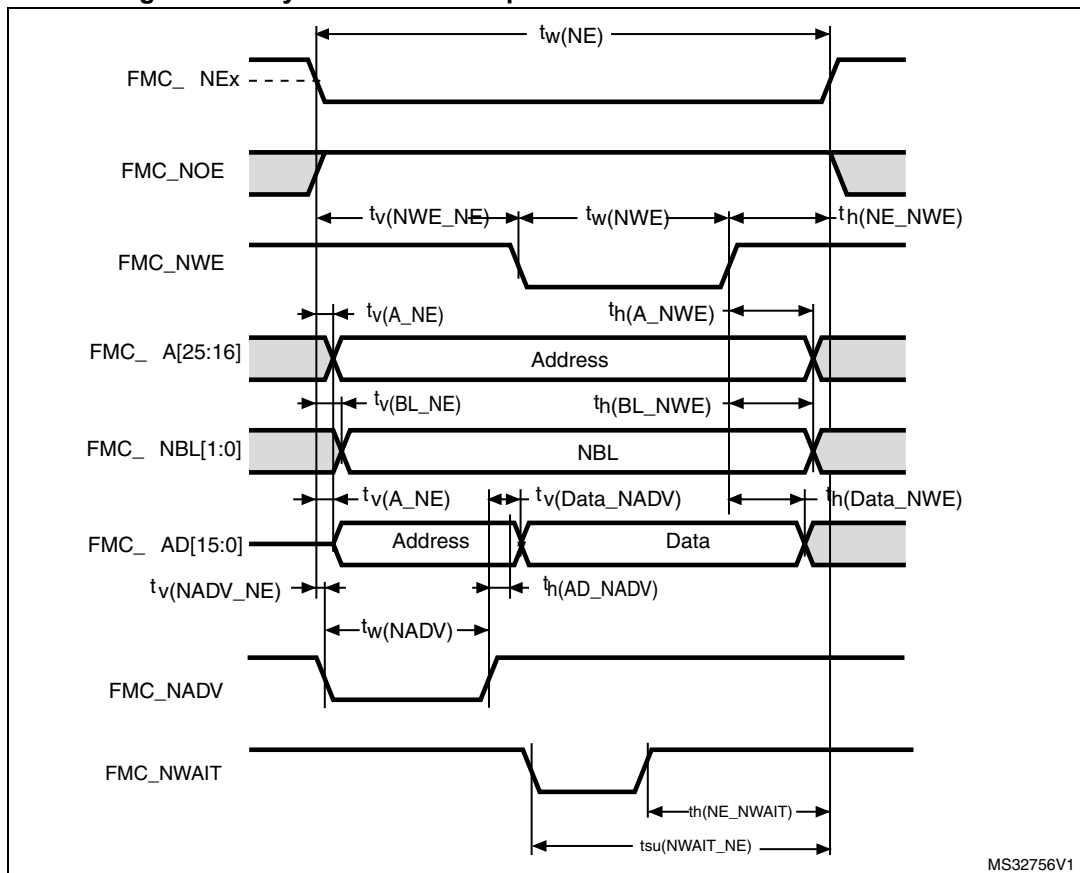
1. $C_L = 30$ pF.
2. Guaranteed by characterization results.

Table 91. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} + 0.5$	$8T_{HCLK} + 2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 1.5$	ns
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	ns
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$	-	ns

1. $C_L = 30$ pF.
2. Guaranteed by characterization results.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms



MS32756V1

Table 92. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_v(NWE_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_w(NWE)$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_h(NE_NWE)$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_v(A_NE)$	FMC_NEx low to FMC_A valid	-	0	ns
$t_v(NADV_NE)$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_w(NADV)$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	ns
$t_h(AD_NADV)$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	ns
$t_h(A_NWE)$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_h(BL_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_v(BL_NE)$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_v(Data_NADV)$	FMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	ns
$t_h(Data_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

6.3.27 Camera interface (DCMI) timing specifications

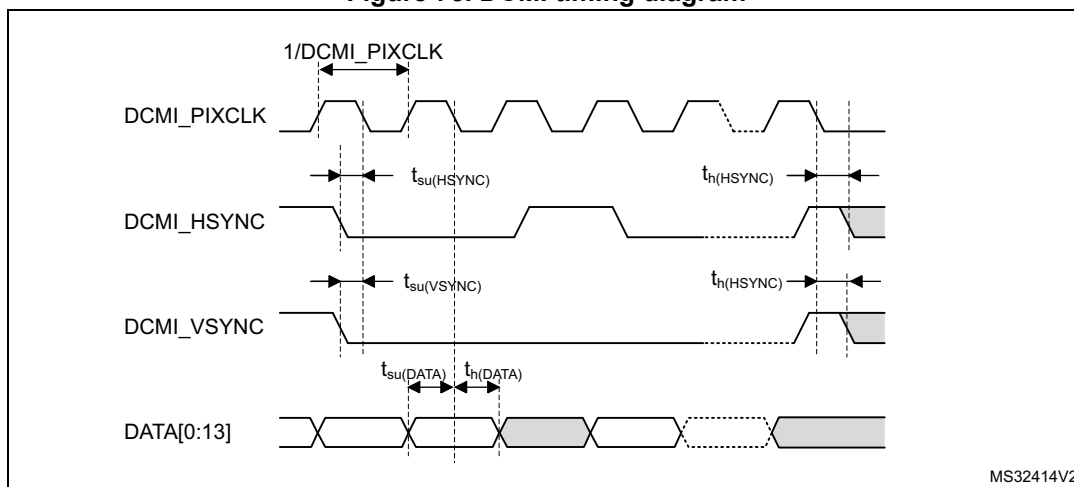
Unless otherwise specified, the parameters given in [Table 106](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 17](#), with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 106. DCMI characteristics

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su}(DATA)$	Data input setup time	2	-	ns
$t_h(DATA)$	Data input hold time	2.5	-	
$t_{su}(HSYNC)$ $t_{su}(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input setup time	0.5	-	
$t_h(HSYNC)$ $t_h(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	

Figure 75. DCMI timing diagram

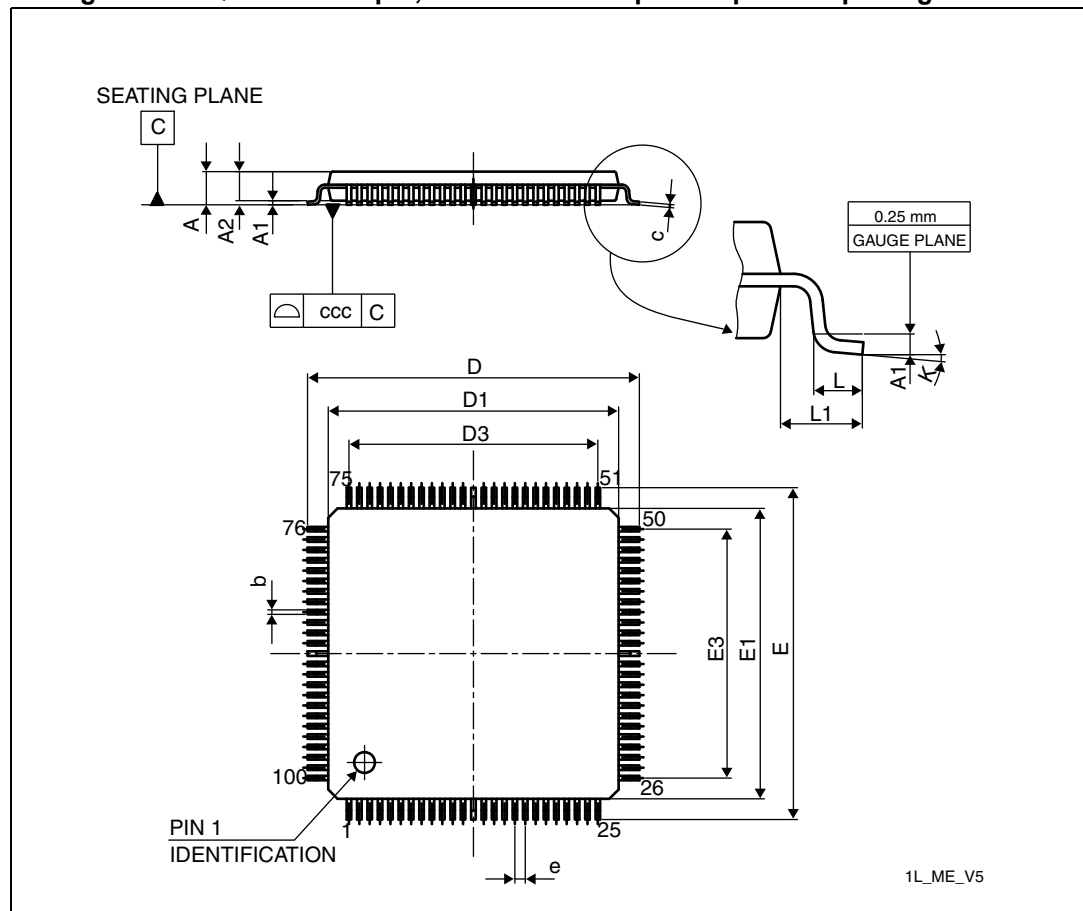


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 80. LQFP100 -100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 110. LQPF100 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 99. UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

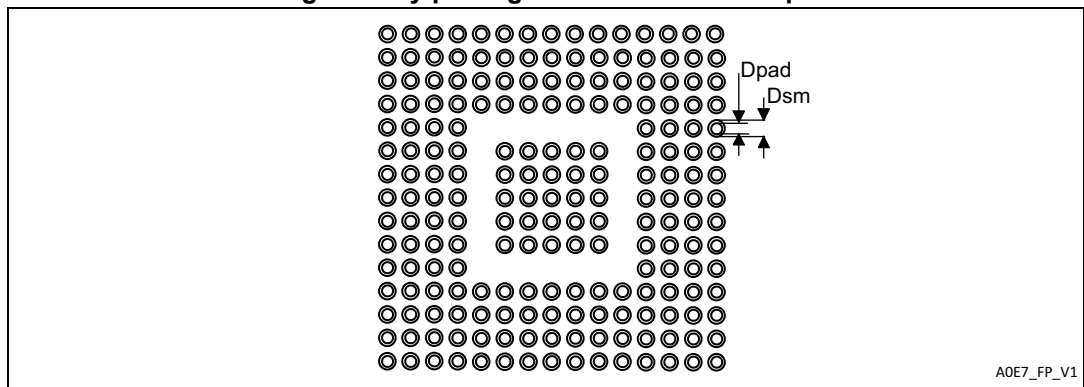
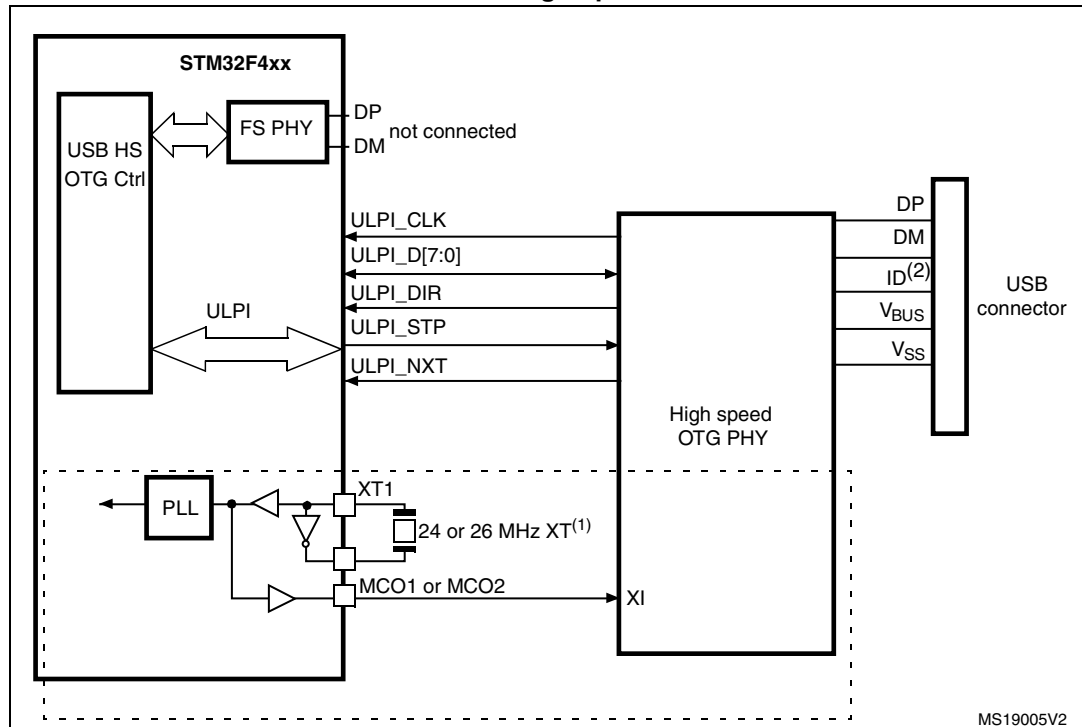


Table 119. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

B.2 USB OTG high speed (HS) interface solutions

Figure 106. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F43x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.