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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f439zgt6

3.26 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

Note: For I2S2 full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.

3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).

3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.42 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

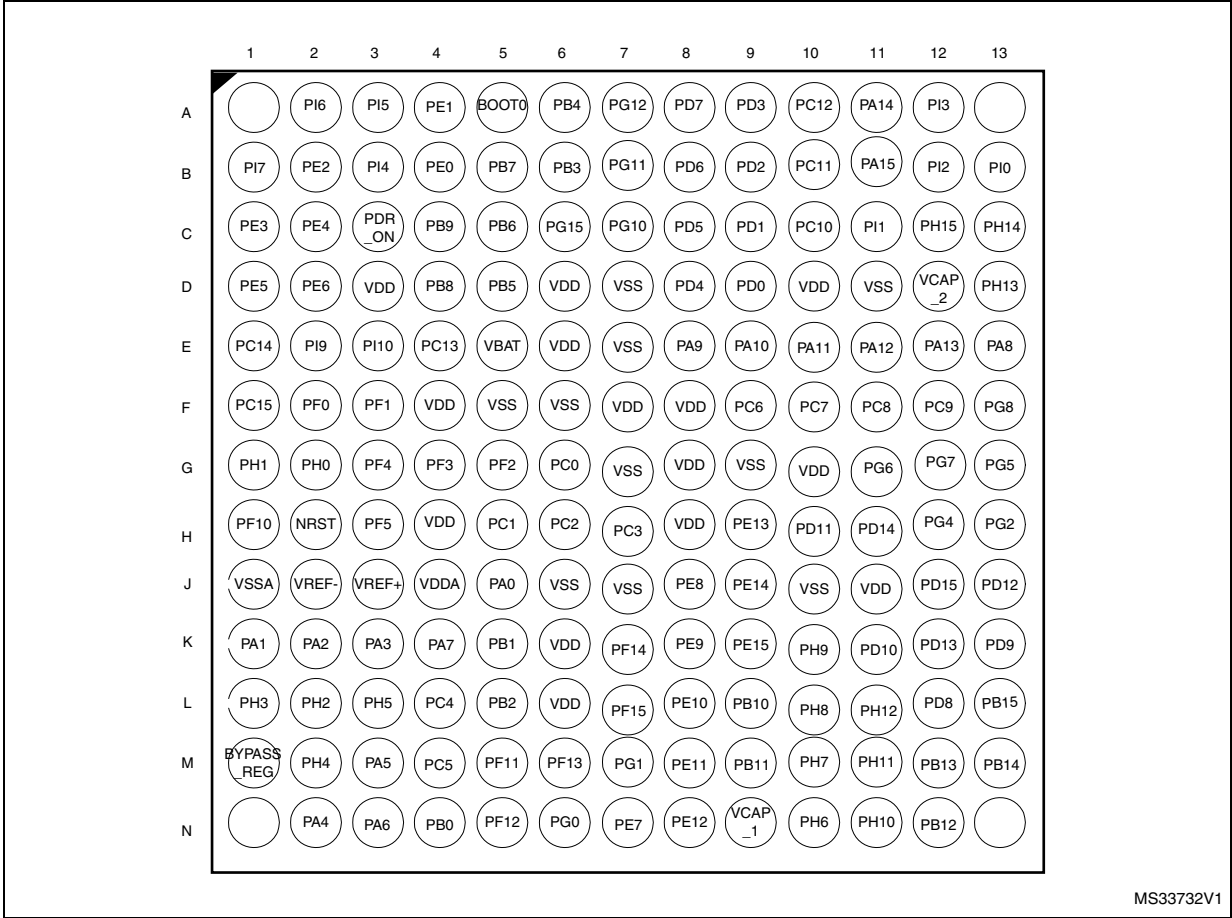
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.43 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F43x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Figure 16. STM32F43x UFBGA169 ballout



1. The above figure shows the package top view.
2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.

Table 10. STM32F437xx and STM32F439xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	-	M1	L4	48	N11	-	L5	BYPASS_ REG	I	FT	-	-	-
28	39	J11	K4	49	J8	52	K5	V _{DD}	S	-	-	-	-
29	40	N2	N4	50	M10	53	N4	PA4	I/O	TTa	(5)	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_ IN4 /DAC_ OUT1
30	41	M3	P4	51	M9	54	P4	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_ IN5/DAC_ OUT2
31	42	N3	P3	52	N10	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_ IN6
32	43	K4	R3	53	L8	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_ RMII_CRS_DV, EVENTOUT	ADC12_ IN7
33	44	L4	N5	54	M8	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_ RMII_RXD0, EVENTOUT	ADC12_ IN14
34	45	M4	P5	55	N9	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_ RMII_RXD1, EVENTOUT	ADC12_ IN15
-	-	-	-	-	J7	59	L7	V _{DD}	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-

4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
6. If the device is delivered in an WLCSP143, UFBGA169, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS_REG pin is set to V_{DD} (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).
7. PI0 and PI1 cannot be used for I2S2 full-duplex mode.
8. The DCMI_VSYNC alternate function on PG9 is only available on silicon revision 3.

5 Memory mapping

The memory map is shown in [Figure 19](#).

Figure 19. Memory map

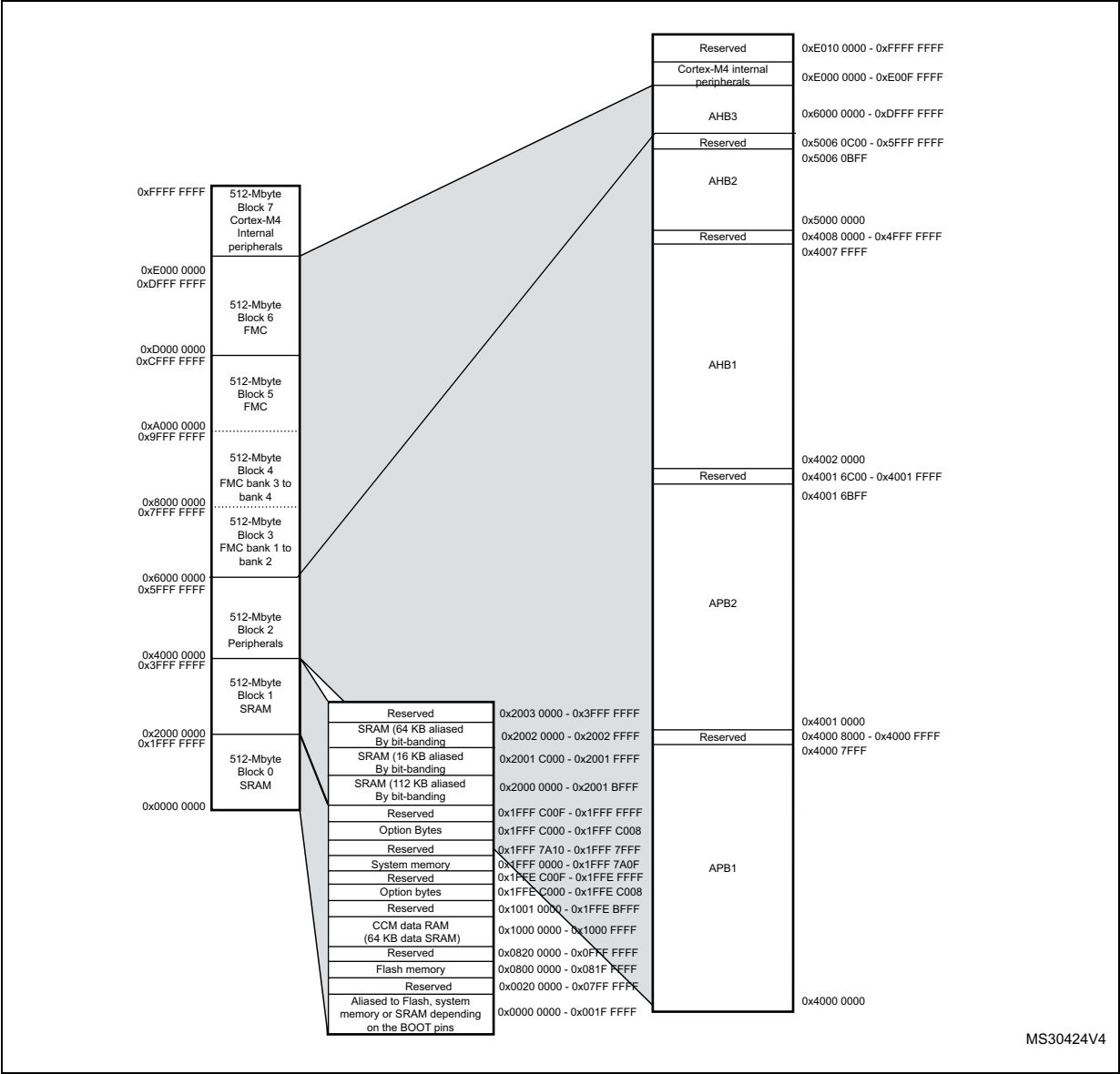


Table 13. STM32F437xx and STM32F439xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000 - 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00 - 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	DMA2D
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	Reserved
	0x4002 6800 - 0x4002 7FFF	
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Sleep mode	All Peripherals enabled ⁽²⁾	180	78	89 ⁽³⁾	110	130 ⁽³⁾	mA
			168	66	75 ⁽³⁾	93	110 ⁽³⁾	
			150	56	61	80	96	
			144	54	58	78	94	
			120	40	44	59	72	
			90	32	34	46	56	
			60	22	23	31	38	
			30	10	16	30	43	
			25	9	14	28	40	
			16	5	12	25	40	
			8	3	8	22	35	
			4	3	7	21	34	
			2	2	6.5	20	33	
		All Peripherals disabled	180	21	26 ⁽³⁾	54	76 ⁽³⁾	
			168	16	20 ⁽³⁾	41	58 ⁽³⁾	
			150	14	17	36	52	
			144	13	16.5	35	51	
			120	10	14	28	41	
			90	8	13	26	37	
			60	6	9	17	25	
			30	5	8	22	35	
			25	3	7	21	34	
			16	3	7	21	34	
			8	2	6	20	33	
			4	2	6	20	33	
			2	2	6	20	33	

1. Guaranteed by characterization unless otherwise specified.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

3. Based on characterization, tested in production.

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 52: EMI characteristics](#)). It is available only on the main PLL.

Table 46. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL_IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

If $f_{\text{PLL_IN}} = 1 \text{ MHz}$, and $f_{\text{MOD}} = 1 \text{ kHz}$, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLLN}] / (100 \times 5 \times \text{MODEPER})$$

$f_{\text{VCO_OUT}}$ must be expressed in MHz.

With a modulation depth (md) = $\pm 2\%$ (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126 \text{md(quantized)\%}$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 56: I/O static characteristics](#)).

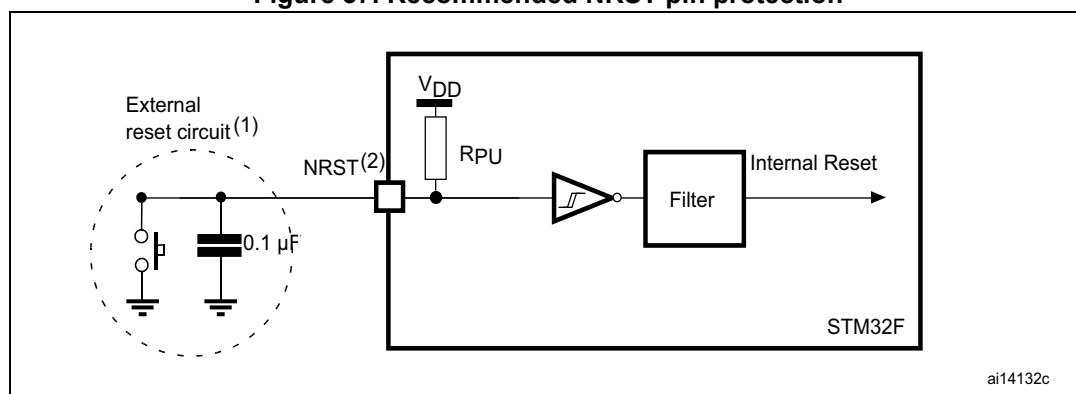
Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μ s

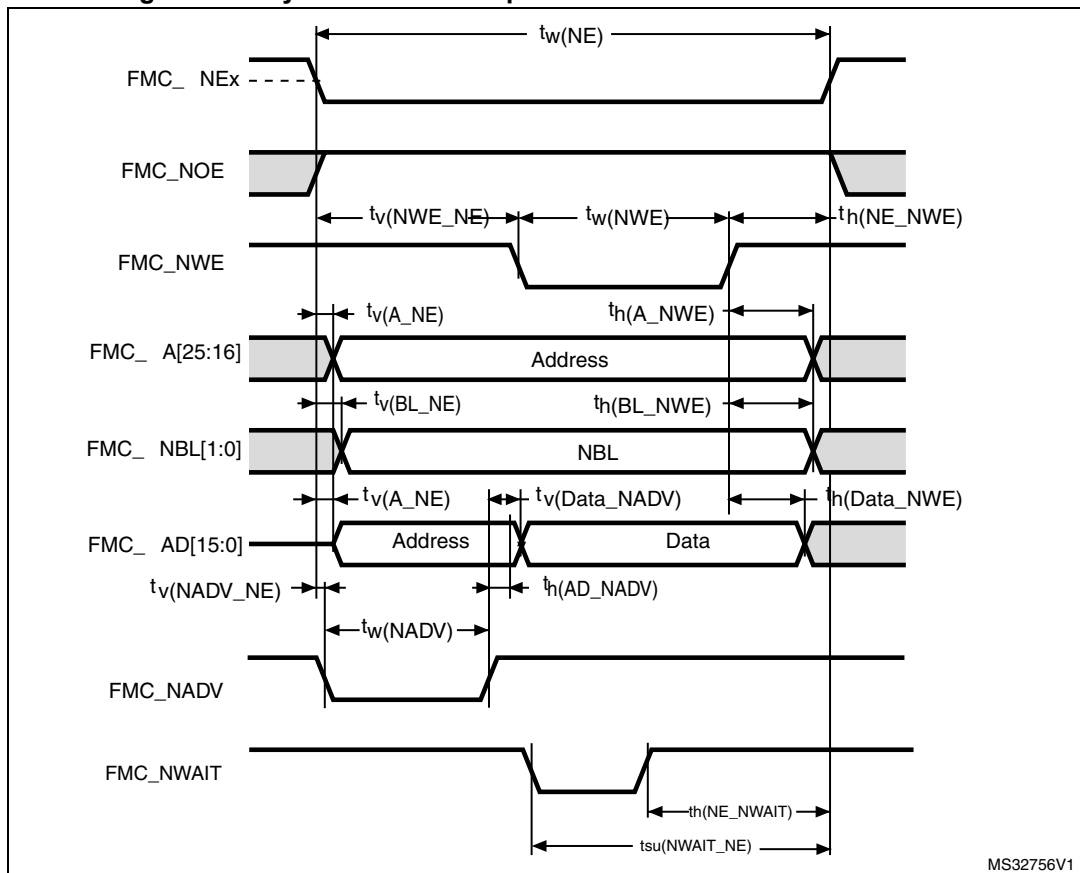
1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 59](#). Otherwise the reset is not taken into account by the device.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms



MS32756V1

Table 92. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_v(NWE_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_w(NWE)$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_h(NE_NWE)$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_v(A_NE)$	FMC_NEx low to FMC_A valid	-	0	ns
$t_v(NADV_NE)$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_w(NADV)$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	ns
$t_h(AD_NADV)$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	ns
$t_h(A_NWE)$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_h(BL_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_v(BL_NE)$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_v(Data_NADV)$	FMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	ns
$t_h(Data_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	ns
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Synchronous waveforms and timings

[Figure 59](#) through [Figure 62](#) represent synchronous waveforms and [Table 94](#) through [Table 97](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

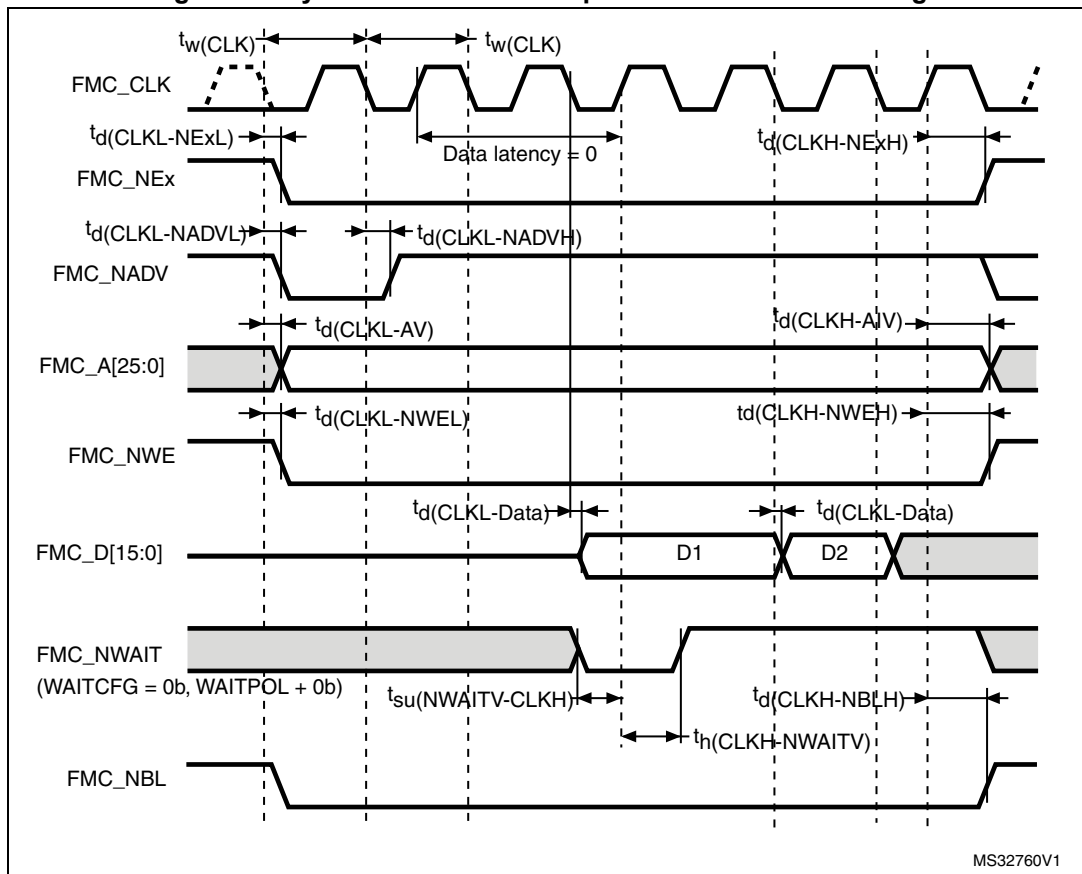
In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

Table 96. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	0	-	ns
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4		
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0		

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Figure 62. Synchronous non-multiplexed PSRAM write timings**Table 97. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾**

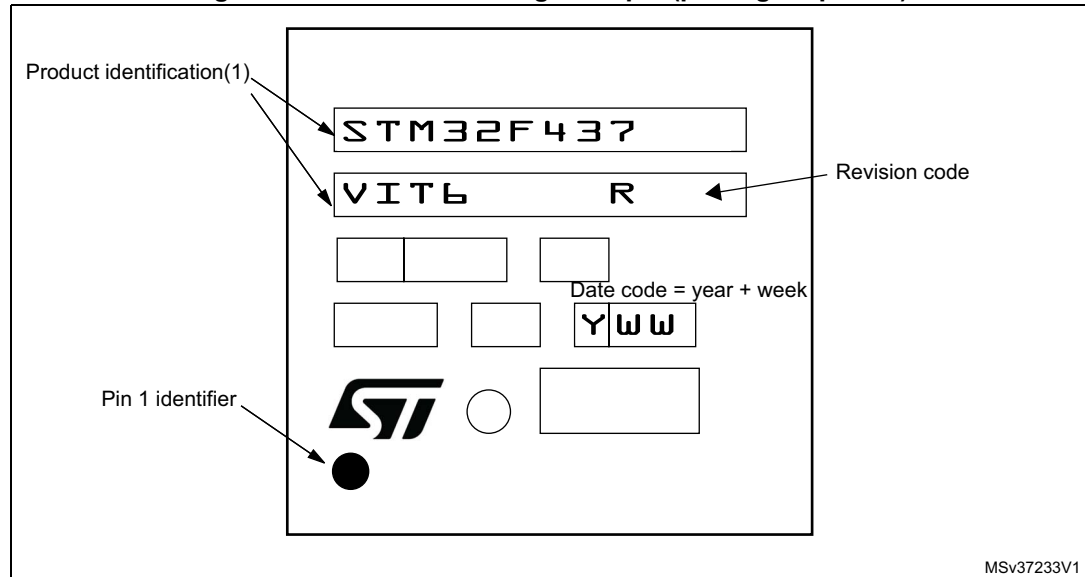
Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	0.5	ns
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x=0..2)	T_{HCLK}	-	ns
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	0	ns

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

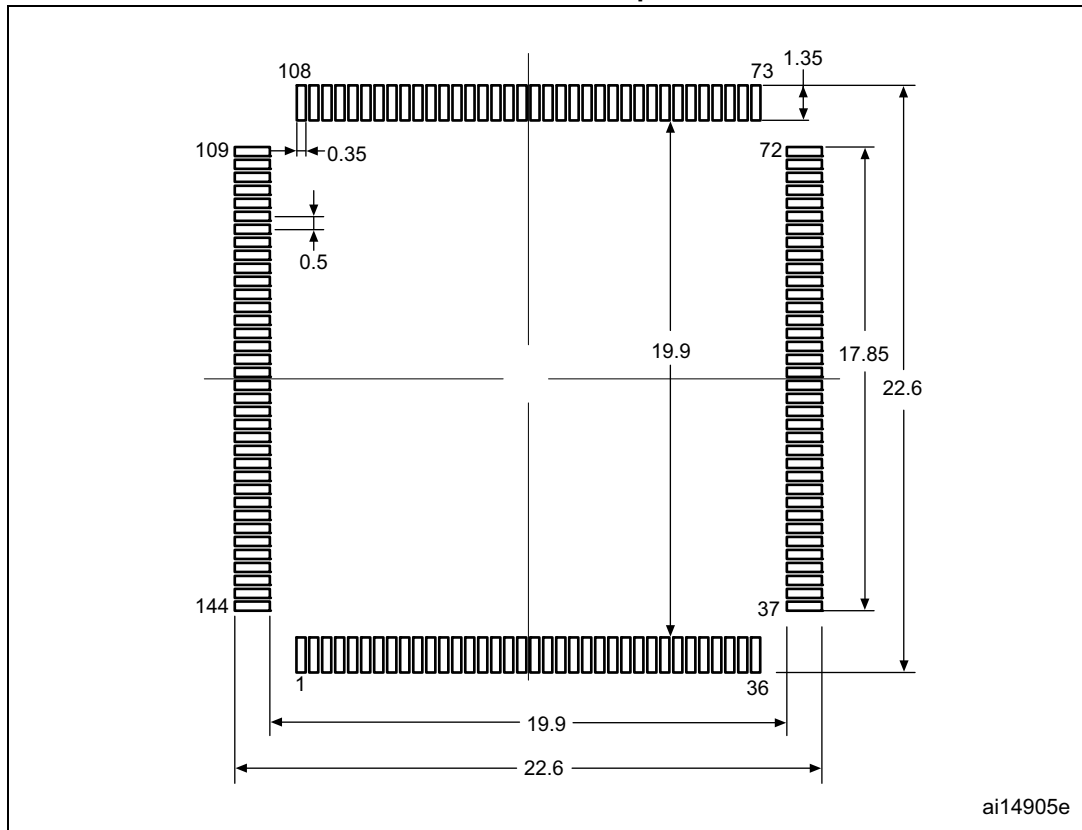
Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 82. LQFP100 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Figure 87. LQPF144- 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint



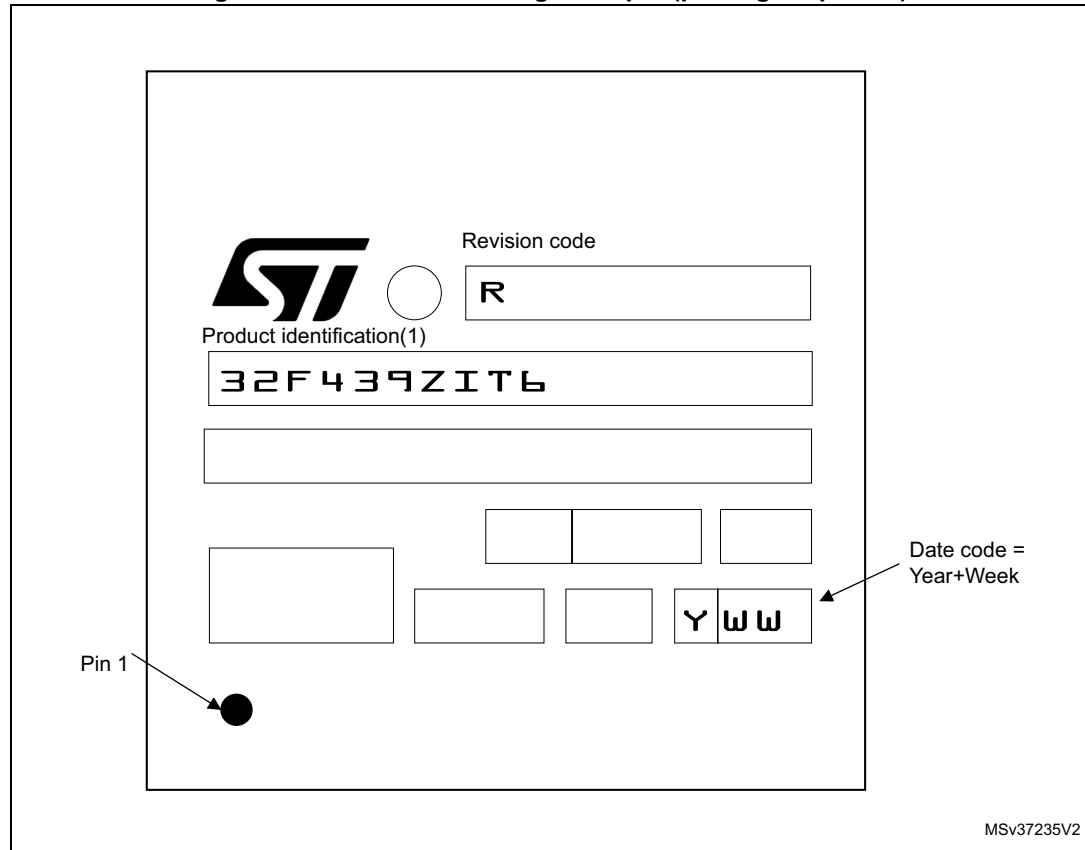
1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 88. LQFP144 marking example (package top view)



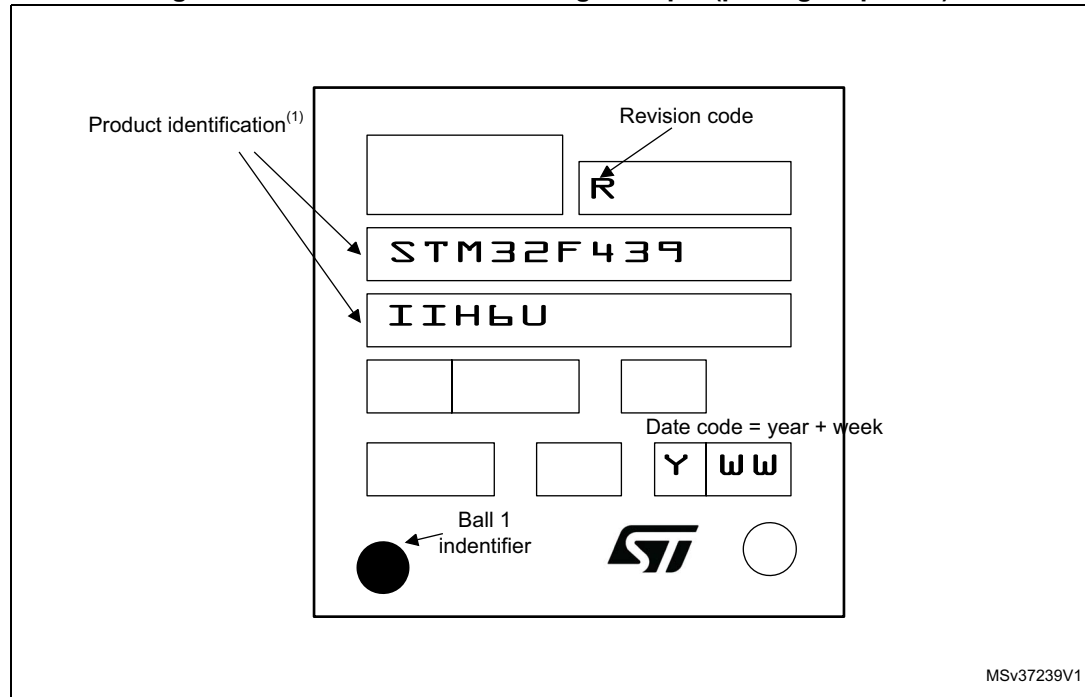
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking for UFBGA176+25

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 100. UFBGA176+25 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD} .
- The over-drive mode is not supported.

A.1 Operating conditions

Table 123. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to $2.1 V^{(3)}$	Conversion time up to 1.2 Msps	20 MHz ⁽⁴⁾	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 3.17.1: Internal reset ON](#)).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

Table 124. Document revision history (continued)

Date	Revision	Changes
19-Feb-2015	6	<p>Update SPI/IS2 in Table 2: STM32F437xx and STM32F439xx features and peripheral counts.</p> <p>Updated LQFP208 in Table 4: Regulator ON/OFF and internal reset ON/OFF availability.</p> <p>Updated Figure 19: Memory map.</p> <p>Changed PLS[2:0]=101 (falling edge) maximum value in Table 22: reset and power control block characteristics.</p> <p>Updated current consumption with all peripherals disabled in Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM.</p> <p>Updated note 1. in Table 28: Typical and maximum current consumptions in Standby mode.</p> <p>Updated t_{WUSTOP} in Table 36: Low-power mode wakeup timings.</p> <p>Updated ESD standards and Table 53: ESD absolute maximum ratings.</p> <p>Updated Table 56: I/O static characteristics.</p> <p>Section : I2C interface characteristics: updated section introduction, removed Table I2C characteristics, Figure I2C bus AC waveforms and measurement circuit and Table SCL frequency; added Table 61: I2C analog filter characteristics.</p> <p>Updated measurement conditions in Table 62: SPI dynamic characteristics.</p> <p>Updated Figure 51: Typical connection diagram using the ADC.</p> <p>Updated Section : Device marking for LQFP100.</p> <p>Updated Figure 83: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline and Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data; added Figure 84: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint and Table 112: WLCSP143 recommended PCB design rules (0.4 mm pitch). Updated Figure 85: WLCSP143 marking example (package top view) and related note. Updated Section : Device marking for WLCSP143.</p> <p>Updated Section : Device marking for LQFP144.</p> <p>Updated Section : Device marking for LQFP176.</p> <p>Updated Figure 92: LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline; Updated Section : Device marking for LQFP208.</p> <p>Modified UFBGA169 pitch, updated Figure 95: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline and Table 116: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data; updated Section : Device marking for LQFP208.</p> <p>updated Section : Device marking for UFBGA169, Section : Device marking for UFBGA176+25 and Section : Device marking for TFBGA176.</p> <p>Updated Z pin count in Table 122: Ordering information scheme.</p>

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