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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atuc64d3-a2ut

5.4 Programming Model

5.4.1 Register File Configuration

The AVR32UC register file is shown below.

Figure 5-3. The AVR32UC Register File

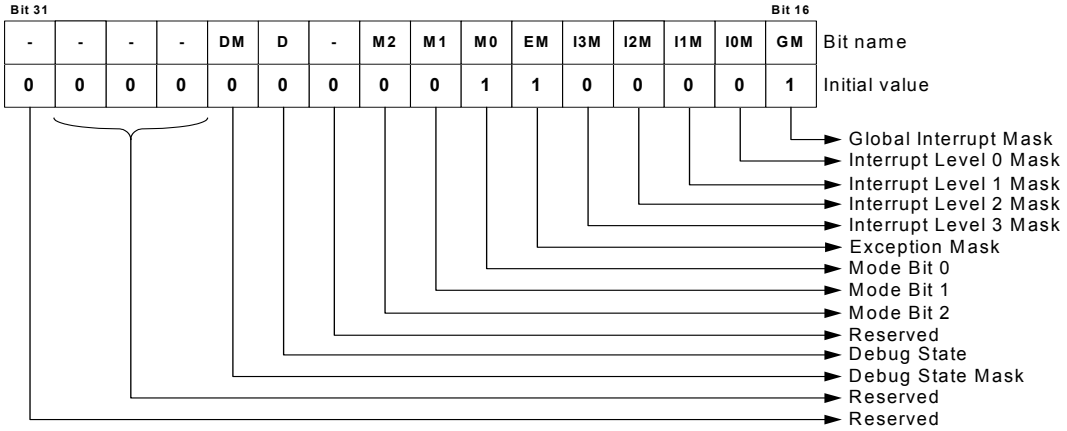
Application	Supervisor	INT0	INT1	INT2	INT3	Exception	NMI	Secure
Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0	Bit 31 Bit 0
PC	PC	PC	PC	PC	PC	PC	PC	PC
LR	LR	LR	LR	LR	LR	LR	LR	LR
SP_APP	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SEC
R12	R12	R12	R12	R12	R12	R12	R12	R12
R11	R11	R11	R11	R11	R11	R11	R11	R11
R10	R10	R10	R10	R10	R10	R10	R10	R10
R9	R9	R9	R9	R9	R9	R9	R9	R9
R8	R8	R8	R8	R8	R8	R8	R8	R8
R7	R7	R7	R7	R7	R7	R7	R7	R7
R6	R6	R6	R6	R6	R6	R6	R6	R6
R5	R5	R5	R5	R5	R5	R5	R5	R5
R4	R4	R4	R4	R4	R4	R4	R4	R4
R3	R3	R3	R3	R3	R3	R3	R3	R3
R2	R2	R2	R2	R2	R2	R2	R2	R2
R1	R1	R1	R1	R1	R1	R1	R1	R1
R0	R0	R0	R0	R0	R0	R0	R0	R0
SR	SR	SR	SR	SR	SR	SR	SR	SR

SS_STATUS
SS_ADRF
SS_ADRR
SS_ADR0
SS_ADR1
SS_SP_SYS
SS_SP_APP
SS_RAR
SS_RSR

5.4.2 Status Register Configuration

The Status Register (SR) is split into two halfwords, one upper and one lower, see Figure 5-4 and Figure 5-5. The lower word contains the C, Z, N, V, and Q condition code flags and the R, T, and L bits, while the upper halfword contains information about the mode and state the processor executes in. Refer to the *AVR32 Architecture Manual* for details.

Figure 5-4. The Status Register High Halfword



12.7.15 Peripheral Power Control Register

Name: PPCR

Access Type: Read/Write

Offset: 0x160

Reset Value: 0x00000018

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	ASTRCMASK	TWISRCMASK	RSTTM	-	RSTPUN

- **ASTRCMASK : AST Request Clock Mask**
  0: AST Request Clock is disabled
  1: AST Request Clock is enabled
- **TWISRCMASK : TWIS0 Request Clock Mask**
  0: TWIS Request Clock is disabled
  1: TWIS Request Clock is enabled
- **RSTPUN: Reset Pullup, active low**
  0: Pull-up for external reset on
  1: Pull-up for external reset off
- **RSTTM : Reset test mode**
  0: External reset not in test mode
  1: External reset in test mode

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refere to the UNLOCK register description for details.

13.6.20 Oscillator 0 Interface Version Register

Name: OSCVERSION

Access Type: Read-only

Offset: 0x03D8

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	VARIANT			

15	14	13	12	11	10	9	8
-	-	-	-	VERSION[11:8]			

7	6	5	4	3	2	1	0
VERSION[7:0]							

- **VARIANT: Variant number**
  Reserved. No functionality associated.
- **VERSION: Version number**
  Version number of the module. No functionality associated.

19.7.1.8 IP Name Register 1

Register Name: UNAME1

Access Type: Read-Only

Offset: 0x0824

Reset Value: -

31	30	29	28	27	26	25	24
UNAME1[31:24]							

23	22	21	20	19	18	17	16
UNAME1[23:16]							

15	14	13	12	11	10	9	8
UNAME1[15:8]							

7	6	5	4	3	2	1	0
UNAME1[7:0]							

- **UNAME1: IP Name Part One**
  This field indicates the first part of the ASCII-encoded name of the USBC IP.

19.7.2.6 Device Global Interrupt Enable Clear Register

Register Name: UDINTECLR

Access Type: Write-Only

Offset: 0x0014

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	EP8INTEC(1)	EP7INTEC(1)	EP6INTEC(1)	EP5INTEC(1)	EP4INTEC(1)

15	14	13	12	11	10	9	8
EP3INTEC(1)	EP2INTEC(1)	EP1INTEC(1)	EP0INTEC	-	-	-	-

7	6	5	4	3	2	1	0
-	UPRSMEC	EORSMEC	WAKEUPEC	EORSTEC	SOFEC	-	SUSPEC

Note: 1. EPnINTEC bits are within the range from EP0INTEC to EP6INTEC.

Writing a zero to a bit in this register has no effect.

Writing a one to a bit in this register will clear the corresponding bit in UDINTE.

These bits always read as zero.

19.8 Module Configuration

Table 19-6. USBC Clocks

Clock Name	Description
CLK_USBC	Clock for the USBC bus interface
GCLK_USBC	48Mhz USB clock. This clock frequency must be configured to 48MHz. The generic clock used for the USBC is GCLK3

Table 19-7. Register Reset Values

Register	Reset Value
UVERS	0x00000200
UFEATURES	0x00000007
UADDRSIZE	0x00001000
UNAME1	0x48555342
UNAME2	0x00000000

20.3 Block Diagram

Figure 20-1. USART Block Diagram

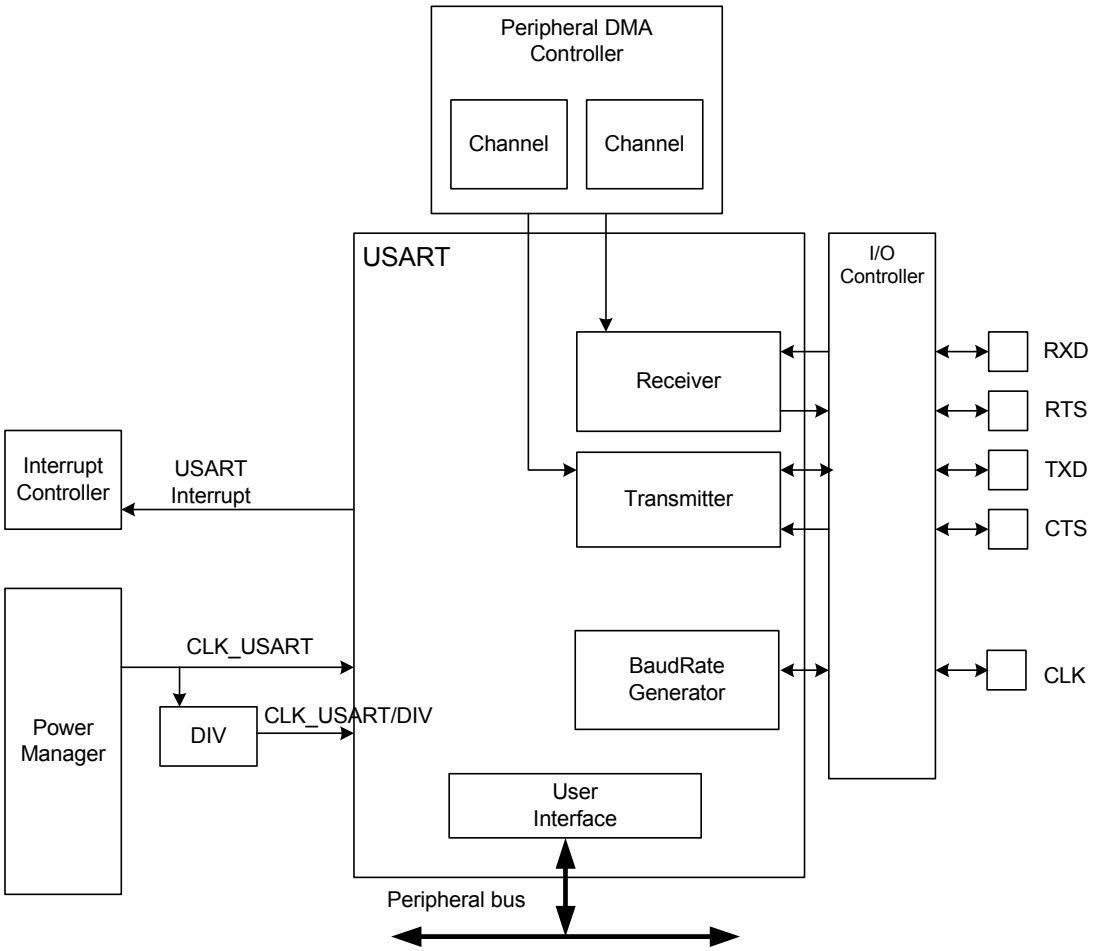
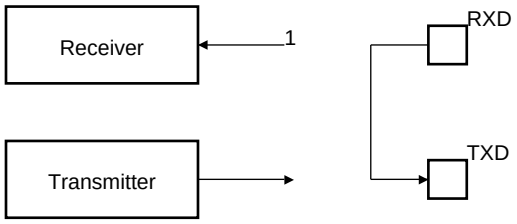


Table 20-1. SPI Operating Mode

PIN	USART	SPI Slave	SPI Master
RXD	RXD	MOSI	MISO
TXD	TXD	MISO	MOSI
RTS	RTS	–	CS
CTS	CTS	CS	–

Figure 20-23. Remote Loopback Mode Configuration



20.6.7 Write Protection Registers

To prevent single software errors from corrupting USART behavior, certain address spaces can be write-protected by writing the correct Write Protect KEY and a one to the Write Protect Enable bit in the Write Protect Mode Register (WPMR.WPKEY, and WPMR.WPEN). Disabling the write protection is done by writing the correct key, and a zero to WPEN.

Write attempts to a write protected register are detected and the Write Protect Violation Status bit in the Write Protect Status Register (WPSR.WPVS) is set, while the Write Protect Violation Source field (WPSR.WPVSRC) indicates the targeted register. Writing the correct key to the Write Protect KEY bit (WPMR.WPKEY) clears WPVSRC and WPVS.

The protected registers are:

- ”Mode Register” on page 358
- ”Baud Rate Generator Register” on page 368
- ”Receiver Time-out Register” on page 369
- ”Transmitter Timeguard Register” on page 370

20.7.5 Interrupt Mask Register

Name: IMR

Access Type: Read-only

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	CTSIC	–	–	–
15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	–	ITER/UNRE	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	–	–	RXBRK	TXRDY	RXRDY

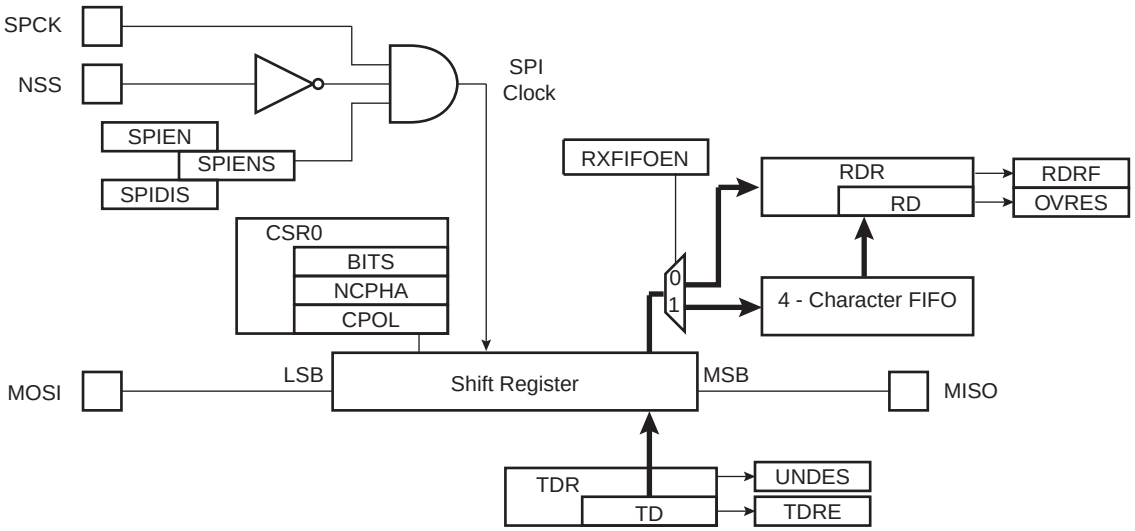
0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

A bit in this register is cleared when the corresponding bit in IDR is written to one.

A bit in this register is set when the corresponding bit in IER is written to one.

Figure 21-9. Slave Mode Functional Block Diagram



21.8.6 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	UNDES	TXEMPTY	NSSR

7	6	5	4	3	2	1	0
-	-	-	-	OVRES	MODF	TDRE	RDRF

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will set the corresponding bit in IMR.

21.8.13 Write Protection Control Register

Register Name: WPCR

Access Type: Read-write

Offset: 0xE4

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
SPIWPKEY[23:16]							

23	22	21	20	19	18	17	16
SPIWPKEY[15:8]							

15	14	13	12	11	10	9	8
SPIWPKEY[7:0]							

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SPIWPEN

- **SPIWPKEY: SPI Write Protection Key Password**

  If a value is written in SPIWPEN, the value is taken into account only if SPIWPKEY is written with “SPI” (SPI written in ASCII Code, i.e. 0x535049 in hexadecimal).
- **SPIWPEN: SPI Write Protection Enable**

  1: The Write Protection is Enabled

  0: The Write Protection is Disabled

22.8.3 Status Register

Name: SR

Access Type: Read-only

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	TXURCH		-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	RXORCH	

7	6	5	4	3	2	1	0
-	TXUR	TXRDY	TXEN	-	RXOR	RXRDY	RXEN

- **TXURCH: Transmit Underrun Channel**
  This field is cleared when SCR.TXUR is written to one
  Bit i of this field is set when a transmit underrun error occurred in channel i (i=0 for first channel of the frame)
- **RXORCH: Receive Overrun Channel**
  This field is cleared when SCR.RXOR is written to one
  Bit i of this field is set when a receive overrun error occurred in channel i (i=0 for first channel of the frame)
- **TXUR: Transmit Underrun**
  This bit is cleared when the corresponding bit in SCR is written to one
  This bit is set when an underrun error occurs on the THR register or when the corresponding bit in SSR is written to one
- **TXRDY: Transmit Ready**
  This bit is cleared when data is written to THR
  This bit is set when the THR register is empty and can be written with new data to be transmitted
- **TXEN: Transmitter Enabled**
  This bit is cleared when the Transmitter is effectively disabled, following a CR.TXDIS or CR.SWRST request
  This bit is set when the Transmitter is effectively enabled, following a CR.TXEN request
- **RXOR: Receive Overrun**
  This bit is cleared when the corresponding bit in SCR is written to one
  This bit is set when an overrun error occurs on the RHR register or when the corresponding bit in SSR is written to one
- **RXRDY: Receive Ready**
  This bit is cleared when the RHR register is read
  This bit is set when received data is present in the RHR register
- **RXEN: Receiver Enabled**
  This bit is cleared when the Receiver is effectively disabled, following a CR.RXDIS or CR.SWRST request
  This bit is set when the Receiver is effectively enabled, following a CR.RXEN request

23.9.3 SMBus Timing Register

Name: SMBTR

Access Type: Read/Write

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
EXP				-	-	-	-

23	22	21	20	19	18	17	16
THMAX							

15	14	13	12	11	10	9	8
TLOWM							

7	6	5	4	3	2	1	0
TLOWS							

- **EXP: SMBus Timeout Clock Prescaler**
  Used to specify how to prescale the TIM and TLOWM counters in SMBTR. Counters are prescaled according to the following formula

$$f_{prescaled,SMBus} = \frac{f_{CLKTWIM}}{2^{(EXP+1)}}$$

- **THMAX: Clock High Maximum Cycles**
  Clock cycles in clock high maximum count. Prescaled by SMBTR.EXP. Used for bus free detection. Used to time $T_{HIGH:MAX}$.
  NOTE: Uses the prescaler specified by CWGR, NOT the prescaler specified by SMBTR.
- **TLOWM: Master Clock Stretch Maximum Cycles**
  Clock cycles in master maximum clock stretch count. Prescaled by SMBTR.EXP. Used to time $T_{LOW:MEXT}$
- **TLOWS: Slave Clock Stretch Maximum Cycles**
  Clock cycles in slave maximum clock stretch count. Prescaled by SMBTR.EXP. Used to time $T_{LOW:SEXT}$.

25.7.14 Composite Waveform Generation

Name: CWG

Access Type: Read/Write

Offset: 0x3C+k*0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
XOR							

23	22	21	20	19	18	17	16
XOR							

15	14	13	12	11	10	9	8
XOR							

7	6	5	4	3	2	1	0
XOR							

- **XOR: Pair Waveform XOR'ed**
  If the bit *n* in XOR field is one, the pair of PWMA output waveforms will be XORed before output. The even number output will be the XOR'ed output and the odd number output will be reverse of it. For example, if bit 0 in XOR is one, the pair of PWMA output waveforms for channel 0 and 1 will be XORed together.
  If bit *n* in XOR is zero, normal waveforms are output for that pair. Note that
  If more than one CWG register is present, CWG0 controls the first 32 pairs, corresponding to channels 63 downto 0, and CWG1 controls the second 32 pairs, corresponding to channels 127 downto 64.

Figure 26-8. WAVSEL = 2 Without Trigger

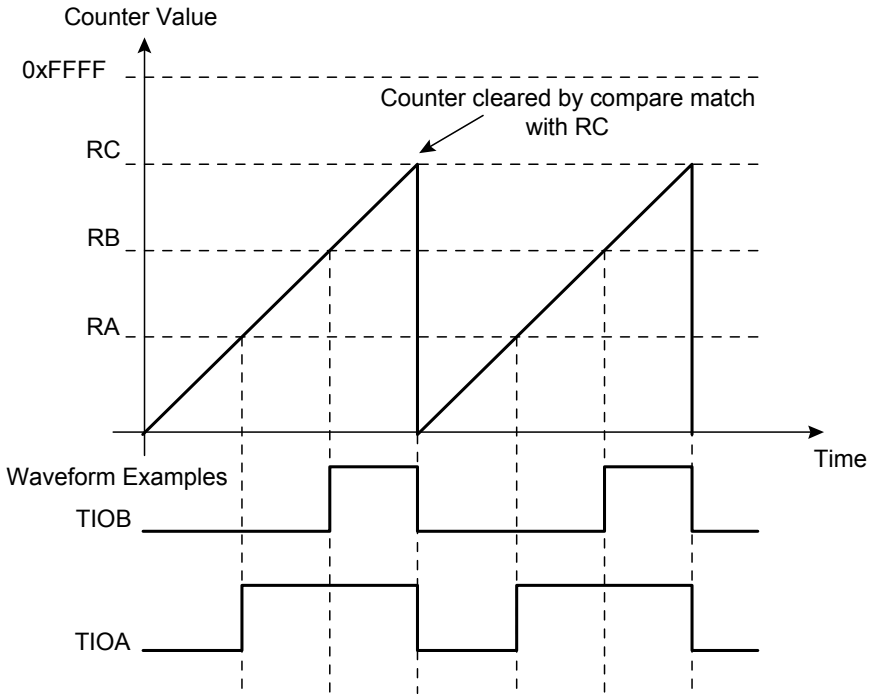
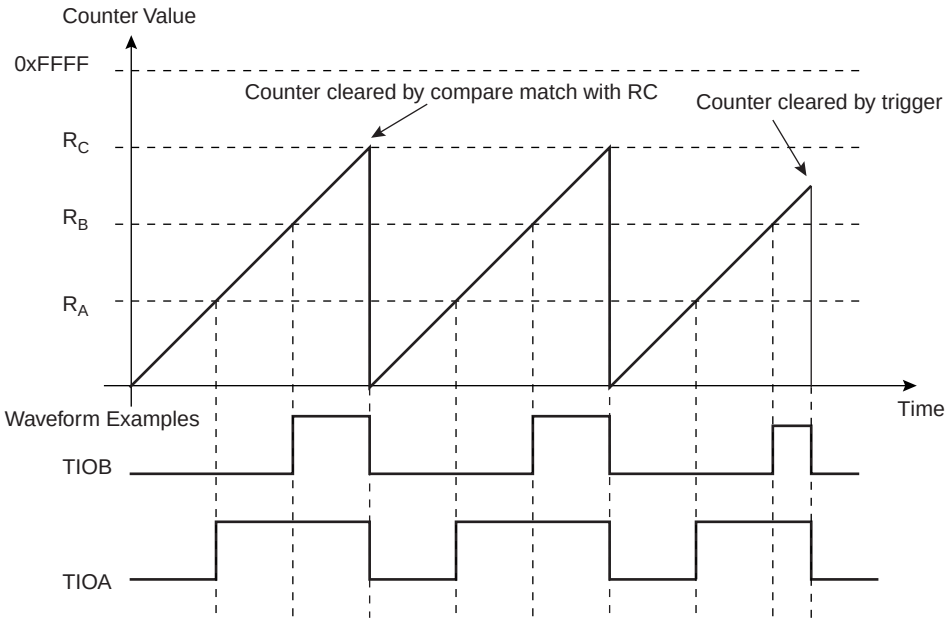


Figure 26-9. WAVSEL = 2 With Trigger



26.6.3.4 WAVSEL = 1

When CMRn.WAVSEL is one, the value of CVn is incremented from 0 to 0xFFFF. Once 0xFFFF is reached, the value of CVn is decremented to 0, then re-incremented to 0xFFFF and so on. See Figure 26-10 on page 541.

26.7.10 Channel Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x28 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

27.7.12 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x44

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
DMATSC	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	ACQDONE	ACREADY
7	6	5	4	3	2	1	0
-	-	-	-	-	ATSC	ATCAL	-

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will set the corresponding bit in IMR.

30.7.2 Status Register

Name: SR

Access Type: Read-only

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	TRMIS	-	-	OVERRUN	DREADYINT	READYINT
7	6	5	4	3	2	1	0
-	-	-	-	-	CENABLED	-	BUSY

- **TRMIS: Transmit Mismatch**
  0: No transfers mismatches.
  1: The transceiver was active when receiving.
  This bit is set when the transceiver is active when receiving.
  This bit is cleared when corresponding bit in SCR is written to one.
- **OVERRUN: Data Overrun**
  0: No data overwritten in RHR.
  1: Data in RHR has been overwritten before it has been read.
  This bit is set when data in RHR is overwritten before it has been read.
  This bit is cleared when corresponding bit in SCR is written to one.
- **DREADYINT: Data Ready Interrupt**
  0: No new data in the RHR.
  1: New data received and placed in the RHR.
  This bit is set when new data is received and placed in the RHR.
  This bit is cleared when corresponding bit in SCR is written to one.
- **READYINT: Ready Interrupt**
  0: The interface has not generated an ready interrupt.
  1: The interface has had a transition from busy to not busy.
  This bit is set when the interface has transition from busy to not busy.
  This bit is cleared when corresponding bit in SCR is written to one.

- **CENABLED: Clock Enabled**
  0: The aWire clock is not enabled.
  1: The aWire clock is enabled.

32. Electrical Characteristics

32.1 Disclaimer

All values in this chapter are preliminary and subject to change without further notice.

32.2 Absolute Maximum Ratings*

Table 32-1. Absolute Maximum Ratings

Operating temperature ..... -40°C to +85°C
Storage temperature ..... -60°C to +150°C
Voltage on input pins (except for 5V pins) with respect to ground .....-0.3V to V_{VDD}[2]+0.3V
Voltage on 5V tolerant[1] pins with respect to ground .....-0.3V to 5.5V
Total DC output current on all I/O pins - VDDIO 152mA
Total DC output current on all I/O pins - VDDANA..... 152mA
Maximum operating voltage VDDCORE..... 1.95V
Maximum operating voltage VDDIO, VDDIN 3.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. 5V tolerant pins, see Section 3.2 "Peripheral Multiplexing on I/O lines" on page 8

2. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3.2 on page 8 for details.

32.3 Supply Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C.

Table 32-2. Supply Characteristics

Symbol	Parameter	Voltage		
		Min	Max	Unit
V_{VDDIO}	DC supply peripheral I/Os	3.0	3.6	V
V_{VDDIN}	DC supply internal regulator, 3.3V single supply mode	3.0	3.6	V
$V_{VDDCORE}$	DC supply core	1.65	1.95	V
V_{VDDANA}	Analog supply voltage	3.0	3.6	V
$V_{ADVREFP}$	Analog reference voltage	2.6	V_{VDDANA}	V

32.4 Maximum Clock Frequencies

These parameters are given in the following conditions:

- $V_{VDDCORE}$ = 1.65 to 1.95V