18.7.19 Access Status Register

Name: ASR

Access: Read/Write

Offset : 0x1E4

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AE

- AE: Access Error
  This bit is set when a write to a locked register occurs.
  This bit can be written to 0 by software.

19.8 Module Configuration

Table 19-6. USBC Clocks

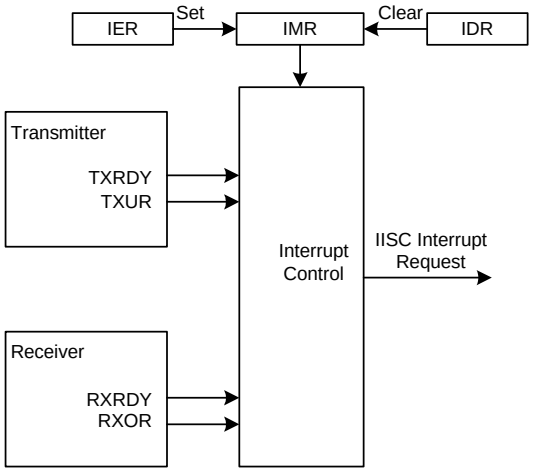
Clock Name	Description
CLK_USBC	Clock for the USBC bus interface
GCLK_USBC	48Mhz USB clock. This clock frequency must be configured to 48MHz. The generic clock used for the USBC is GCLK3

Table 19-7. Register Reset Values

Register	Reset Value
UVERS	0x00000200
UFEATURES	0x00000007
UADDRSIZE	0x00001000
UNAME1	0x48555342
UNAME2	0x00000000

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with NCPHA to produce the required clock/data relationship between master and slave devices.

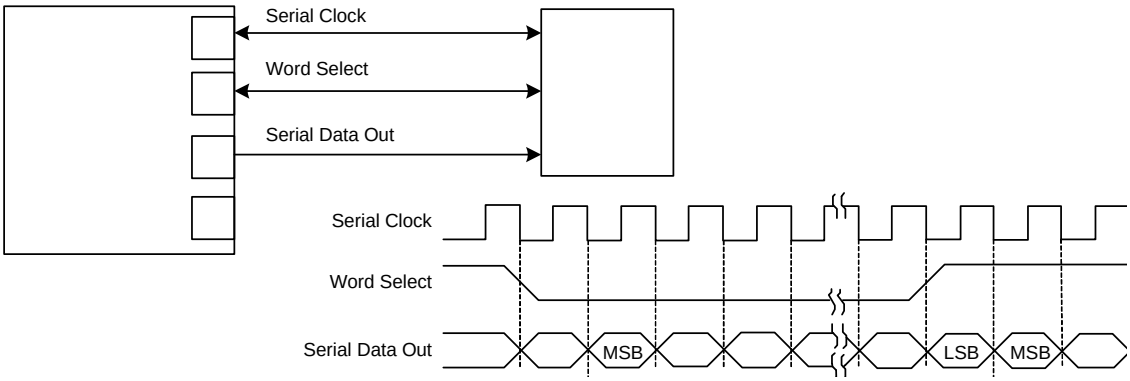
Figure 22-4. Interrupt Block Diagram



22.7 IISC Application Examples

The IISC can support several serial communication modes used in audio or high-speed serial links. Some standard applications are shown in the following figures. All serial link applications supported by the IISC are not listed here.

Figure 22-5. Audio Application Block Diagram



30.7.3 Status Clear Register

Name: SCR

Access Type: Write-only

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	TRMIS	-	-	OVERRUN	DREADYINT	READYINT

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in SR and the corresponding interrupt request.

31.5 JTAG and Boundary-scan (JTAG)

Rev: 2.2.2.4

31.5.1 Features

- IEEE1149.1 compliant JTAG Interface
- Boundary-scan Chain for board-level testing
- Direct memory access and programming capabilities through JTAG Interface

31.5.2 Overview

The JTAG Interface offers a four pin programming and debug solution, including boundary-scan support for board-level testing.

Figure 31-9 on page 692 shows how the JTAG is connected in an 32-bit AVR device. The TAP Controller is a state machine controlled by the TCK and TMS signals. The TAP Controller selects either the JTAG Instruction Register or one of several Data Registers as the scan chain (shift register) between the TDI-input and TDO-output.

The Instruction Register holds JTAG instructions controlling the behavior of a Data Register. The Device Identification Register, Bypass Register, and the boundary-scan chain are the Data Registers used for board-level testing. The Reset Register can be used to keep the device reset during test or programming.

The Service Access Bus (SAB) interface contains address and data registers for the Service Access Bus, which gives access to On-Chip Debug, programming, and other functions in the device. The SAB offers several modes of access to the address and data registers, as described in Section 31.5.11.

Section 31.6 lists the supported JTAG instructions, with references to the description in this document.

Starting in Run-Test/Idle, OCD registers are accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Shift-DR: Scan in the direction bit (1=read, 0=write) and the 7-bit address for the OCD register.
7. Go to Update-DR and re-enter Select-DR Scan.
8. In Shift-DR: For a read operation, scan out the contents of the addressed register. For a write operation, scan in the new contents of the register.
9. Return to Run-Test/Idle.

For any operation, the full 7 bits of the address must be provided. For write operations, 32 data bits must be provided, or the result will be undefined. For read operations, shifting may be terminated once the required number of bits have been acquired.

Table 31-47. NEXUS_ACCESS Details

Instructions	Details
IR input value	10000 (0x10)
IR output value	peb01
DR Size	34 bits
DR input value (Address phase)	aaaaaaar xxxxxxxx xxxxxxxx xxxxxxxx xx
DR input value (Data read phase)	xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx xx
DR input value (Data write phase)	ddddddddd ddddddddd ddddddddd ddddddddd xx
DR output value (Address phase)	xx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb
DR output value (Data read phase)	eb ddddddddd ddddddddd ddddddddd ddddddddd
DR output value (Data write phase)	xx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb

31.6.3.2 MEMORY_SERVICE

This instruction allows access to registers in an optional Memory Service Unit. The 7-bit register index, a read/write control bit, and the 32-bit data is accessed through the JTAG port.

The data register is alternately interpreted by the SAB as an address register and a data register. The SAB starts in address mode after the MEMORY_SERVICE instruction is selected, and toggles between address and data mode each time a data scan completes with the busy bit cleared.

Starting in Run-Test/Idle, Memory Service registers are accessed in the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Shift-DR: Scan in the direction bit (1=read, 0=write) and the 7-bit address for the Memory Service register.