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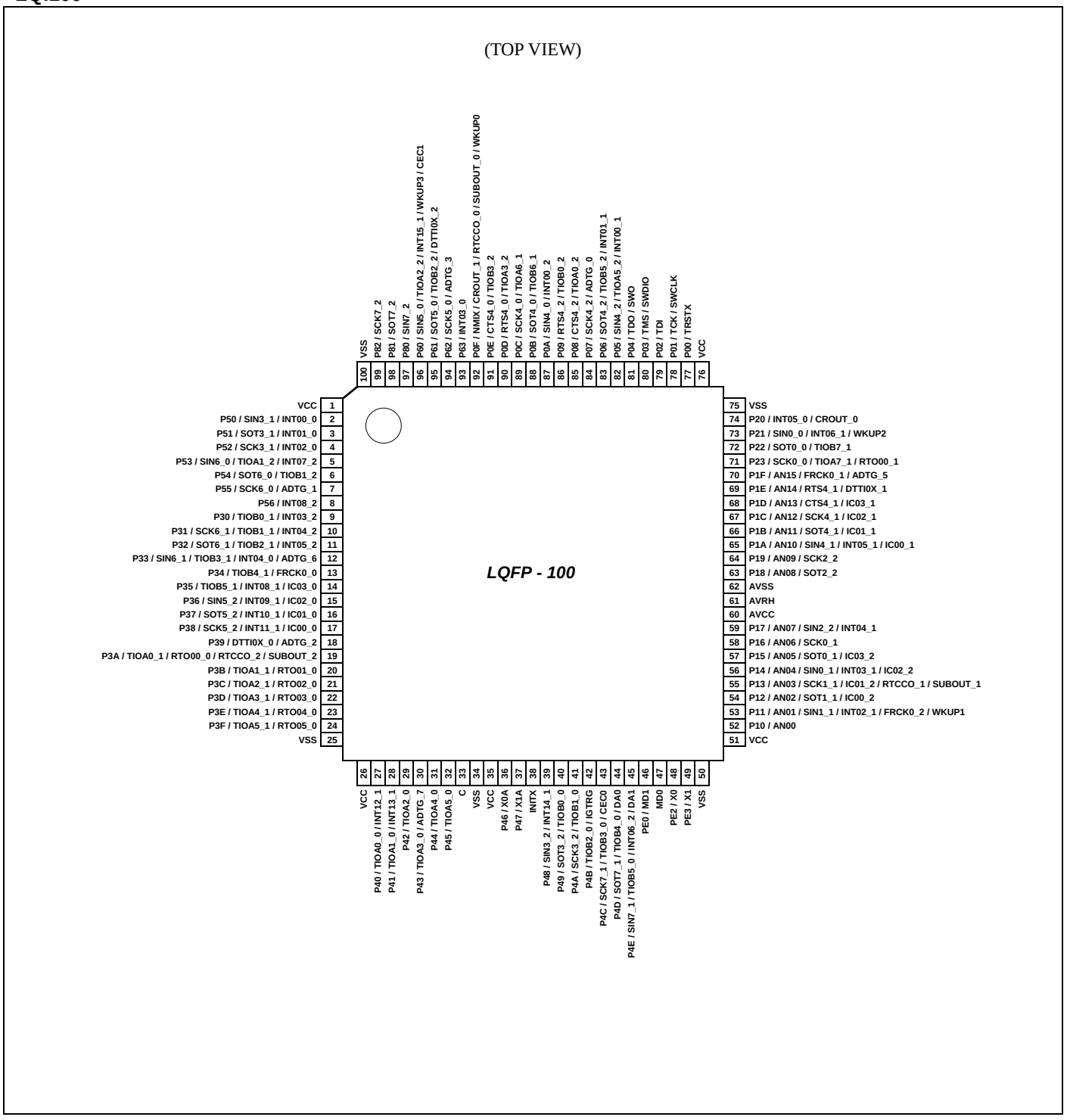
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSIO, I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9af1a2mpmc1-g-sne2

LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-80	LQFP-100	QFP-100			
13	17	22	100	P3D RTO03_0 (PPG02_0) TIOA3_1	E	H
14	18	23	1	P3E RTO04_0 (PPG04_0) TIOA4_1	E	H
15	19	24	2	P3F RTO05_0 (PPG04_0) TIOA5_1	E	H
16	20	25	3	VSS	-	
-	-	26	4	VCC	-	
-	-	27	5	P40 TIOA0_0 INT12_1	E	F
-	-	28	6	P41 TIOA1_0 INT13_1	E	F
-	-	29	7	P42 TIOA2_0	E	H
-	-	30	8	P43 TIOA3_0 ADTG_7	E	H
-	21	31	9	P44 TIOA4_0	E	H
-	22	32	10	P45 TIOA5_0	E	H
17	23	33	11	C	-	
-	24	34	12	VSS	-	
18	25	35	13	VCC	-	
19	26	36	14	P46 X0A	D	M
20	27	37	15	P47 X1A	D	N
21	28	38	16	INITX	B	C
-	29	39	17	P48 INT14_1 SIN3_2	E	F

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-80	LQFP-100	QFP-100			
36	44	54	32	P12 AN02 SOT1_1 (SDA1_1) IC00_2	F	J
37	45	55	33	P13 AN03 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1	F	J
38	46	56	34	P14 AN04 IC02_2 INT03_1	F	K
-				SIN0_1		
39	47	57	35	P15 AN05 IC03_2	F	J
-				SOT0_1 (SDA0_1)		
-	48	58	36	P16 AN06 SCK0_1 (SCL0_1)	F	J
40	49	59	37	P17 AN07 SIN2_2 INT04_1	F	K
41	50	60	38	AVCC	-	
42	51	61	39	AVRH	-	
43	52	62	40	AVSS	-	
44	53	63	41	P18 AN08 SOT2_2 (SDA2_2)	F	J
45	54	64	42	P19 AN09 SCK2_2 (SCL2_2)	F	J

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64	LQFP-80	LQFP-100	QFP-100			
-	70	90	68	P0D RTS4_0 TIOA3_2	E	H
-	71	91	69	P0E CTS4_0 TIOB3_2	E	H
57	72	92	70	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 WKUP0	E	I
-	73	93	71	P63 INT03_0	E	O
58	74	94	72	P62 SCK5_0 (SCL5_0) ADTG_3	E	H
59	75	95	73	P61 SOT5_0 (SDA5_0) TIOB2_2 DTTI0X_2	E	H
60	76	96	74	P60 SIN5_0 TIOA2_2 INT15_1 WKUP3 CEC1	G	R
61	77	97	75	P80 SIN7_2	G	H
62	78	98	76	P81 SOT7_2 (SDA7_2)	G	H
63	79	99	77	P82 SCK7_2 (SCL7_2)	G	H
64	80	100	78	VSS	-	

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

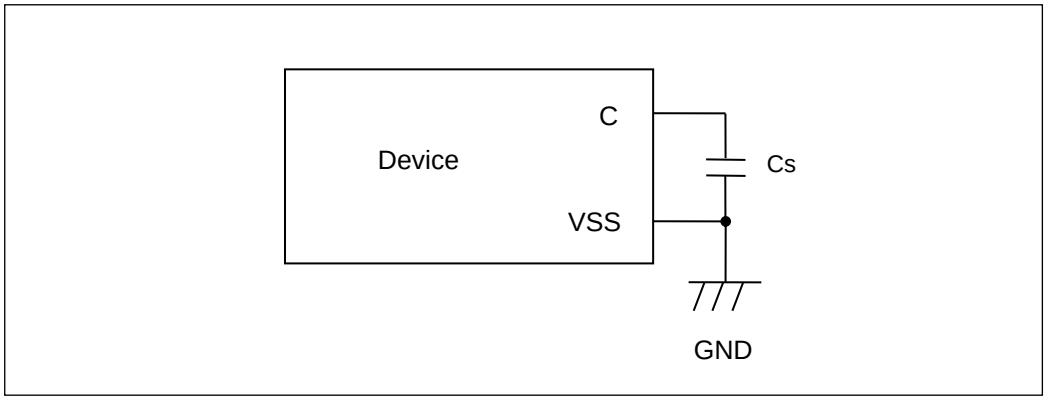
Pin function	Pin name	Function description	Pin No			
			LQFP-64	LQFP-80	LQFP-100	QFP-100
ADC	ADTG_0	A/D converter external trigger input pin	-	66	84	62
	ADTG_1		-	7	7	85
	ADTG_2		9	13	18	96
	ADTG_3		58	74	94	72
	ADTG_4		-	-	-	-
	ADTG_5		-	-	70	48
	ADTG_6		8	12	12	90
	ADTG_7		-	-	30	8
	ADTG_8		-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	34	42	52	30
	AN01		35	43	53	31
	AN02		36	44	54	32
	AN03		37	45	55	33
	AN04		38	46	56	34
	AN05		39	47	57	35
	AN06		-	48	58	36
	AN07		40	49	59	37
	AN08		44	53	63	41
	AN09		45	54	64	42
	AN10		-	55	65	43
	AN11		-	56	66	44
	AN12		-	-	67	45
	AN13		-	-	68	46
	AN14		-	-	69	47
	AN15		-	-	70	48

Pin function	Pin name	Function description	Pin No			
			LQFP-64	LQFP-80	LQFP-100	QFP-100
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	-	-	27	5
	TIOA0_1		10	14	19	97
	TIOA0_2		-	-	85	63
	TIOB0_0	Base timer ch.0 TIOB pin	22	30	40	18
	TIOB0_1		5	9	9	87
	TIOB0_2		-	-	86	64
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	-	-	28	6
	TIOA1_1		11	15	20	98
	TIOA1_2		-	5	5	83
	TIOB1_0	Base timer ch.1 TIOB pin	23	31	41	19
	TIOB1_1		6	10	10	88
	TIOB1_2		-	6	6	84
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	-	-	29	7
	TIOA2_1		12	16	21	99
	TIOA2_2		60	76	96	74
	TIOB2_0	Base timer ch.2 TIOB pin	24	32	42	20
	TIOB2_1		7	11	11	89
	TIOB2_2		59	75	95	73
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	-	-	30	8
	TIOA3_1		13	17	22	100
	TIOA3_2		-	70	90	68
	TIOB3_0	Base timer ch.3 TIOB pin	25	33	43	21
	TIOB3_1		8	12	12	90
	TIOB3_2		-	71	91	69
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	-	21	31	9
	TIOA4_1		14	18	23	1
	TIOA4_2		-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	26	34	44	22
	TIOB4_1		-	-	13	91
	TIOB4_2		-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	-	22	32	10
	TIOA5_1		15	19	24	2
	TIOA5_2		-	-	82	60
	TIOB5_0	Base timer ch.5 TIOB pin	27	35	45	23
	TIOB5_1		-	-	14	92
	TIOB5_2		-	-	83	61
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	56	69	89	67
	TIOB6_1	Base timer ch.6 TIOB pin	55	68	88	66
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-
	TIOA7_1		46	57	71	49
	TIOA7_2		-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-
	TIOB7_1		47	58	72	50
	TIOB7_2		-	-	-	-

Pin function	Pin name	Function description	Pin No			
			LQFP-64	LQFP-80	LQFP-100	QFP-100
Debugger	SWCLK	Serial wire debug interface clock input pin	50	62	78	56
	SWDIO	Serial wire debug interface data input / output pin	52	64	80	58
	SWO	Serial wire viewer output pin	53	65	81	59
	TRSTX	JTAG reset input pin	49	61	77	55
	TCK	JTAG test clock input pin	50	62	78	56
	TDI	JTAG test data input pin	51	63	79	57
	TMS	JTAG test mode state input/output pin	52	64	80	58
	TDO	JTAG debug data output pin	53	65	81	59
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	80
	INT00_1		-	-	82	60
	INT00_2		54	67	87	65
	INT01_0	External interrupt request 01 input pin	3	3	3	81
	INT01_1		-	-	83	61
	INT02_0	External interrupt request 02 input pin	4	4	4	82
	INT02_1		35	43	53	31
	INT03_0	External interrupt request 03 input pin	-	73	93	71
	INT03_1		38	46	56	34
	INT03_2		5	9	9	87
	INT04_0	External interrupt request 04 input pin	8	12	12	90
	INT04_1		40	49	59	37
	INT04_2		6	10	10	88
	INT05_0	External interrupt request 05 input pin	-	60	74	52
	INT05_1		-	55	65	43
	INT05_2		7	11	11	89
	INT06_1	External interrupt request 06 input pin	48	59	73	51
	INT06_2		27	35	45	23
	INT07_2	External interrupt request 07 input pin	-	5	5	83
	INT08_1	External interrupt request 08 input pin	-	-	14	92
	INT08_2		-	8	8	86
	INT09_1	External interrupt request 09 input pin	-	-	15	93
	INT10_1	External interrupt request 10 input pin	-	-	16	94
	INT11_1	External interrupt request 11 input pin	-	-	17	95
	INT12_1	External interrupt request 12 input pin	-	-	27	5
	INT13_1	External interrupt request 13 input pin	-	-	28	6
	INT14_1	External interrupt request 14 input pin	-	29	39	17
	INT15_1	External interrupt request 15 input pin	60	76	96	74
	NMIX	Non-Maskable Interrupt input pin	57	72	92	70

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (CS) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC → AVCC → AVRH

Turning off: AVRH → AVCC → VCC

Serial Communication

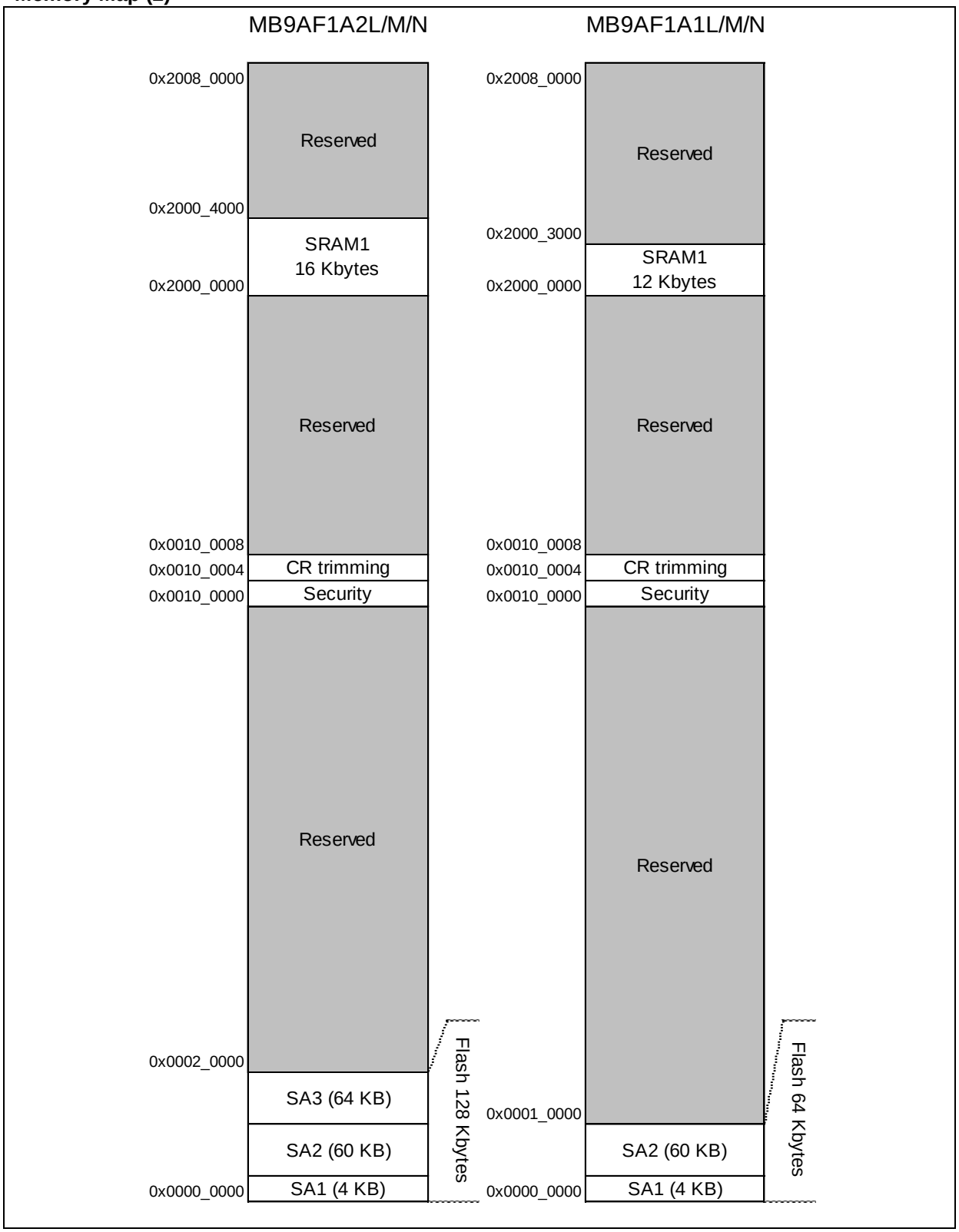
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Memory Map (2)



*: See MB9AAA0N/1A0N/A30N/130N/130L Series Flash Programming Manual to confirm the detail of Flash memory.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Reserved
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Reserved
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver
0x4003_5000	0x4003_50FF		Low-Voltage Detector
0x4003_5100	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	Maintain previous state	Hi-Z / input enabled	Maintain previous state
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
S	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled		Maintain previous state	Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state
T	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

*1: Oscillation is stopped at Sub run mode, Low-speed CR Run mode, Sub Sleep mode, Low-speed CR Sleep mode, Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

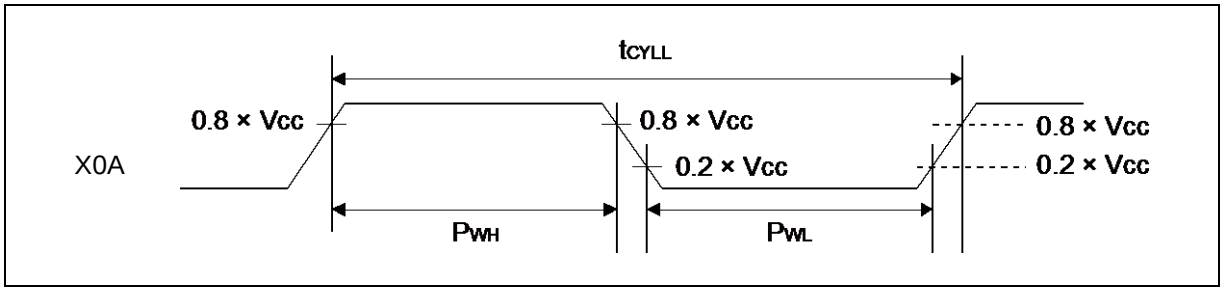
*3: Maintain previous state at Timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*4: Maintain previous state at Timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

12.4.2 Sub Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

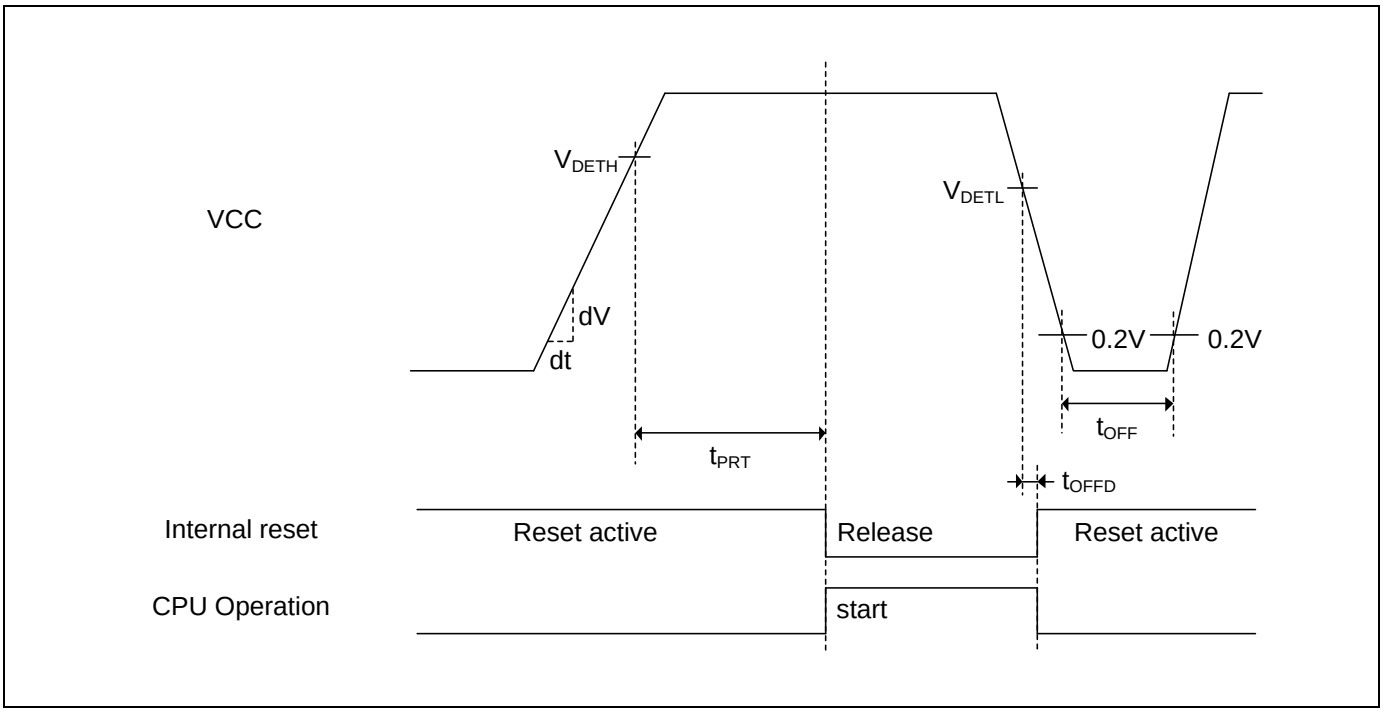
Built-in High-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions		Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CRH}	V_{CC} ≥ 2.2 V	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.8	4	4.2		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
		V_{CC} < 2.2 V	T_A = + 25°C	3.4	4	4.6	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.16	4	4.84		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
Frequency stabilization time	t_{CRWT}	-		-	-	10	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value.
This period is able to use High-speed CR clock as source clock.

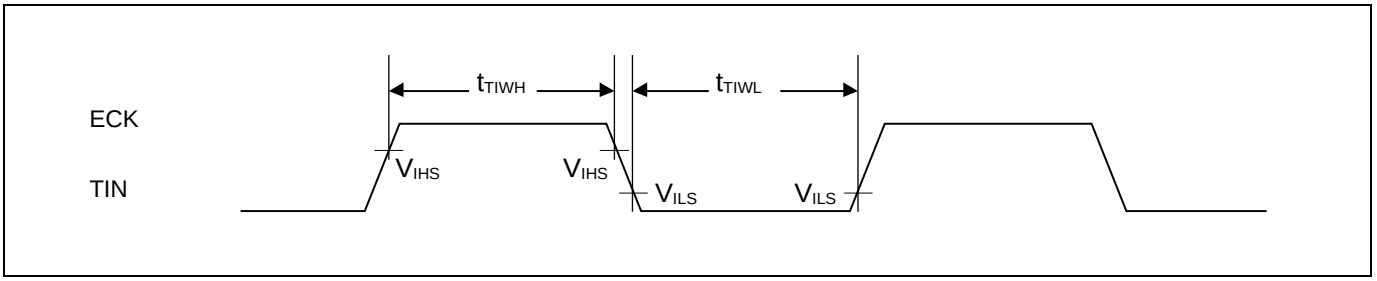


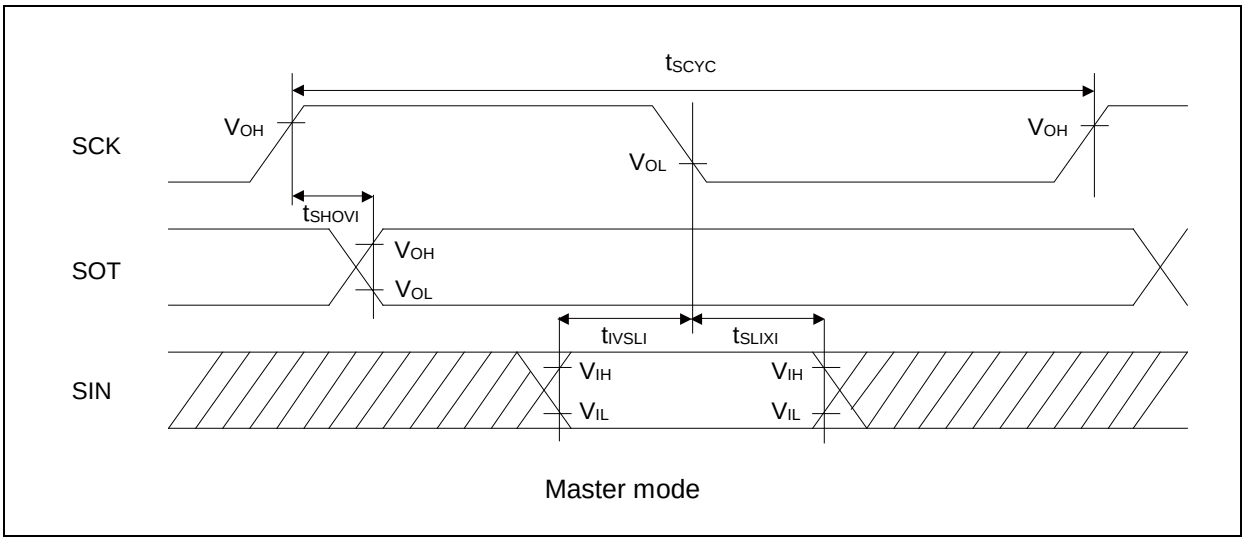
12.4.8 Base Timer Input Timing

Timer input timing

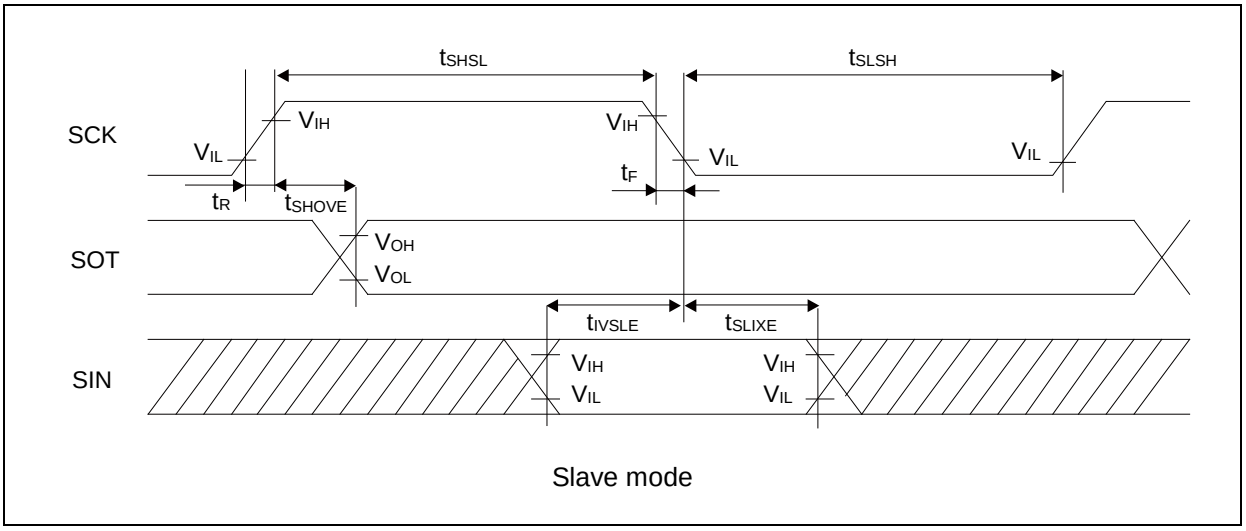
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	





Master mode



Slave mode

CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤ V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 50 pF.*

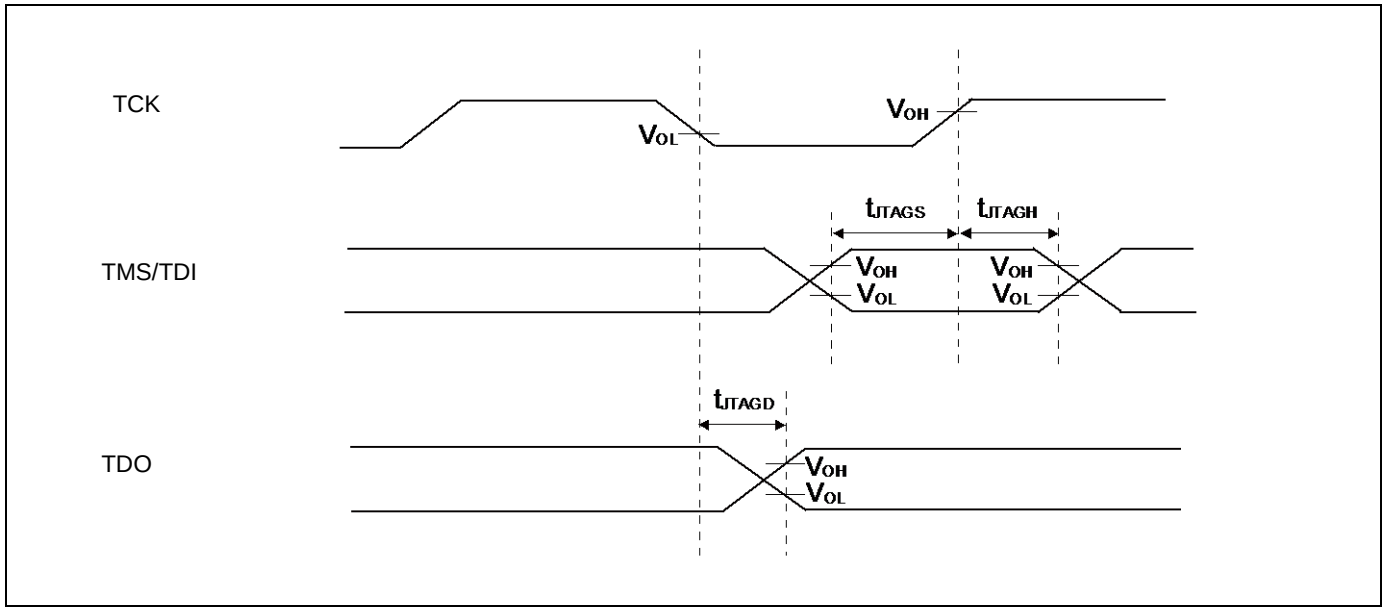
12.4.12 JTAG Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK, TMS,TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS,TDI hold time	t_{JTAGH}	TCK, TMS,TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	30	ns	
			2.7 V $\leq V_{CC} < 4.5$ V	-	45		
			$V_{CC} < 2.7$ V	-	60		

Note:

- *When the external load capacitance C_L = 50 pF.*



12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

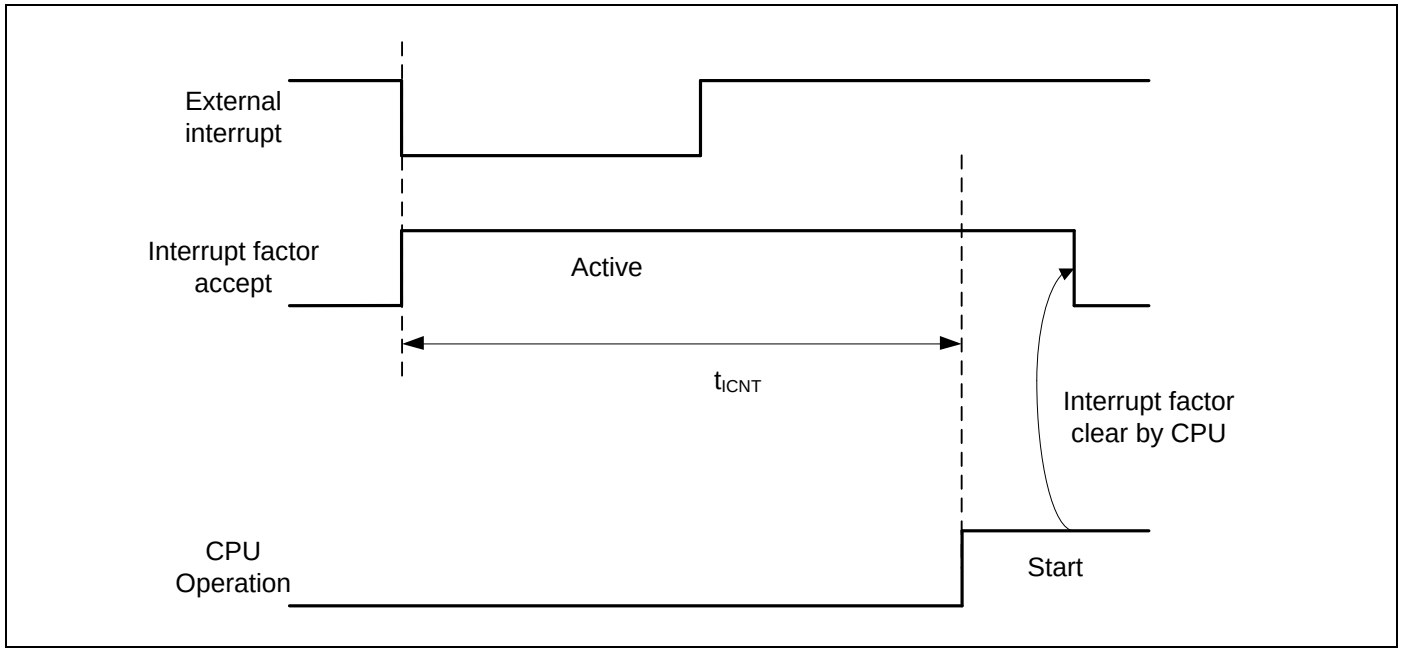
Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		630	1260	µs	
Sub Timer mode		630	1260	µs	
RTC mode, Stop mode		1083	2100	µs	
Deep Standby RTC mode Deep Standby Stop mode		1099	2127	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Major Changes

Spansion Publication Number: DS706-00068

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
-	-	Changed from Preliminary to Full Producton
-	-	Deleted a part of QFN
43	BLOCK DIAGRAM	Added note for MB9AF1AxL
58,59	ELECTRICAL CHARACTERISTICS 3.DC Characteristics (1) Current Rating	Revised the values of “TBD”
Revision 2.0		
2	Features · On-chip Memories	Changed the description of on-chip SRAM
7 - 31	Packages Pin Assignment List of Pin Functions	Deleted QFN package
40	Handling Devices Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
44	Memory Map · Memory map(2)	Added the summary of Flash memory sector
57 - 59	Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main Timer mode current · Added Flash Memory Current · Moved A/D Converter Current · Moved D/A Converter Current
60	Electrical Characteristics 3. DC Characteristics (2) Pin Characteristics	Added the input leak current of CEC port at power off
63	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added the figure of Main PLL connection
64	Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	· Changed the figure of timing · Changed from Reset release delay time(t_{OND}) to Time until releasing Power-on reset(t_{PRT})
66 - 73	Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
77	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AV_{CC} < 2.7 V
81	Electrical Characteristics 7. Low-voltage Detection Characteristics	Deleted the figure
84	Electrical Characteristics 8. Flash Memory Write/Erase Characteristics	Change to the erase time of include write time prior to internal erase

Page	Section	Change Results
85 - 88	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
89	Ordering Information	Changed notation of part number

NOTE: Please see “Document History” about later revised information.