# Infineon Technologies - MB91F467BAPMC-GSE2-W001 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | FR60 RISC |
| Core Size | 32-Bit Single-Core |
| Speed | 96MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, PWM, WDT |
| Number of I/O | 108 |
| Program Memory Size | 1.0625MB (1.0625M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 32x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w001 |

and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

- Clock modulator
- Clock monitor
- Sub-clock calibration
  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

### Package and Technology

- Package: QFP-144
- CMOS 180 nm technology

- Main oscillator stabilization timer
  Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 125°C

3. ICU: MD3=1: Do not set PFR = 1 & EPFR = 1 (for LIN Synch Field detect).
4. OCU: MD3=1: You cannot use external out-port (but, OCU-function is active.)
5. Reload Timer: MD3=1: CH 7, 6, 5, and 4 cannot select external event
6. PPG: MD3=1: You can use CH15 to 8 of PPG. CH15 to12 cannot select external trigger.
7. Up/Down Counter: MD3=1: You can use Timer-mode only.
8. LIN-USART CH 0 (shared with external bus) can be used for asynchronous mode only.
9. External Interrupts: INT7 to INT4(shared with external bus) can be used for MD3=0 mode only. INT0 (shared with external bus) can be used for MD3=0 mode only.

### 3.1.1 Power supply/Ground pins

| Pin no. | Pin name | I/O | Function |
|---|---|---|---|
| 1, 19, 37, 55, 73, 81, 86, 91, 109, 127 | VSS5 | Supply | Ground pins |
| 54, 72, 90, 108, 126 | VDD5 | | Power supply pins |
| 88, 89 | VDD5R | | Power supply pins for internal regulator |
| 105 | AVSS5 | | Analog ground pin for A/D converter |
| 107 | AVCC5 | | Power supply pin for A/D converter |
| 106 | AVRH5 | | Reference power supply pin for A/D converter |
| 87 | VCC18C | | Capacitor connection pin for internal regulator |
| 18, 36, 144 | VDD35 | | Power supply pins for external bus part of I/O ring |

| Pin no. | Pin name | I/O | I/O circuit type[1] | Function |
|---|---|---|---|---|
| 95 | P19_4 | I/O | A | General-purpose input/output ports |
| | SIN5 | | | Data input pin of USART5 |
| 96 | P19_5 | I/O | A | General-purpose input/output ports |
| | SOT5 | | | Data output pin of USART5 |
| 97 | P19_6 | I/O | A | General-purpose input/output ports |
| | SCK5 | | | Clock input/output pin of USART5 |
| | CK5 | | | External clock input pin of free-run timer 5 |
| 98 | P18_0 | I/O | A | General-purpose input/output ports |
| | SIN6 | | | Data input pin of USART6 |
| 99 | P18_1 | I/O | A | General-purpose input/output ports |
| | SOT6 | | | Data output pin of USART6 |
| 100 | P18_2 | I/O | A | General-purpose input/output ports |
| | SCK6 | | | Clock input/output pin of USART6 |
| | CK6 | | | External clock input pin of free-run timer 6 |
| 101 | P18_4 | I/O | A | General-purpose input/output ports |
| | SIN7 | | | Data input pin of USART7 |
| 102 | P18_5 | I/O | A | General-purpose input/output ports |
| | SOT7 | | | Data output pin of USART7 |
| 103 | P18_6 | I/O | A | General-purpose input/output ports |
| | SCK7 | | | Clock input/output pin of USART7 |
| | CK7 | | | External clock input pin of free-run timer 7 |
| 104 | ALARM_0 | I | N | Alarm comparator input pin |
| 110 to 117 | P29_0 to P29_7 | I/O | B | General-purpose input/output ports |
| | AN0 to AN7 | | | Analog input pins of A/D converter |
| 118 to 125 | P28_0 to P28_7 | I/O | B | General-purpose input/output ports |
| | AN8 to AN15 | | | Analog input pins of A/D converter |
| 128 | P24_2 | I/O | A | General-purpose input/output ports |
| | INT2 | | | External interrupt input pin |
| 129 | P24_3 | I/O | A | General-purpose input/output ports |
| | INT3 | | | External interrupt input pin |
| 130 to 133 | P14_0 to P14_3 | I/O | A | General-purpose input/output ports |
| | ICU0 to ICU3 | | | Input capture input pins |
| | TIN0 to TIN3 | | | External trigger input pins of reload timer |
| | TTG0/8 to TTG3/11 | | | External trigger input pins of PPG timer |
| 134 to 137 | P15_0 to P15_3 | I/O | A | General-purpose input/output ports |
| | OCU0 to OCU3 | | | Output compare output pins |
| | TOT0 to TOT3 | | | Reload timer output pins |
| 138 to 143 | P27_0 to P27_5 | I/O | B | General-purpose input/output ports |
| | AN16 to AN21 | | | Analog input pins of A/D converter |

1. For information about the I/O circuit type, refer to “I/O Circuit Types”.

# 6. Notes on Debugger

## 6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

## 6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

## 6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

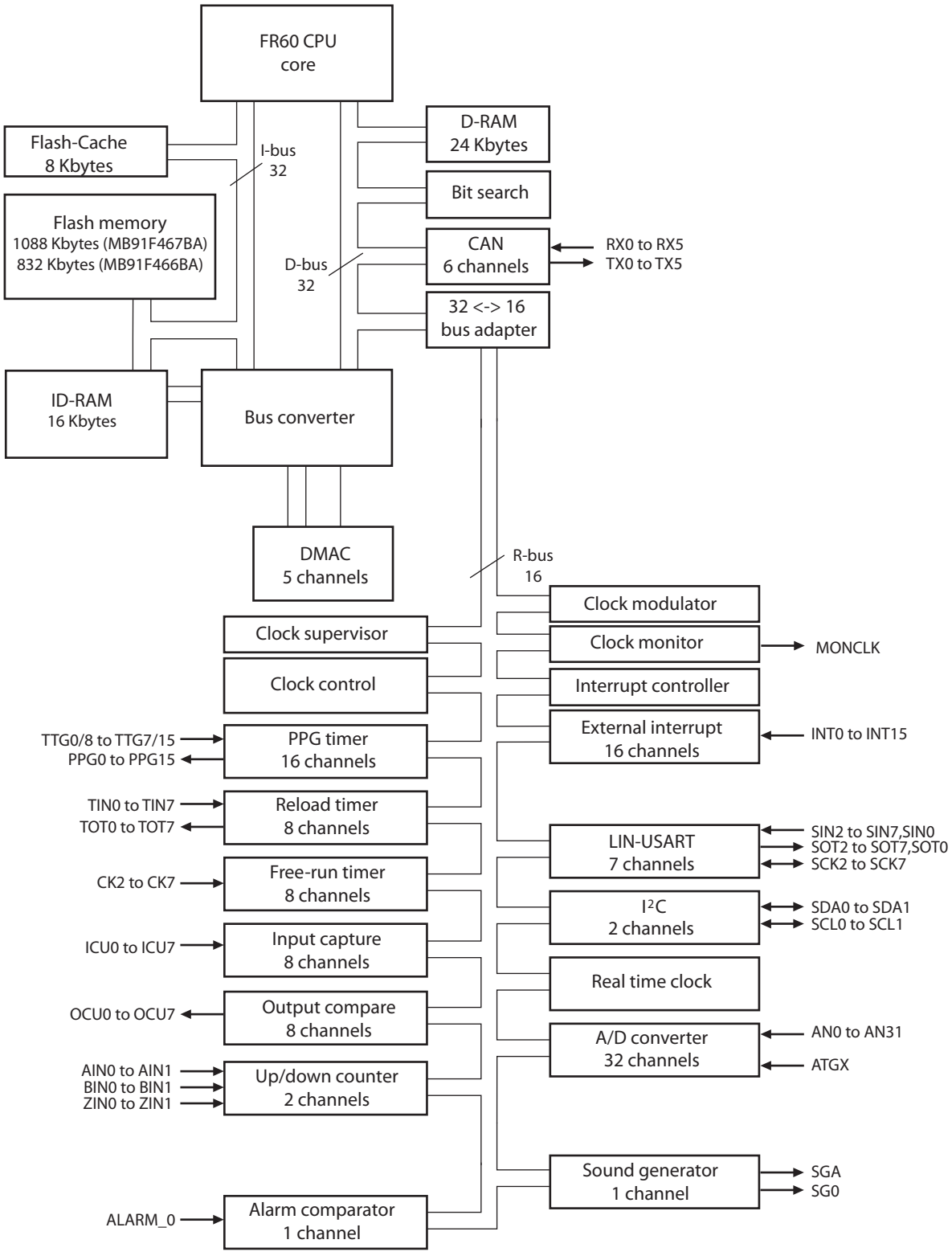
## 6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,the operation before and after the EIT always proceeds according to specification.

- **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**
  (a) a user interrupt or NMI is accepted;
  (b) single-step execution is performed;
  (c) execution breaks due to a data event or from the emulator menu.
  1. D0 and D1 flags are updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

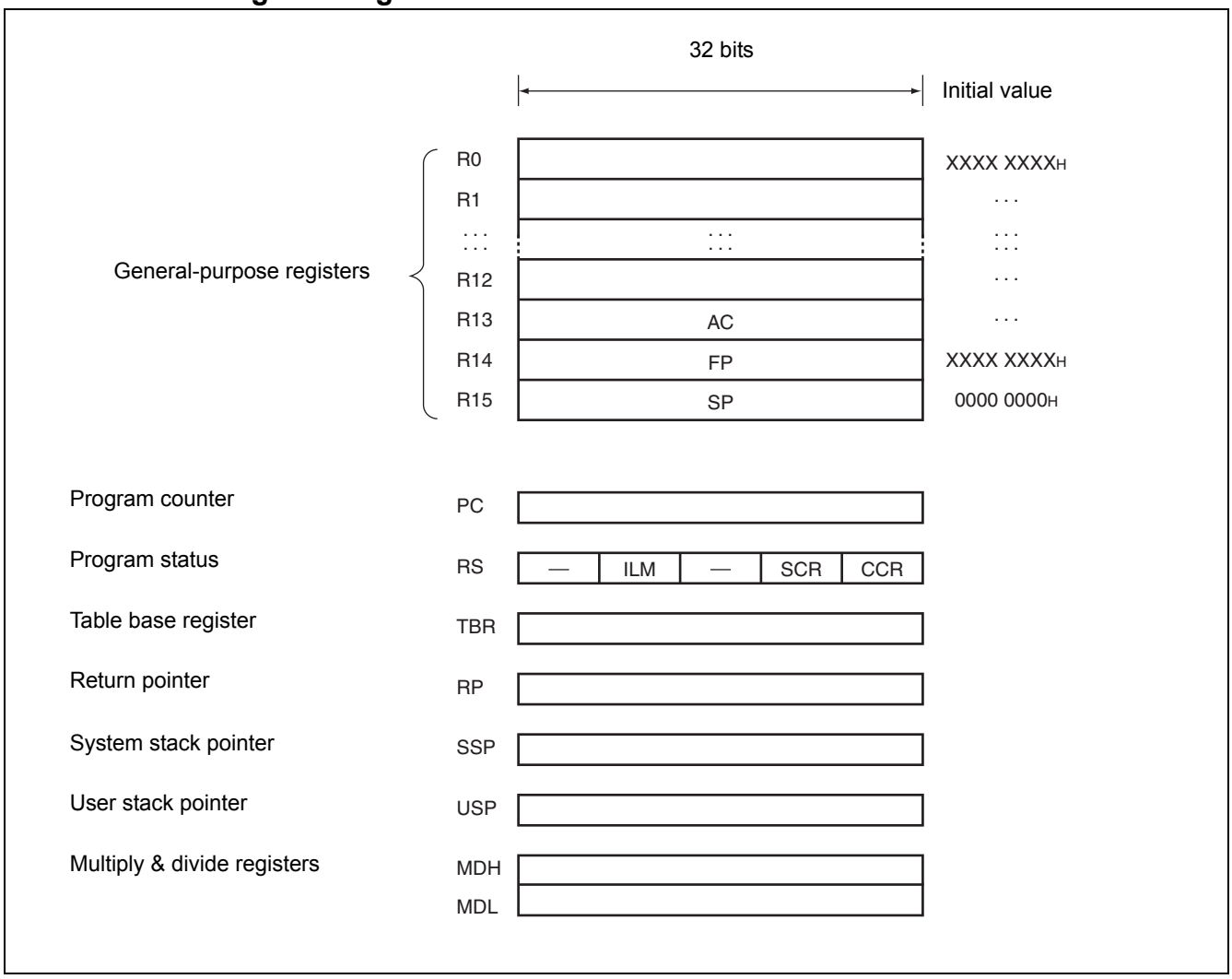
- **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**
  1. The PS register is updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

## 7.2 MB91F467BA/466BA with MD_3=0



## 8.3 Programming Model

### 8.3.1 Basic Programming Model



| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $0001C0_H$ | TMRLR2 [W]<br>XXXXXXXX XXXXXXXX | | TMR2 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 2<br>(PPG 4, PPG 5) |
| $0001C4_H$ | Reserved | | TMCSRH2<br>[R/W]<br>- - - 00000 | TMCSRL2<br>[R/W]<br>0 - 000000 | |
| $0001C8_H$ | TMRLR3 [W]<br>XXXXXXXX XXXXXXXX | | TMR3 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 3<br>(PPG 6, PPG 7) |
| $0001CC_H$ | Reserved | | TMCSRH3<br>[R/W]<br>- - - 00000 | TMCSRL3<br>[R/W]<br>0 - 000000 | |
| $0001D0_H$ | TMRLR4 [W]<br>XXXXXXXX XXXXXXXX | | TMR4 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 4<br>(PPG 8, PPG 9) |
| $0001D4_H$ | Reserved | | TMCSRH4<br>[R/W]<br>- - - 00000 | TMCSRL4<br>[R/W]<br>0 - 000000 | |
| $0001D8_H$ | TMRLR5 [W]<br>XXXXXXXX XXXXXXXX | | TMR5 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 5<br>(PPG 10, PPG 11) |
| $0001DC_H$ | Reserved | | TMCSRH5<br>[R/W]<br>- - - 00000 | TMCSRL5<br>[R/W]<br>0 - 000000 | |
| $0001E0_H$ | TMRLR6 [W]<br>XXXXXXXX XXXXXXXX | | TMR6 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 6<br>(PPG 12, PPG 13) |
| $0001E4_H$ | Reserved | | TMCSRH6<br>[R/W]<br>- - - 00000 | TMCSRL6<br>[R/W]<br>0 - 000000 | |
| $0001E8_H$ | TMRLR7 [W]<br>XXXXXXXX XXXXXXXX | | TMR7 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 7<br>(PPG 14, PPG 15)<br>(A/D Converter) |
| $0001EC_H$ | Reserved | | TMCSRH7<br>[R/W]<br>- - - 00000 | TMCSRL7<br>[R/W]<br>0 - 000000 | |
| $0001F0_H$ | TCDT0 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS0 [R/W]<br>00000000 | Free Running Timer 0<br>(ICU 0, ICU 1) |
| $0001F4_H$ | TCDT1 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS1 [R/W]<br>00000000 | Free Running Timer 1<br>(ICU 2, ICU 3) |
| $0001F8_H$ | TCDT2 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS2 [R/W]<br>00000000 | Free Running Timer 2<br>(OCU 0, OCU 1) |
| $0001FC_H$ | TCDT3 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS3 [R/W]<br>00000000 | Free Running Timer 3<br>(OCU 2, OCU 3) |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000200_H$ | DMACA0 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| $000204_H$ | DMACB0 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000208_H$ | DMACA1 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $00020C_H$ | DMACB1 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000210_H$ | DMACA2 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $000214_H$ | DMACB2 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000218_H$ | DMACA3 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $00021C_H$ | DMACB3 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000220_H$ | DMACA4 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| $000224_H$ | DMACB4 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000228_H$ to $00023C_H$ | Reserved | | | | |
| $000240_H$ | DMACR [R/W]<br>00 - - 0000 | Reserved | | | |
| $000244_H$ to $0002CC_H$ | Reserved | | | | Reserved |
| $0002D0_H$ | Reserved | ICS045 [R/W]<br>00000000 | Reserved | ICS67 [R/W]<br>00000000 | Input Capture<br>4 to 7 |
| $0002D4_H$ | IPCP4 [R]<br>XXXXXXXX XXXXXXXX | | IPCP5 [R]<br>XXXXXXXX XXXXXXXX | | |
| $0002D8_H$ | IPCP6 [R]<br>XXXXXXXX XXXXXXXX | | IPCP7 [R]<br>XXXXXXXX XXXXXXXX | | |
| $0002DC_H$ | OCS45 [R/W]<br>- - - 0 - - 00 0000 - - 00 | | OCS67 [R/W]<br>- - - 0 - - 00 0000 - - 00 | | Output Compare<br>4 to 7 |
| $0002E0_H$ | OCCP4 [R/W]<br>XXXXXXXX XXXXXXXX | | OCCP5 [R/W]<br>XXXXXXXX XXXXXXXX | | |
| $0002E4_H$ | OCCP6 [R/W]<br>XXXXXXXX XXXXXXXX | | OCCP7 [R/W]<br>XXXXXXXX XXXXXXXX | | |
| $0002E8_H$ to $0002EC_H$ | Reserved | | | | Reserved |
| $0002F0_H$ | TCDT4 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS4 [R/W]<br>00000000 | Free Running Timer 4<br>(ICU 4, ICU 5) |
| $0002F4_H$ | TCDT5 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS5 [R/W]<br>00000000 | Free Running Timer 5<br>(ICU 6, ICU 7) |
| $0002F8_H$ | TCDT6 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS6 [R/W]<br>00000000 | Free Running Timer 6<br>(OCU 4, OCU 5) |
| $0002FC_H$ | TCDT7 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS7 [R/W]<br>00000000 | Free Running Timer 7<br>(OCU 6, OCU 7) |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $0004A0_H$ | Reserved | WTCER [R/W]<br>- - - - - - 00 | WTCR [R/W]<br>00000000 000 - 00 - 0 | | Real Time Clock (Watch Timer) |
| $0004A4_H$ | Reserved | WTBR [R/W]<br>- - - XXXXX XXXXXXXX XXXXXXXX | | | |
| $0004A8_H$ | WTHR [R/W]<br>- - - 00000 | WTMR [R/W]<br>- - 000000 | WTSR [R/W]<br>- - 000000 | Reserved | |
| $0004AC_H$ | CSVTR [R/W]<br>- - - 00010 | CSVCR [R/W]<br>- 011100 | CSCFG [R/W]<br>0X000000 | CMCFG [R/W]<br>00000000 | Clock- Supervisor / Selector/ Monitor |
| $0004B0_H$ | CUCR [R/W]<br>- - - - - - - - - - - - 0 - - 00 | | CUTD [R/W]<br>10000000 00000000 | | Calibration of Sub Clock |
| $0004B4_H$ | CUTR1 [R]<br>- - - - - - - - 00000000 | | CUTR2 [R]<br>00000000 00000000 | | |
| $0004B8_H$ | CMPR [R/W]<br>- - 000010 11111101 | | Reserved | CMCR [R/W]<br>- 001 - - 00 | Clock Modulator |
| $0004BC_H$ | CMT1 [R/W]<br>00000000 1 - - - 0000 | | CMT2 [R/W]<br>- - 000000 - - 000000 | | |
| $0004C0_H$ | CANPRE [R/W]<br>0 - - - 0000 | CANCKD [R/W]<br>- - 000000 | Reserved | | CAN Clock Control |
| $0004C4_H$ | LVSEL [R/W]<br>00000111 | LVDET [R/W]<br>00000 - 00 | HWWDE [R/W]<br>- - - - - - 00 | HWWD [R/W,W]<br>00011000 | Low Voltage Detection/ Hardware Watchdog |
| $0004C8_H$ | OSCRH [R/W]<br>000 - - 001 | OSCRL [R/W]<br>- - - - - 000 | WPCRH [R/W]<br>000 - - 001 | WPCRL [R/W]<br>- - - - - - 00 | Main-/Sub-Oscillation Stabilisation Timer |
| $0004CC_H$ | OSCCR [R/W]<br>- - - - - - 00 | Reserved | REGSEL [R/W]<br>- - 000110 | REGCTR [R/W]<br>- - - 0 - - 00 | Main- Oscillation Standby Control / Main/ Sub Regulator Control |
| $0004D0_H$ to $00063C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C440_H$ | IF2CREQ4 [R/W]<br>00000000 00000001 | | IF2CMSK4 [R/W]<br>00000000 00000000 | | CAN 4<br>IF 2 Register<br><br>**Note:** Not on MB91F465BB/MB91F464 BB |
| $00C444_H$ | IF2MSK24 [R/W]<br>11111111 11111111 | | IF2MSK14 [R/W]<br>11111111 11111111 | | |
| $00C448_H$ | IF2ARB24 [R/W]<br>00000000 00000000 | | IF2ARB14 [R/W]<br>00000000 00000000 | | |
| $00C44C_H$ | IF2MCTR4 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C450_H$ | IF2DTA14 [R/W]<br>00000000 00000000 | | IF2DTA24 [R/W]<br>00000000 00000000 | | |
| $00C454_H$ | IF2DTB14 [R/W]<br>00000000 00000000 | | IF2DTB24 [R/W]<br>00000000 00000000 | | |
| $00C458_H$ to $00C45C_H$ | Reserved | | | | |
| $00C460_H$ | IF2DTA24 [R/W]<br>00000000 00000000 | | IF2DTA14 [R/W]<br>00000000 00000000 | | |
| $00C464_H$ | IF2DTB24 [R/W]<br>00000000 00000000 | | IF2DTB14 [R/W]<br>00000000 00000000 | | |
| $00C468_H$ to $00C47C_H$ | Reserved | | | | |
| $00C480_H$ | TREQR24 [R]<br>00000000 00000000 | | TREQR14 [R]<br>00000000 00000000 | | CAN 4<br>Status Flags<br><br>**Note:** Not on MB91F465BB/MB91F464 BB |
| $00C484_H$ to $00C48C_H$ | Reserved | | | | |
| $00C490_H$ | NEWDT24 [R]<br>00000000 00000000 | | NEWDT14 [R]<br>00000000 00000000 | | |
| $00C494_H$ to $00C49C_H$ | Reserved | | | | |
| $00C4A0_H$ | INTPND24 [R]<br>00000000 00000000 | | INTPND14 [R]<br>00000000 00000000 | | |
| $00C4A4_H$ to $00C4AC_H$ | Reserved | | | | |
| $00C4B0_H$ | MSGVAL24 [R]<br>00000000 00000000 | | MSGVAL14 [R]<br>00000000 00000000 | | |
| $00C4B4_H$ to $00C4FC_H$ | Reserved | | | | |
| $00C500_H$ | CTRLR5 [R/W]<br>00000000 00000001 | | STATR5 [R/W]<br>00000000 00000000 | | CAN 5<br>Control Register<br><br>**Note:** Not on MB91F465BB/MB91F464 BB |
| $00C504_H$ | ERRCNT5 [R]<br>00000000 00000000 | | BTR5 [R/W]<br>00100011 00000001 | | |
| $00C508_H$ | INTR5 [R]<br>00000000 00000000 | | TESTR5 [R/W]<br>00000000 X0000000 | | |
| $00C50C_H$ | BRPE5 [R/W]<br>00000000 00000000 | | CBSYNC5 | | |

# 15. Electrical Characteristics

## 15.1 Absolute Maximum Ratings

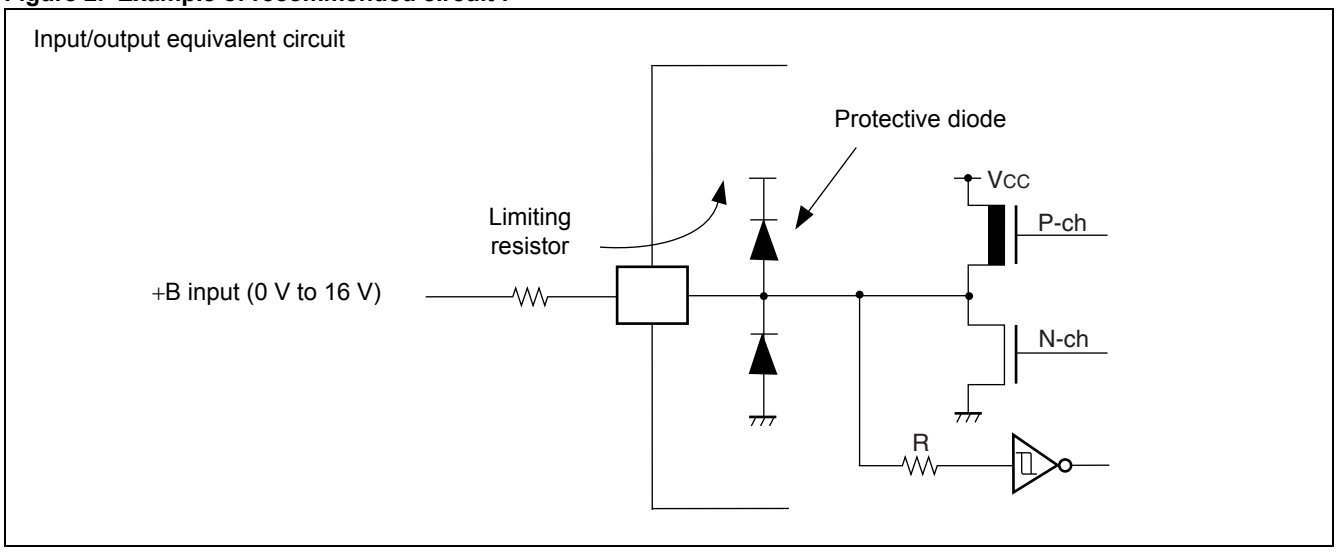
| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply slew rate | – | – | 50 | V/ms | |
| Power supply voltage 1[1] | $V_{DD}5R$ | – 0.3 | + 6.0 | V | |
| Power supply voltage 2[1] | $V_{DD}5$ | – 0.3 | + 6.0 | V | |
| Relationship of the supply voltages | $AV_{CC}5$ | $V_{DD}5$-0.3<br>$V_{DD}35$-0.3 | $V_{DD}5$+0.3<br>$V_{DD}35$+0.3 | V | At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output. |
| | | $V_{SS}5$-0.3<br>$V_{DD}35$-0.3 | $V_{DD}5$+0.3<br>$V_{DD}35$+0.3 | V | All pins of the Ports 26 to 29 (ANn) follow the condition of $V_{IA}$ |
| Analog power supply voltage[1] | $AV_{CC}5$ | – 0.3 | + 6.0 | V | [2] |
| Analog reference power supply voltage[1] | AVRH | – 0.3 | + 6.0 | V | [2] |
| Input voltage 1[1] | $V_{I1}$ | Vss5 – 0.3 | $V_{DD}5$ + 0.3 | V | |
| Analog pin input voltage[1] | $V_{IA}$ | AVss5 – 0.3 | AVcc5 + 0.3 | V | |
| Output voltage 1[1] | $V_{O1}$ | Vss5 – 0.3 | $V_{DD}5$ + 0.3 | V | |
| Maximum clamp current | $I_{CLAMP}$ | – 4.0 | + 4.0 | mA | [3] |
| Total maximum clamp current | $\Sigma \lvert I_{CLAMP} \rvert$ | – | 20 | mA | [3] |
| "L" level maximum output current[4] | $I_{OL}$ | – | 10 | mA | |
| "L" level average output current[5] | $I_{OLAV}$ | – | 8 | mA | |
| "L" level total maximum output current | $\Sigma I_{OL}$ | – | 100 | mA | |
| "L" level total average output current[6] | $\Sigma I_{OLAV}$ | – | 50 | mA | |
| "H" level maximum output current[4] | $I_{OH}$ | – | – 10 | mA | |
| "H" level average output current[5] | $I_{OHAV}$ | – | – 4 | mA | |
| "H" level total maximum output current | $\Sigma I_{OH}$ | – | – 100 | mA | |
| "H" level total average output current[6] | $\Sigma I_{OHAV}$ | – | – 25 | mA | |
| Permitted operating frequency MB91F465BB/F464BB | $f_{max, CLKB}$ | – | 100 | MHz | $T_A \leq 105$ °C |
| | $f_{max, CLKP}$ | – | 50 | | |
| | $f_{max, CLKT}$ | – | 50 | | |
| | $f_{max, CLKCAN}$ | – | 50 | | |
| Permitted operating frequency MB91F465BB/F464BB | $f_{max, CLKB}$ | – | 96 | MHz | $T_A \leq 125$ °C |
| | $f_{max, CLKP}$ | – | 48 | | |
| | $f_{max, CLKT}$ | – | 48 | | |
| | $f_{max, CLKCAN}$ | – | 48 | | |
| Permitted operating frequency MB91F467BA/F466BA | $f_{max, CLKB}$ | – | 96 | MHz | $T_A \leq 105$ °C |
| | $f_{max, CLKP}$ | – | 48 | | |
| | $f_{max, CLKT}$ | – | 48 | | |
| | $f_{max, CLKCAN}$ | – | 48 | | |

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Permitted operating frequency MB91F467BA/F466BA | $f_{max, CLKB}$ | – | 92 | MHz | $T_A \leq 125$ °C |
| | $f_{max, CLKP}$ | – | 46 | | |
| | $f_{max, CLKT}$ | – | 46 | | |
| | $f_{max, CLKCAN}$ | – | 46 | | |
| Permitted power dissipation [7] | $P_D$ | – | 1200 *8 | mW | $T_A \leq 85$ °C |
| | | – | 600 *8 | mW | $T_A \leq 105$ °C |
| | | – | 1300 *8 | mW | $T_A \leq 105$ °C, no Flash program/erase [9] |
| | | – | 1000 *8 | mW | $T_A \leq 115$ °C, no Flash program/erase [9] |
| | | – | 750 *8 | mW | $T_A \leq 125$ °C, no Flash program/erase [9] |
| Operating temperature | $T_A$ | − 40 | + 125 | °C | |
| Storage temperature | Tstg | − 55 | + 150 | °C | |

1. The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.
2. $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.
3.

- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.

**Figure 2. Example of recommended circuit :**



4. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
5. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
6. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.
7. The maximum permitted power dissipation depends onm the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} + I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

8. Worst case value for the QFP package mounted on a 4-layer PCB at specified $T_A$ without air flow.
9. Please contact Fujitsu for reliability limitations when using under these conditions.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 15.6 Flash Memory Program/Erase Characteristics

### 15.6.1 MB91F467BA/466BA

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, $T_A$ = –40 °C to + 105 °C)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.5 | 2.0 | s | Erasure programming time not included |
| Chip erase time | - | n*0.5 | n*2.0 | s | n is the number of Flash sector of the device |
| Word (16-bit width) programming time | - | 6 | 100 | µs | System overhead time not included |
| Program/Erase cycle | 10 000 | | | cycle | |
| Flash data retention time | 20 | | | year | [1] |

1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

### 15.6.2 MB91F465BB/464BB

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, $T_A$ = –40 °C to + 105 °C)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.9 | 3.6 | s | Erasure programming time not included |
| Chip erase time | - | n*0.9 | n*3.6 | s | n is the number of Flash sector of the device |
| Word (16-bit or 32-bit width) programming time | - | 23 | 370 | µs | System overhead time not included |
| Program/Erase cycle | 10 000 | | | cycle | |
| Flash data retention time | 20 | | | year | [1] |

1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

**Figure 4. Internal Clock Mode (Master Mode)**

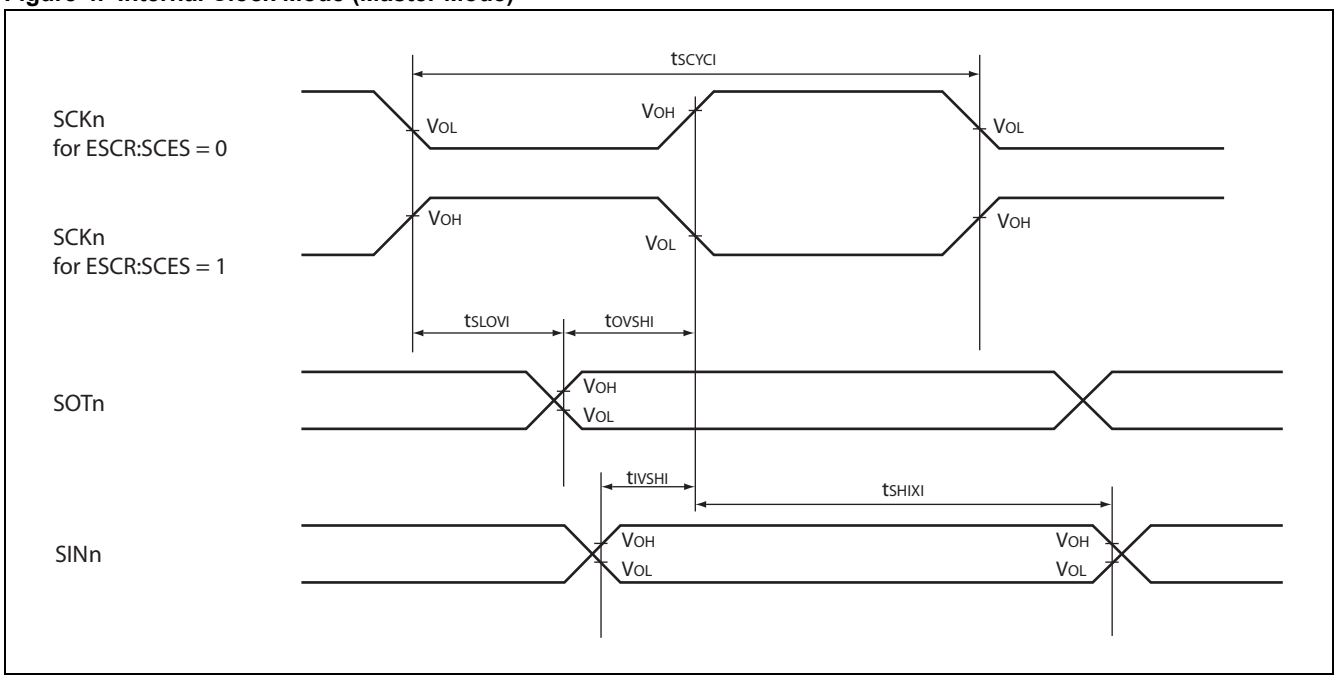
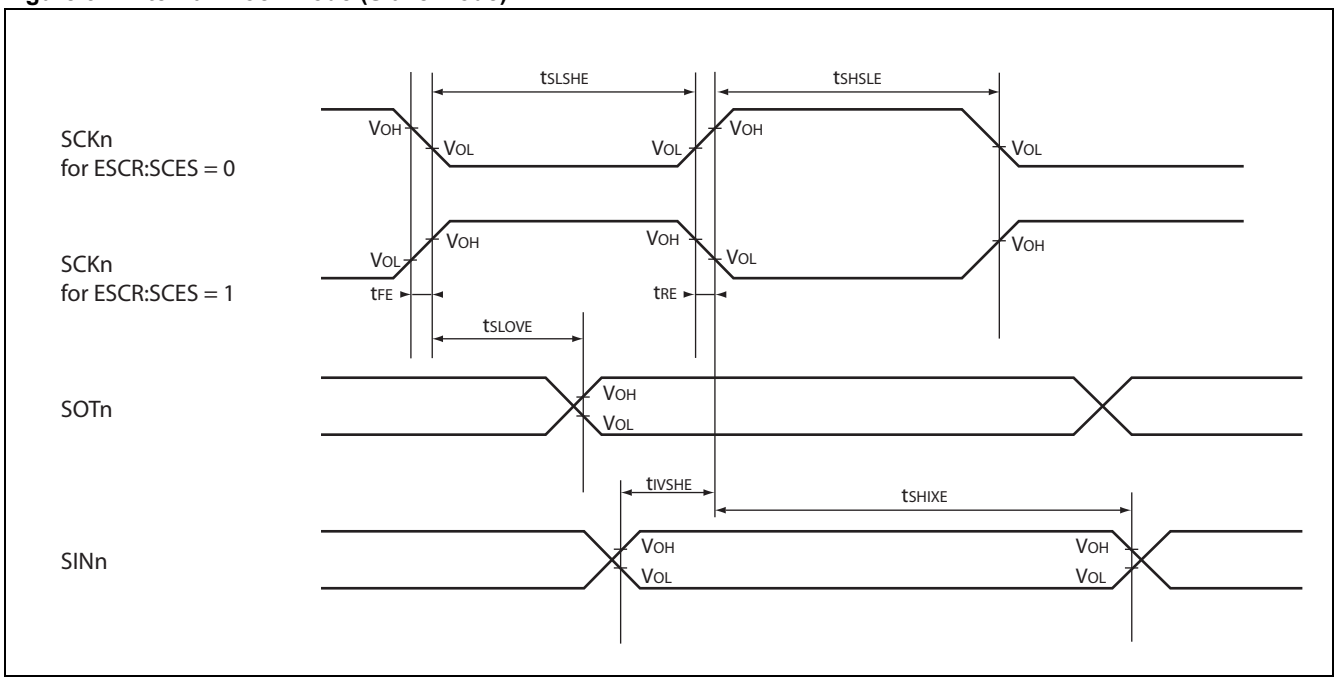



**Figure 5. External Clock Mode (Slave Mode)**



## 15.7.4 I $^2$C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements
All AC tests were measured under the following conditions:
- ❒ -$IO_{drive}$ = 3 mA
- ❒ -$V_{DD}5$ = 3.0 V to 5.5 V, $I_{load}$ = 3 mA
- ❒ -$V_{SS}5$ = 0 V
- ❒ -Ta = - 40 °C to + 125 °C
- ❒ -$C_l$ = 50 pF
- ❒ -VOL = 0.3 × $V_{DD}5$
- ❒ -VOH = 0.7 × $V_{DD}5$
- ❒ -EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

### 15.7.4.1 Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, $T_A$ = –40 °C to + 125 °C)

| Parameter | Symbol | Pin name | Value | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | SCLn | 0 | 400 | kHz | |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | SCLn, SDAn | 0.6 | – | µs | |
| LOW period of the SCL clock | $t_{LOW}$ | SCLn | 1.3 | – | µs | |
| HIGH period of the SCL clock | $t_{HIGH}$ | SCLn | 0.6 | – | µs | |
| Setup time for a repeated START condition | $t_{SU;STA}$ | SCLn, SDAn | 0.6 | – | µs | |
| Data hold time for I$^2$C-bus devices | $t_{HD;DAT}$ | SCLn, SDAn | 0 | 0.9 | µs | |
| Data setup time | $t_{SU;DAT}$ | SCLn SDAn | 100 | – | ns | |
| Rise time of both SDA and SCL signals | $t_r$ | SCLn, SDAn | 20 + 0.1Cb | 300 | ns | |
| Fall time of both SDA and SCL signals | $t_f$ | SCLn, SDAn | 20 + 0.1Cb | 300 | ns | |
| Setup time for STOP condition | $t_{SU;STO}$ | SCLn, SDAn | 0.6 | – | µs | |
| Bus free time between a STOP and START condition | $t_{BUF}$ | SCLn, SDAn | 1.3 | – | µs | |
| Capacitive load for each bus line | $C_b$ | SCLn, SDAn | – | 400 | pF | |
| Pulse width of spike suppressed by input filter | $t_{SP}$ | SCLn, SDAn | 0 | (1..1.5) × $t_{CLKP}$ | ns | [1] |

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I$^2$C signals (SDA, SCL) and peripheral clock.

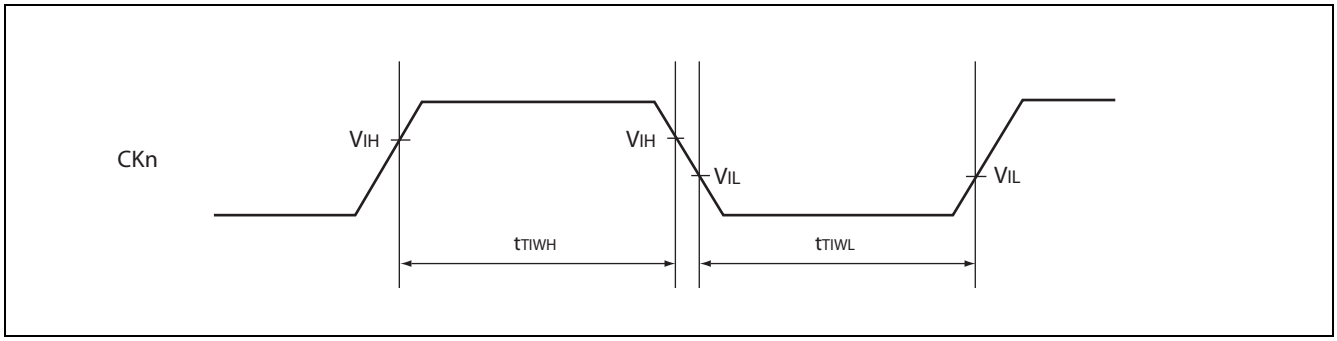
**Note:** $t_{CLKP}$ is the cycle time of the peripheral clock.

### 15.7.5 Free-Run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, $T_A$ = –40 °C to + 125 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | CKn | – | $4t_{CLKP}$ | – | ns |

**Note**: $t_{CLKP}$ is the cycle time of the peripheral clock.

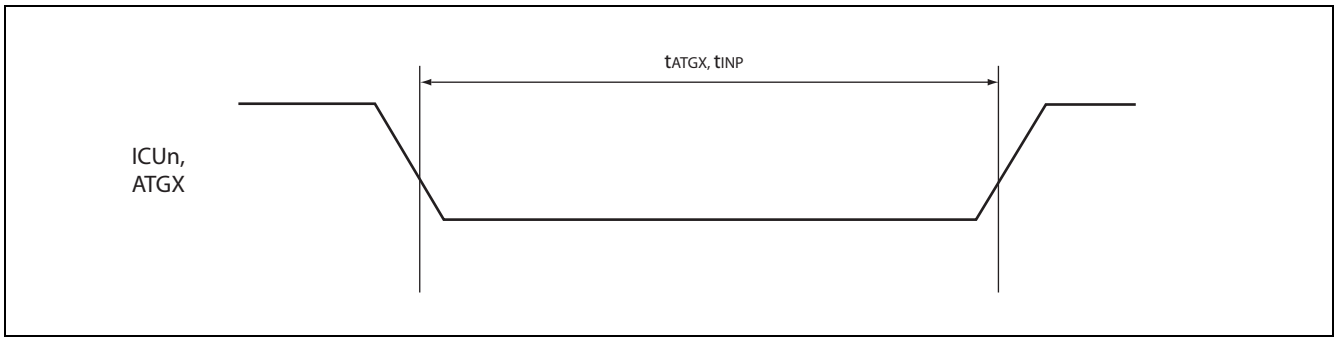



### 15.7.6 Trigger Input Timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, $T_A$ = –40 °C to + 125 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input capture input trigger | $t_{INP}$ | ICUn | – | $5t_{CLKP}$ | – | ns |
| A/D converter trigger | $t_{ATGX}$ | ATGX | – | $5t_{CLKP}$ | – | ns |

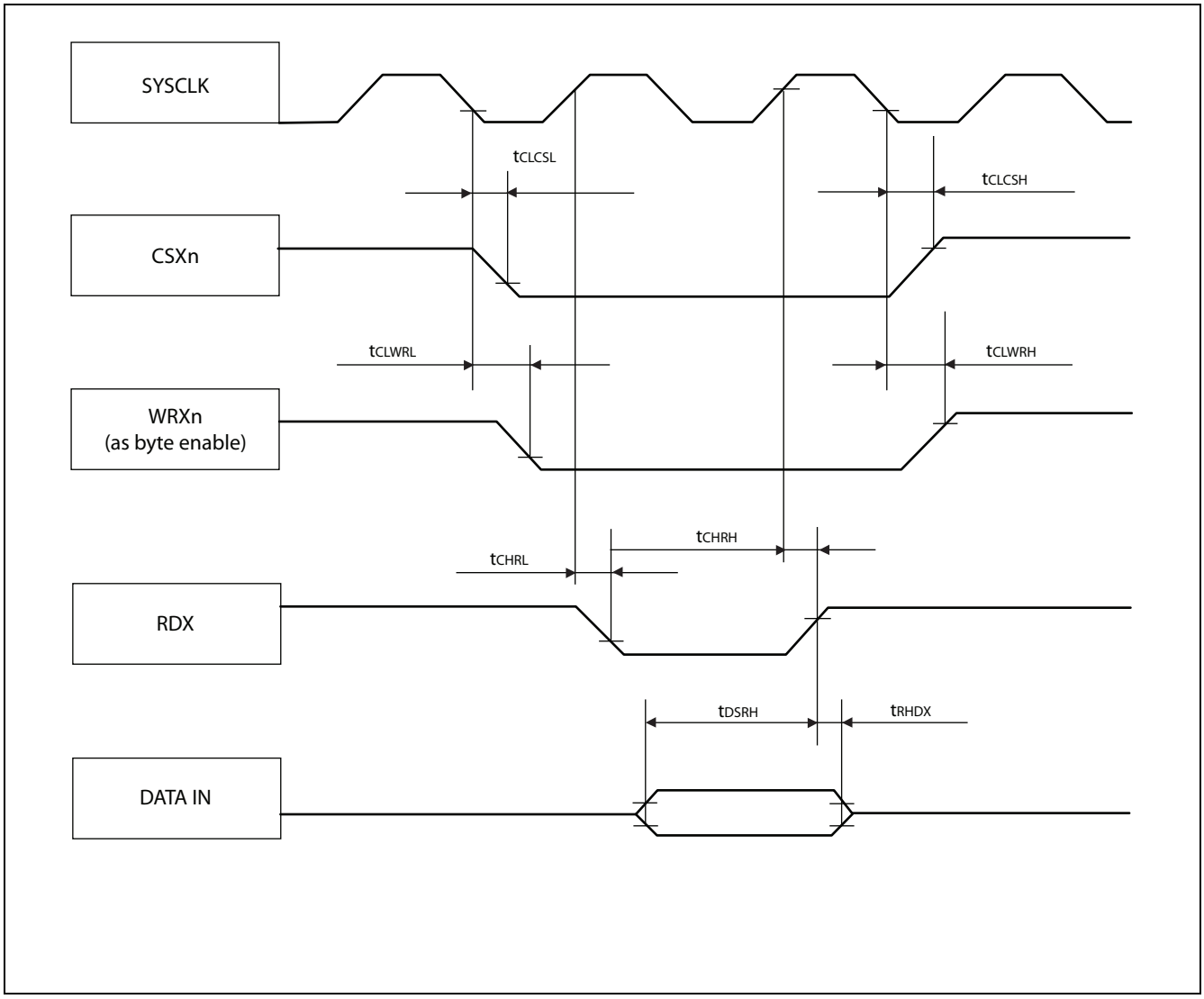
**Note:** $t_{CLKP}$ is the cycle time of the peripheral clock.



### 15.7.7.2 Synchronous/Asynchronous Read Access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A$ = –40 °C to + 125 °C)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| SYSCLK ↑ to RDX delay time | TCHRL | SYSCLK RDX | - 7 | 1 | ns |
| | TCHRH | | - 4 | 2 | ns |
| Data valid to RDX ↑ setup time | TDSRH | RDX D31 to D16 | 33 | - | ns |
| RDX ↑ to Data valid hold time | TRHDX | RDX D31 to D16 | 0 | - | ns |
| SYSCLK ↓ to WRXn (as byte enable) delay time | TCLWRL | SYSCLK WRXn | - | 8 | ns |
| | TCLWRH | | 0 | - | ns |
| SYSCLK ↓ to CSXn delay time | TCLCSL | SYSCLK CSXn | - | 8 | ns |
| | TCLCSH | | - | 12 | ns |



### 15.7.7.4 Asynchronous Write Access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A$ = –40 °C to + 125 °C)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| WRXn ↓ to WRXn ↑ pulse width | TWRLWRH | WRXn | $t_{CLKT}$ | - | ns |
| Data valid to WRXn ↓ setup time | TDSWRL | WRXn D31 to D16 | 1/2 × $t_{CLKT}$ - 10 | - | ns |
| WRXn ↑ to Data valid hold time | TWRHDH | WRXn D31 to D16 | 1/2 × $t_{CLKT}$ - 19 | - | ns |
| WRXn to CSXn delay time | TCLWRL | WRXn CSXn | - | 1/2 × $t_{CLKT}$ | ns |
| | TWRHCH | | 1/2 × $t_{CLKT}$ | - | ns |