Infineon Technologies - MB91F467BAPMC-GSE2-W002 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w002

Contents

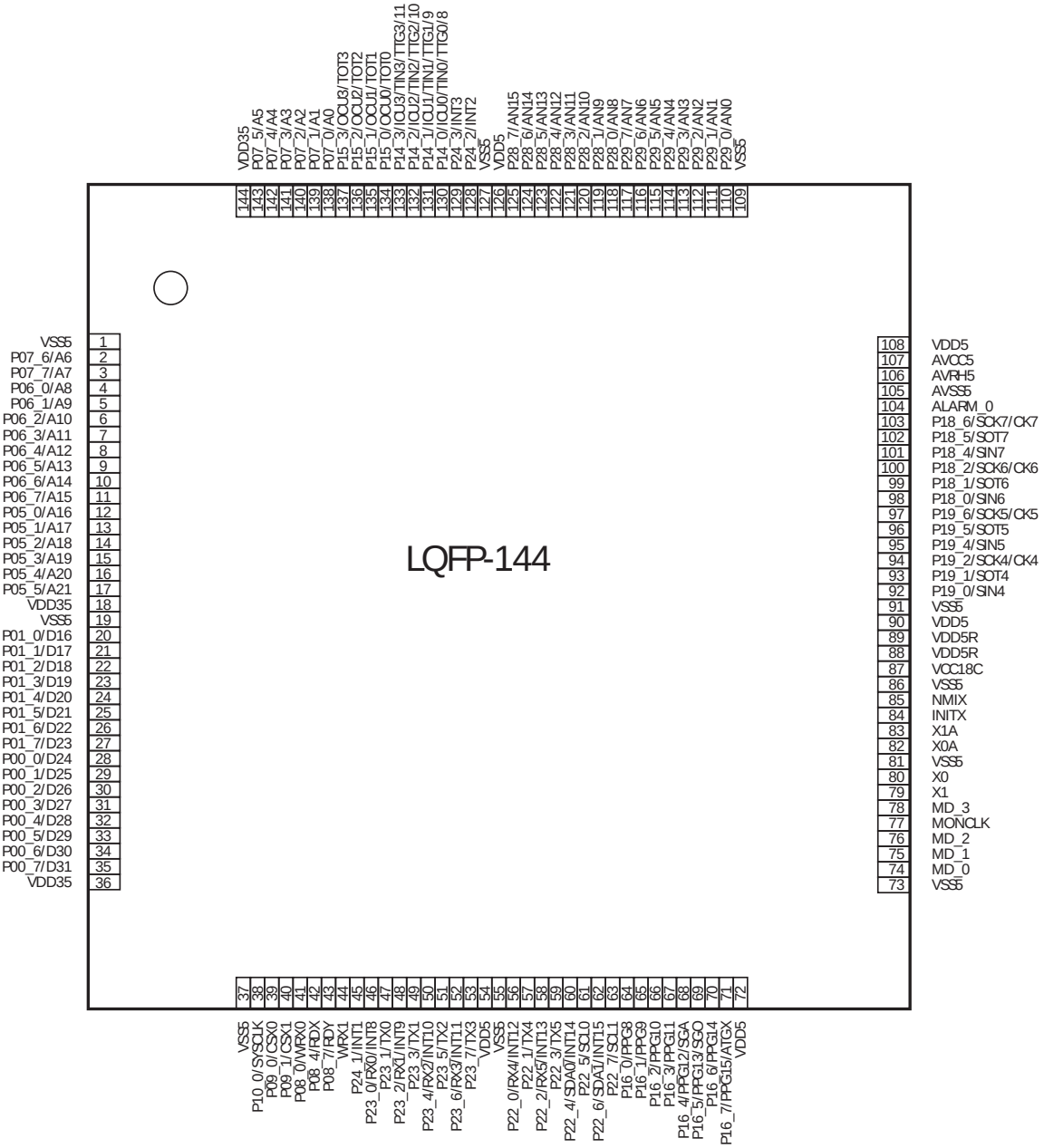
1. Product Lineup

Feature	MB91V460	MB91F465BB/464BB	MB91F467BA/466BA
Max. core frequency (CLKB)	80 MHz	100 MHz	96 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	48 MHz
Max. external bus frequency (CLKT)	40 MHz	50 MHz	48 MHz
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	48 MHz
Technology	0.35µm	0.18µm	0.18µm
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)[1]	MPU (8 ch)[1]	MPU (8 ch)[1]
Flash memory	Emulation SRAM 32bit read data	MB91F465BB: 544 KByte MB91F464BB: 416 KByte	MB91F467BA: 1088 KByte MB91F466BA: 832 KByte
Satellite Flash memory	-	-	-
Flash Protection	-	yes	yes
D-RAM	64 KByte	24 KByte	24 KByte
ID-RAM	64 KByte	16 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch[2]	8 ch[2]
ICU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[3]	MD_3=0: 8 ch MD_3=1: 4 ch[3]
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[4]	MD_3=0: 8 ch MD_3=1: 4 ch[4]
Reload Timer	8 ch	8 ch[5]	8 ch[5]
PPG 16-bit	16 ch	MD_3=0: 16 ch MD_3=1: 8 ch[6]	MD_3=0: 16 ch MD_3=1: 8 ch[6]
PFM 16-bit	1 ch	-	-
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]
C_CAN	6 ch (128msg)	3 ch (32msg)	6 ch (32msg)

2. Pin Assignment

2.1 MB91F467BA/466BA with MD_3=1

(TOP VIEW)



3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466BA			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on Operating in PLL Clock Mode

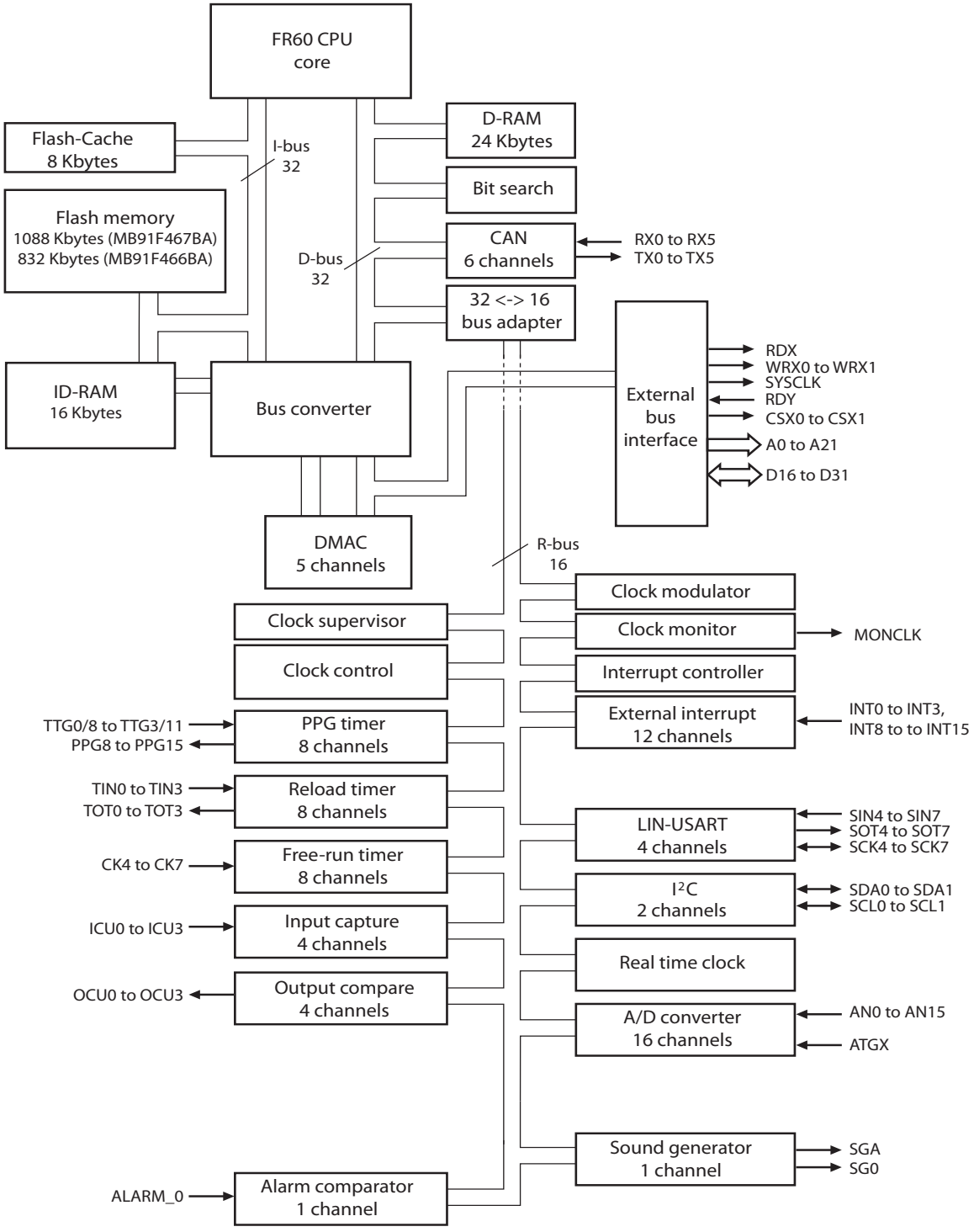
If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

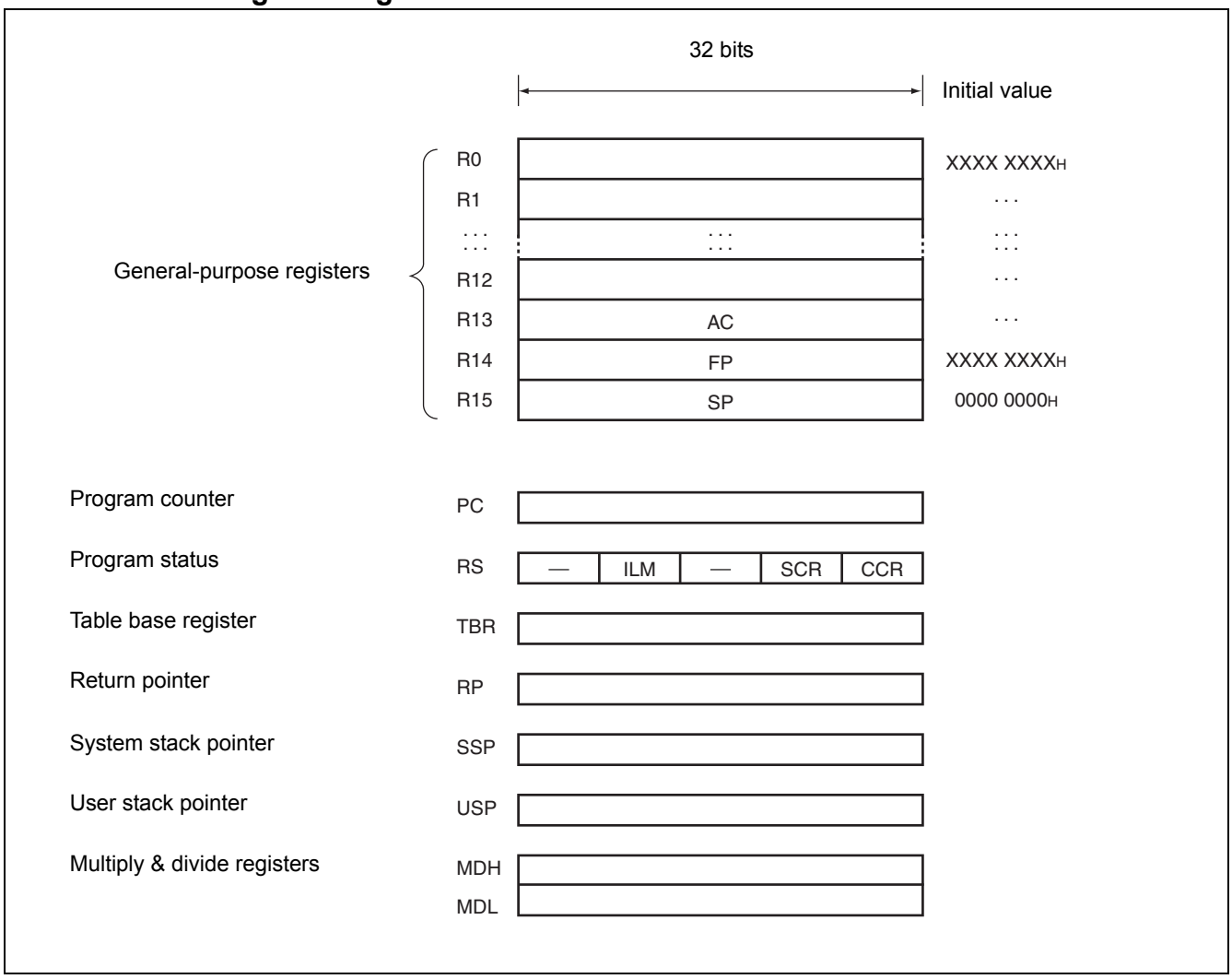
7. Block Diagram

7.1 MB91F467BA/466BA with MD_3=1



8.3 Programming Model

8.3.1 Basic Programming Model



9. Embedded Program/Data Memory (Flash)

9.1 Flash features

- MB91F467BA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.5 Mbits)
- MB91F466BA: 832 Kbytes (12 × 64 Kbytes + 8 × 8 Kbytes = 6.5 Mbits)
- MB91F465BB: 544 Kbytes (8 × 64 Kbytes + 4 × 8 Kbytes = 4.25 Mbits)
- MB91F464BB: 416 Kbytes (6 × 64 Kbytes + 4 × 8 Kbytes = 3.25 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes

9.2.1 64-bit CPU mode (available on MB91F467BA/466BA only) :

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

9.2.2 32-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

9.2.3 16-bit CPU mode:

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in word (16-bit) length units.

9.2.4 Flash Memory Mode (External Access to Flash Memory Enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3.1.3 Flash Memory Map MB91F465BB

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
Legend	Memory not available in this area				Memory available in this area				

9.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TCE xternal pins	FR-CPU mode	MB91F467BA/466BA/F465BB/F464BB External Pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to ‘1’
-	-	MD1	MD1	75	Set to ‘1’
-	-	MD0	MD0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to ‘H’	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to ‘0’
-		EQIN	GP18_5	102	Set to ‘0’
-		TESTX	GP16_5	69	Set to ‘1’
-		RDYI	GP18_4	101	Set to ‘0’
A-1	Internal address bus	FA0	GP05_5	17	Set to ‘0’
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A18		FA17 to FA19	GP05_0 to GP05_2	12 to 14	
A19		FA20	GP05_3	15	See note [1]
-		FA21	GP05_4	16	See note [2]
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

1. A19 is used as address bit on MB91F467BA/F466BA. For MB91F465BB/F464BB, set this pin to ‘1’.
2. For MB91F467BA/F466BA, set this pin to ‘1’. For MB91F465BB/F464BB, this pin can be left open.

9.6.2.2 FSV1 (bit15 to bit0) MB91F467BA/466BA

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 3. Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to “0”	set to “1”	
FSV1[1]	SA1	set to “0”	set to “1”	
FSV1[2]	SA2	set to “0”	set to “1”	
FSV1[3]	SA3	set to “0”	set to “1”	
FSV1[4]	SA4	set to “0”	–	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[15:8]	–	–	–	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing. See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.2.3 FSV1 (bit15 to bit0) MB91F465BB/464BB

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

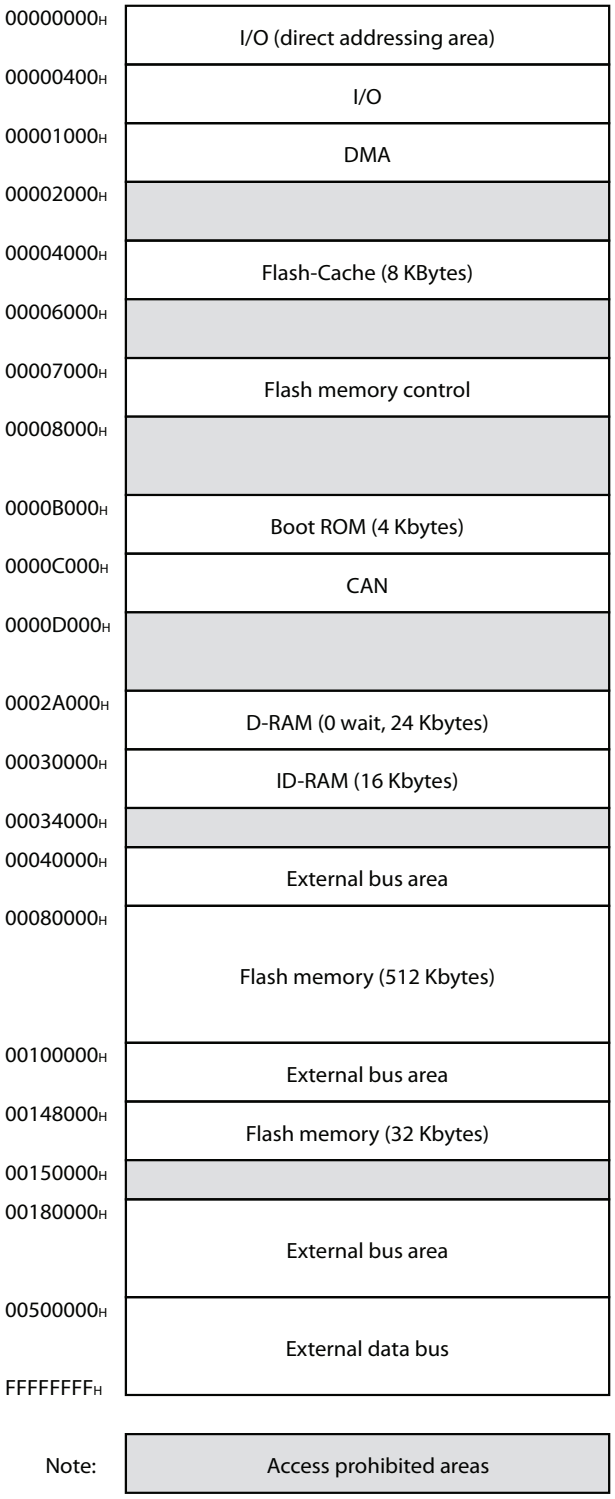
Table 4. Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[3:0]	–	–	–	not available
FSV1[4]	SA4	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[15:8]	–	–	–	not available

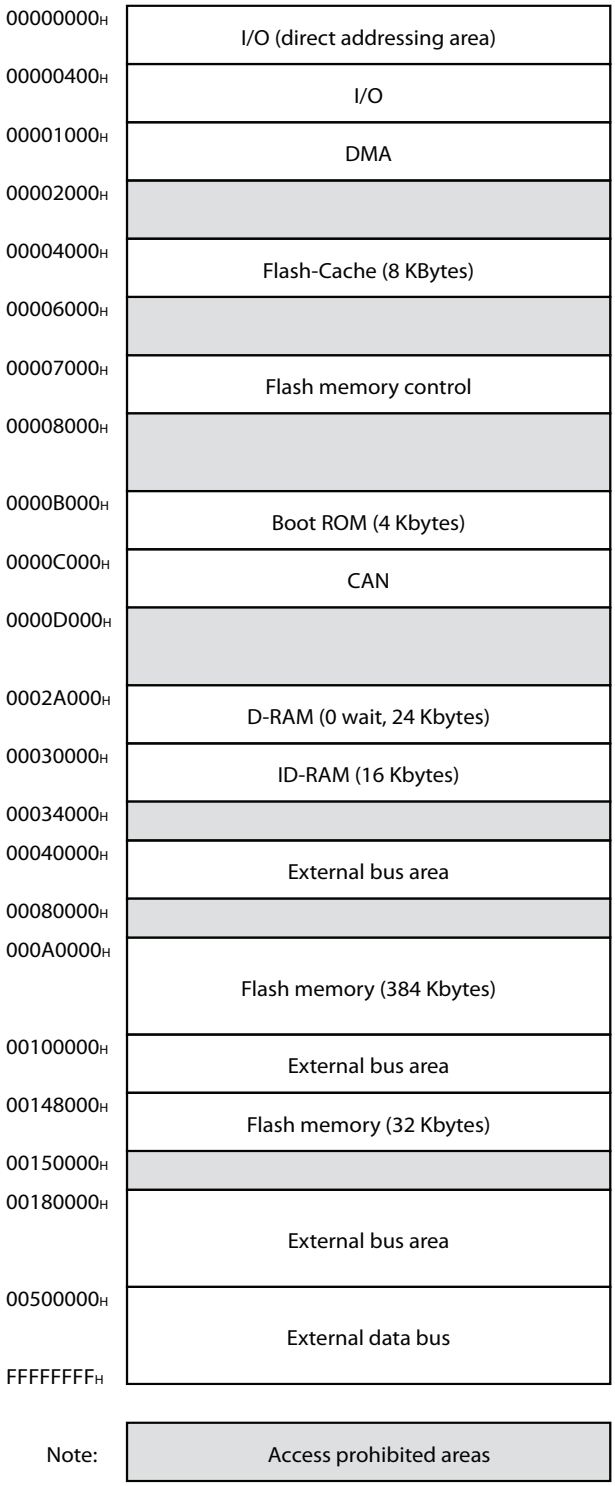
Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing. See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

11.2 MB91F465BB, MB91F464BB

MB91F465BB



MB91F464BB



Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004_H	Reserved	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	Reserved	
$00000C_H$	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020_H to $00002C_H$	Reserved				
000030_H	EIRR0 [R/W] MB91F467BA: 00000000:MD3=0 11110000:MD3=1 MB91F465BB: XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034_H	EIRR1 [R/W] MB91F467BA: 00000000 MB91F465BB: XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC		Delay interrupt
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048_H $00004C_H$	Reserved				Reserved
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000[2]		External Bus Unit
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
$00067C_H$	Reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** [3]	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H to $0007F8_H$	Reserved				External Bus Unit
$0007FC_H$	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800_H to $000CFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $003FFC_H$	Reserved				Reserved
002000_H to $006FFC_H$	Flash-cache size is 8 Kbytes : 004000_H to $005FFC_H$				Flash-cache / I-RAM area
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7

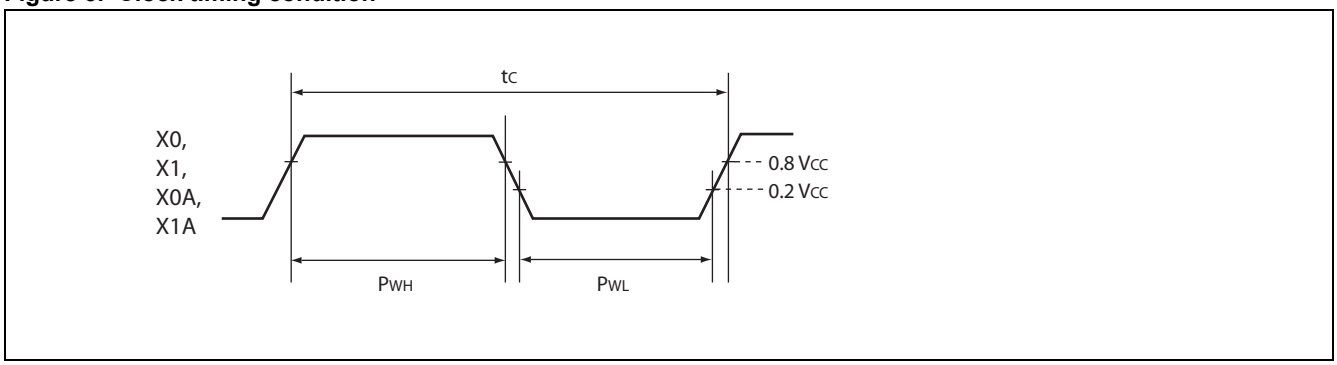
15.7 AC Characteristics

15.7.1 Clock Timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

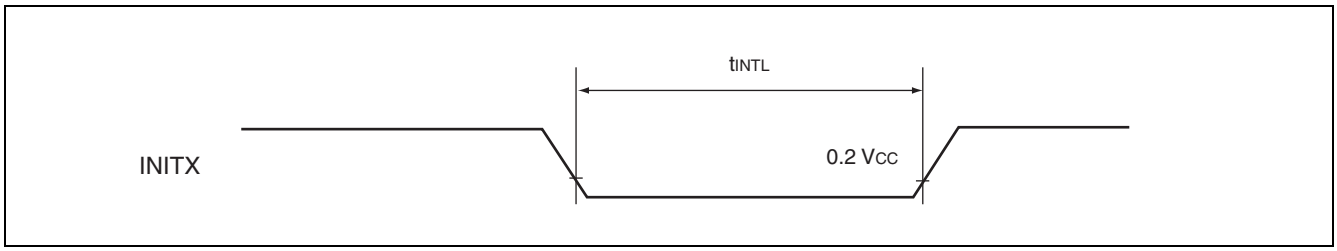
Figure 3. Clock timing condition



15.7.2 Reset Input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	–	8	–	ms
INITX input time (other than the above)				20	–	µs



15.7.7 External Bus AC Timings at $V_{DD}35$ = 3.0 to 5.5 V

Note: This chapter is applicable to MB91F467BA/F466BA

■ Conditions during AC measurements
All AC tests were measured under the following conditions:

- -IO_{drive} = 5 mA
- -$V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 3 mA
- -$V_{SS}5$ = 0 V
- -Ta = − 40 °C to + 125 °C
- -C_l = 50 pF
- -VOL = 0.5 × $V_{DD}35$
- -VOH = 0.5 × $V_{DD}35$
- -EPILR = 0, PILR = 1 (Automotive Level = worst case)

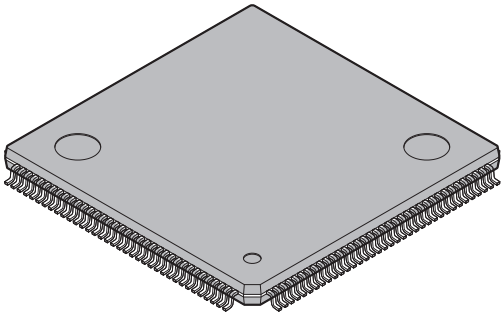
15.7.7.1 Basic Timing

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

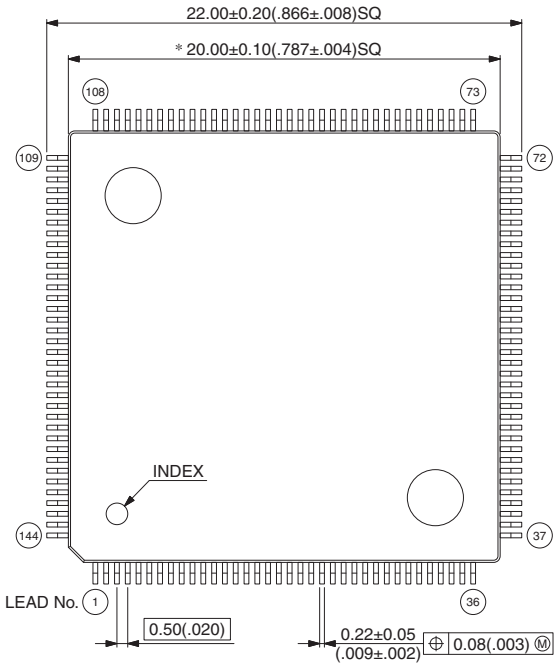
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 x t_{CLKT} - 1	1/2 × t_{CLKT} + 9	ns
	t_{CHCL}		1/2 × t_{CLKT} - 9	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	-	8	ns
	t_{CLCSH}		-	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	-	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

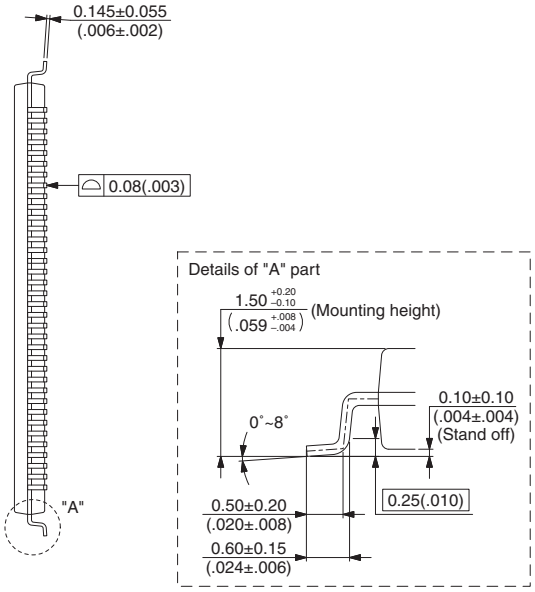
17. Package Dimension

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Document History

Document Title: MB91F467BA/466BA, MB91F465BB/464BB, FR60 MB91460B Series, 32-bit Microcontroller Datasheet Document Number: 002-04608				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/17/2009	Migrated to Cypress and assigned document number 002-04608. No change to document contents or format.
*A	5221423	AKIH	04/25/2016	Updated to Cypress template