Infineon Technologies - MB91F467BAPMC-GSE2-W003 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w003

3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

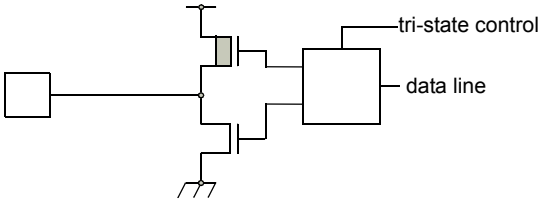
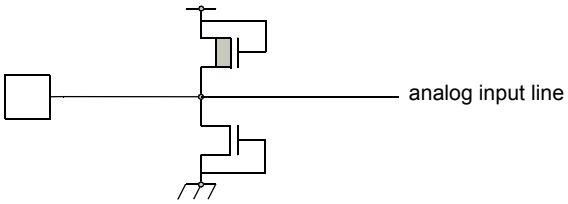
Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466BA			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
48	P23_2	I/O	A	General-purpose input/output port
	RX1			RX input pin of CAN1
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port
	TX1			TX output pin of CAN1
50	P23_4	I/O	A	General-purpose input/output port
	RX2			RX input pin of CAN2
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
	TX2			TX output pin of CAN2
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
	MB91F467BA/MB91F466BA: RX3			RX input pin of CAN3
53	P23_7	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX3			TX output pin of CAN3
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
	MB91F467BA/MB91F466BA: RX4			RX input pin of CAN4
57	P22_1	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX4			TX output pin of CAN4
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
	MB91F467BA/MB91F466BA: RX5			RX input pin of CAN5
59	P22_3	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX5			TX output pin of CAN5
60	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output port
	SDA1			I^2C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output port
	SCL1			I^2C bus clock input/output pin (open drain)

3.1.1 Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
60	P22_4	I/O	C	General-purpose input/output ports
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output ports
	SCL0			I^2C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output ports
	SDA1			I^2C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output ports
	SCL1			I^2C bus clock input/output pin (open drain)
64 to 67	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SG0 output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pins
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

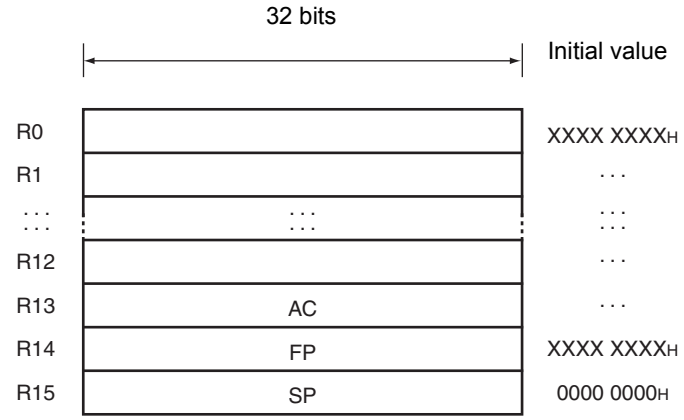
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

8.4 Registers

8.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

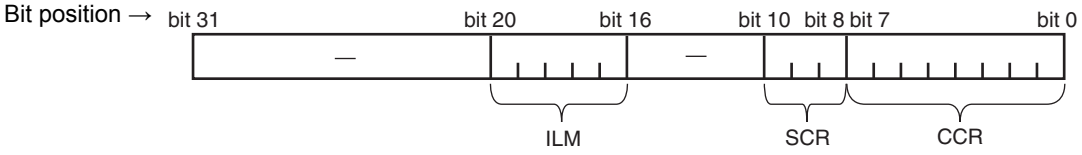
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

Legend	Memory not available in this area	Memory available in this area

9.3.3.3 Address Mapping MB91F465BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
08:0000h to 0F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
08:0000h to 0F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

9.3.3.4 Address Mapping MB91F464BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

9.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

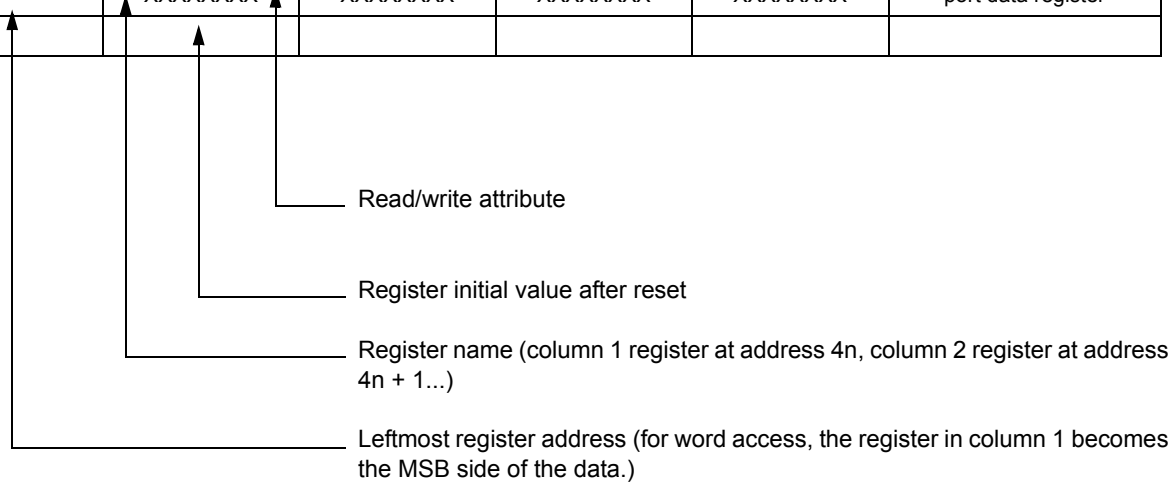
MBM29LV400TCE xternal pins	FR-CPU mode	MB91F467BA/466BA/F465BB/F464BB External Pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to ‘1’
-	-	MD1	MD1	75	Set to ‘1’
-	-	MD0	MD0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to ‘H’	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to ‘0’
-		EQIN	GP18_5	102	Set to ‘0’
-		TESTX	GP16_5	69	Set to ‘1’
-		RDYI	GP18_4	101	Set to ‘0’
A-1	Internal address bus	FA0	GP05_5	17	Set to ‘0’
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A18		FA17 to FA19	GP05_0 to GP05_2	12 to 14	
A19		FA20	GP05_3	15	See note [1]
-		FA21	GP05_4	16	See note [2]
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

1. A19 is used as address bit on MB91F467BA/F466BA. For MB91F465BB/F464BB, set this pin to ‘1’.
2. For MB91F467BA/F466BA, set this pin to ‘1’. For MB91F465BB/F464BB, this pin can be left open.

12. I/O Map

12.1 MB91F467BA/466BA, MB91F465BB/464BB

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$ to $000D3C_H$	Reserved				
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - -0	Reserved	
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D7C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
$000E44_H$	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - - 00	PILR10 [R/W] - - - - - - - 0	Reserved	
$000E4C_H$	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
$000E58_H$	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
$000E60_H$ to $000E7C_H$	Reserved				Reserved
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
$000E84_H$	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 0 - - 0- - - 0	EPILR09 [R/W] - - - - - - 00	EPILR10 [R/W] - - - - - - - 0	Reserved	
$000E8C_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EBC_H$	Reserved				Reserved

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) [5]	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception [5]	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
I^2C 0	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	—
I^2C 1	75	4B			$2D0_H$	$000FFED0_H$	—
Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
Reserved	89	59			298_H	$000FFE98_H$	77
Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Output Compare 5	105	69			258_H	$000FFE58_H$	93
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Output Compare 7	107	6B			250_H	$000FFE50_H$	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	—
Reserved	109	6D			248_H	$000FFE48_H$	—
System Reserved	110	6E	ICR47 [3]	$46F_H$	244_H	$000FFE44_H$	—
System Reserved	111	6F			240_H	$000FFE40_H$	—
PPG 0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG 1	113	71			238_H	$000FFE38_H$	97

14. Recommended Settings

14.1 PLL and Clock Gear Settings

Please note that for MB91F467BA/466BA and MB91F465BB/464BB the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Table 7. Recommended PLL divider and clock gear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	Not on MB91F467BA/466BA
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	64	47.6	97.6 Not on MB91F467BA/466BA
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9 Not on MB91F467BA/466BA
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8

15.7.7 External Bus AC Timings at $V_{DD}35$ = 3.0 to 5.5 V

Note: This chapter is applicable to MB91F467BA/F466BA

■ Conditions during AC measurements
All AC tests were measured under the following conditions:

- -IO_{drive} = 5 mA
- -$V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 3 mA
- -$V_{SS}5$ = 0 V
- -Ta = − 40 °C to + 125 °C
- -C_l = 50 pF
- -VOL = 0.5 × $V_{DD}35$
- -VOH = 0.5 × $V_{DD}35$
- -EPILR = 0, PILR = 1 (Automotive Level = worst case)

15.7.7.1 Basic Timing

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 x t_{CLKT} - 1	1/2 × t_{CLKT} + 9	ns
	t_{CHCL}		1/2 × t_{CLKT} - 9	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	-	8	ns
	t_{CLCSH}		-	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	-	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

18. Revision History

Spansion Publication Number: DS07-16609-1E

Version	Date	Remark
2.0	2008-06-19	Initial version
2.1	2008-08-15	Proof reading results from FJ incorporated; Corrected pinout drawings; IO CIRCUIT TYPES: corrected some typos like on the other datasheets; HANDLING DEVICES: updated the section "Notes on PS register" for better understanding; Interrupt Vector Table: corrected the footnotes FLASH: added note about the operation mode switching capability in Boot ROM; corrected flash security vector FSV2 assignments, corrected section about parallel programming, corrected section pin connections in parallel programming mode so that there is only one page added section "Poweron Sequence in parallel programming mode"; ELECTRICAL CHARACTERISTICS: removed the note that analog input/output pins cannot accept +B signal input; splitted I_{LV} into external and internal LV detection current ADC Characteristics: Corrected the items about nonlinearity error; Corrected the company name
3.0	2009-01-09	Page 1: Corrected document name field in top header Block Diagram: Removed SCK0 (LIN-USART0 is asynchronous only) Added Ta=125C characteristics

19. Main Changes in this Edition

Page	Section	Change Results
104	15. Electrical Characteristics 15.4. A/D converter characteristics	Corrected the column “Value” and “Unit” of the parameter “Zero reading voltage” and “Full scale reading voltage”. (Value : AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB Unit : LSB → V)

NOTE: Please see “Document History” for later revised information.

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