Infineon Technologies - MB91F467BAPMC-GSE2-W005 Datasheet

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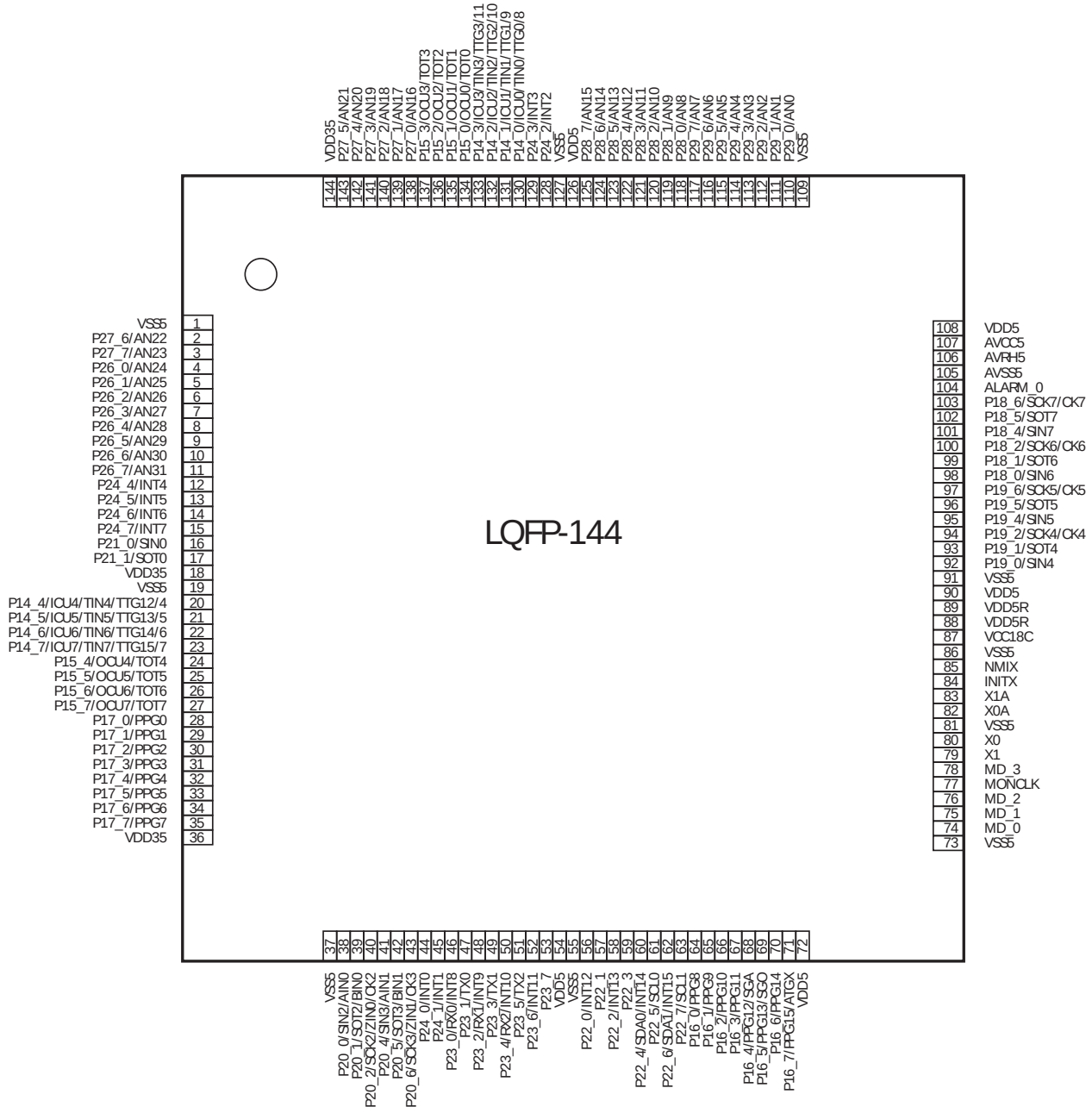
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w005

2.4 MB91F465BB/464BB with MD_3=0

(TOP VIEW)



3.2 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
44	P24_0	I/O	A	General-purpose input/output ports
	INT0			External interrupt input pin
45	P24_1	I/O	A	General-purpose input/output ports
	INT1			External interrupt input pin
46	P23_0	I/O	A	General-purpose input/output ports
	RX0			RX input pin of CAN0
	INT8			External interrupt input pin
47	P23_1	I/O	A	General-purpose input/output ports
	TX0			TX output pin of CAN0
48	P23_2	I/O	A	General-purpose input/output ports
	RX1			RX input pin of CAN1
	INT9			External interrupt input pin
49	P23_3	I/O	A	General-purpose input/output ports
	TX1			TX output pin of CAN1
50	P23_4	I/O	A	General-purpose input/output ports
	RX2			RX input pin of CAN2
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output ports
	TX2			TX output pin of CAN2
52	P23_6	I/O	A	General-purpose input/output ports
	MB91F467BA/ MB91F466BA: RX3			RX input pin of CAN3
	INT11			External interrupt input pin
53	P23_7 MB91F467BA/ MB91F466BA: TX3	I/O	A	General-purpose input/output ports
				TX output pin of CAN3
56	P22_0	I/O	A	General-purpose input/output port
	MB91F467BA/ MB91F466BA: RX4			RX input pin of CAN4
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
	MB91F467BA/ MB91F466BA: TX4			TX output pin of CAN4
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
	MB91F467BA/ MB91F466BA: RX5			RX input pin of CAN5
59	P22_3	I/O	A	General-purpose input/output port
	MB91F467BA/ MB91F466BA: TX5			TX output pin of CAN5

9.3 Flash Access in CPU mode

9.3.1 Flash Configuration

9.3.1.1 Flash Memory Map MB91F467BA

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

Address	Register				Block
	+0	+1	+2	+3	
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 00 - - 0000	Reserved			
000244_H to $0002CC_H$	Reserved				Reserved
$0002D0_H$	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		OCS67 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 4 to 7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ to $0002EC_H$	Reserved				Reserved
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4, OCU 5)
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6, OCU 7)

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $003FFC_H$	Reserved				Reserved
002000_H to $006FFC_H$	Flash-cache size is 8 Kbytes : 004000_H to $005FFC_H$				Flash-cache / I-RAM area
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

Address	Register				Block
	+0	+1	+2	+3	
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved		Reserved		
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved		Reserved		
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved		Reserved		
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved		Reserved		
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$ to $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$ to $00C13C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C210_H$	IF1CREQ2 [R/W] 00000000 00000001		IF1CMSK2 [R/W] 00000000 00000000		CAN 2 IF 1 Register
$00C214_H$	IF1MSK22 [R/W] 11111111 11111111		IF1MSK12 [R/W] 11111111 11111111		
$00C218_H$	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
$00C21C_H$	IF1MCTR2 [R/W] 00000000 00000000		Reserved		
$00C220_H$	IF1DTA12 [R/W] 00000000 00000000		IF1DTA22 [R/W] 00000000 00000000		
$00C224_H$	IF1DTB12 [R/W] 00000000 00000000		IF1DTB22 [R/W] 00000000 00000000		
$00C228_H$ to $00C22C_H$	Reserved				
$00C230_H$	IF1DTA22 [R/W] 00000000 00000000		IF1DTA12 [R/W] 00000000 00000000		
$00C234_H$	IF1DTB22 [R/W] 00000000 00000000		IF1DTB12 [R/W] 00000000 00000000		
$00C238_H$ to $00C23C_H$	Reserved				
$00C240_H$	IF2CREQ2 [R/W] 00000000 00000001		IF2CMSK2 [R/W] 00000000 00000000		CAN 2 IF 2 Register
$00C244_H$	IF2MSK22 [R/W] 11111111 11111111		IF2MSK12 [R/W] 11111111 11111111		
$00C248_H$	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
$00C24C_H$	IF2MCTR2 [R/W] 00000000 00000000		Reserved		
$00C250_H$	IF2DTA12 [R/W] 00000000 00000000		IF2DTA22 [R/W] 00000000 00000000		
$00C254_H$	IF2DTB12 [R/W] 00000000 00000000		IF2DTB22 [R/W] 00000000 00000000		
$00C258_H$ to $00C25C_H$	Reserved				
$00C260_H$	IF2DTA22 [R/W] 00000000 00000000		IF2DTA12 [R/W] 00000000 00000000		
$00C264_H$	IF2DTB22 [R/W] 00000000 00000000		IF2DTB12 [R/W] 00000000 00000000		
$00C268_H$ to $00C27C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $01FFFC_H$	Reserved				EDSU / MPU
020000_H to $02FFFC_H$	D-RAM size is 24 Kbytes : $02A000_H$ - $02FFFC_H$ (data access is 0 wait cycles)				D-RAM area
030000_H to $03FFFC_H$	ID-RAM size is 16 Kbytes : 030000_H - $033FFC_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

1. depends on the number of available CAN channels

2. ACR0 [11 : 10] depends on Mode vector fetch information on bus width

3. TCR [3 : 0] INIT value = 0000, keeps value after RST

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000_H to $1BFFF8_H$	External Bus Area								ROMS8
$1C0000_H$ to $1FFFF8_H$									ROMS9
200000_H to $27FFF8_H$									ROMS10
280000_H to $2FFFF8_H$									ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Notes: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read. On MB91F465BB/F464BB, write access to the flash is only possible in 16-bit mode.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) [5]	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception [5]	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35

15.3 DC Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	CMOS hysteresis input
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	-	V_{DD} + 0.3	V	4.5 V ? V_{DD} ? 5.5 V
				0.74 × V_{DD}	-	V_{DD} + 0.3	V	3 V ? V_{DD} < 4.5 V
		-	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	
		-	Port inputs if TTL input is selected	2.0	-	V_{DD} + 0.3	V	
	V_{IHR}	INITX	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	-	V_{DD} - 0.3	-	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	-	2.5	-	V_{DD} + 0.3	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	-	0.2 × V_{DD}	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	-	0.3 × V_{DD}	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	-	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} - 0.3	-	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		-	Port inputs if TTL input is selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILR}	INITX	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	-	V_{SS} - 0.3	-	0.5	V	External clock in "Oscillation mode"

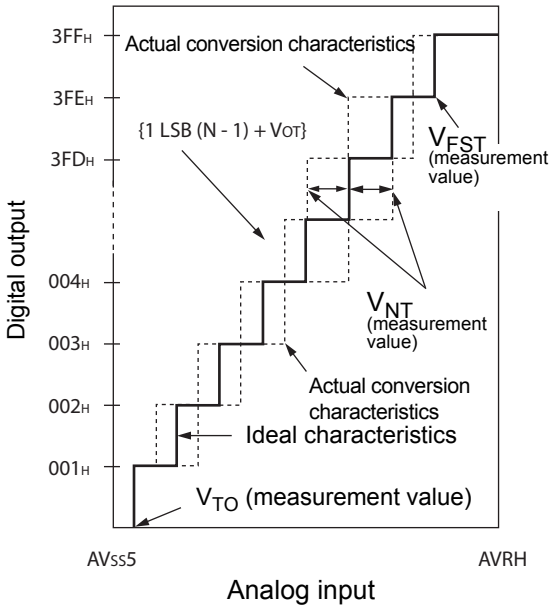
15.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

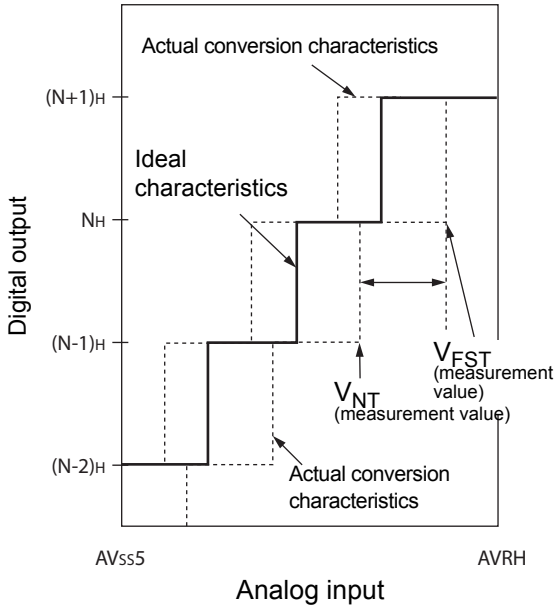
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	– 3	–	+ 3	LSB	
Nonlinearity error	–	–	– 2.5	–	+ 2.5	LSB	
Differential nonlinearity error	–	–	– 1.9	–	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	–	0.6	–	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	–	0.4	–	–	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	–	1.0	–	–	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	–	–	11	pF	
Input resistance	R_{IN}	ANn	–	–	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			–	–	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	– 1	–	+ 1	µA	T_A = + 25 °C
			– 3	–	+ 3	µA	T_A = + 125 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	–	AVRH	V	
Offset between input channels	–	ANn	–	–	4	LSB	

Note: The accuracy gets worse as AVRH - AVRL becomes smaller

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value
V_{OT}: Voltage at which the digital output changes from 000_H to 001_H.
V_{FST}: Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

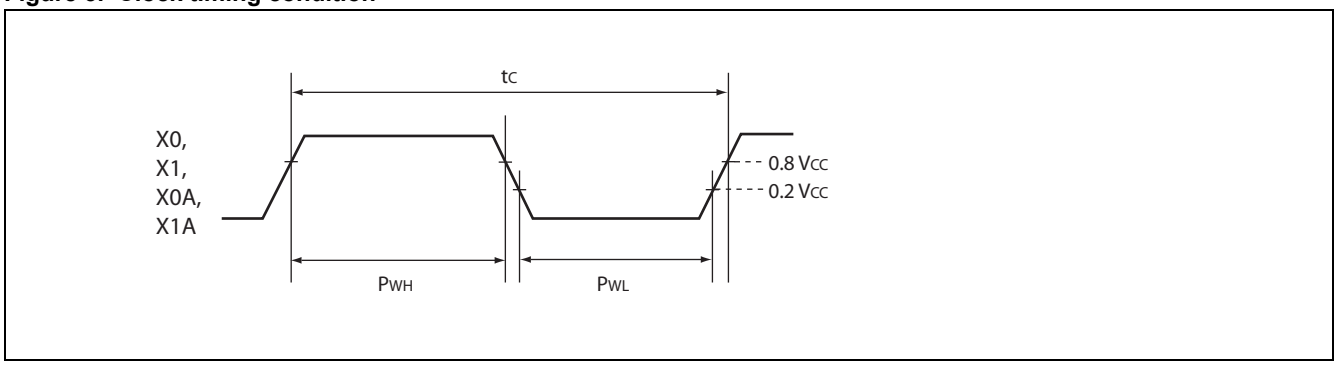
15.7 AC Characteristics

15.7.1 Clock Timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

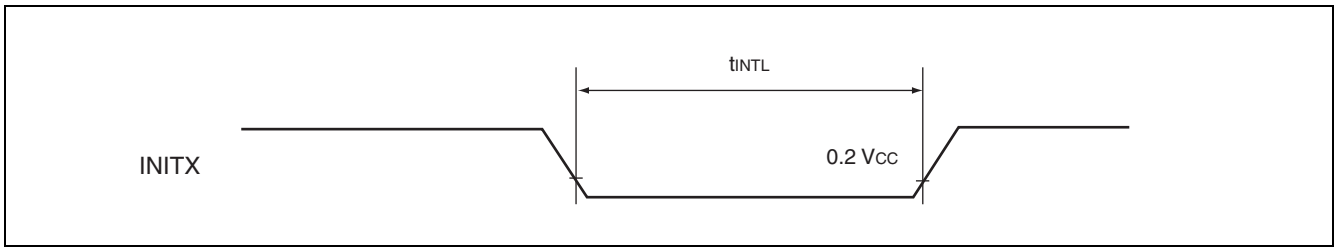
Figure 3. Clock timing condition



15.7.2 Reset Input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	–	8	–	ms
INITX input time (other than the above)				20	–	µs



15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:

- ❒ - IO_{drive} = 5 mA
- ❒ - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ - $V_{SS}5$ = 0 V
- ❒ - T_a = -40 °C to +125× °C
- ❒ - C_l = 50 pF (load capacity value of pins when testing)
- ❒ - VOL = 0.2 x $V_{DD}5$
- ❒ - VOH = 0.8 x $V_{DD}5$
- ❒ - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	-	4 t_{CLKP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		- 30	30	- 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} - 30[1]	-	m × t_{CLKP} - 20[1]	-	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	-	t_{CLKP} + 45	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	-	0	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
Serial clock“L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		-	2 t_{CLKP} + 55	-	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	-	10	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK rising time	t_{FE}	SCKn		-	20	-	20	ns
SCK falling time	t_{RE}	SCKn		-	20	-	20	ns

1. Parameter m depends on t_{SCYCI} and can be calculated as :

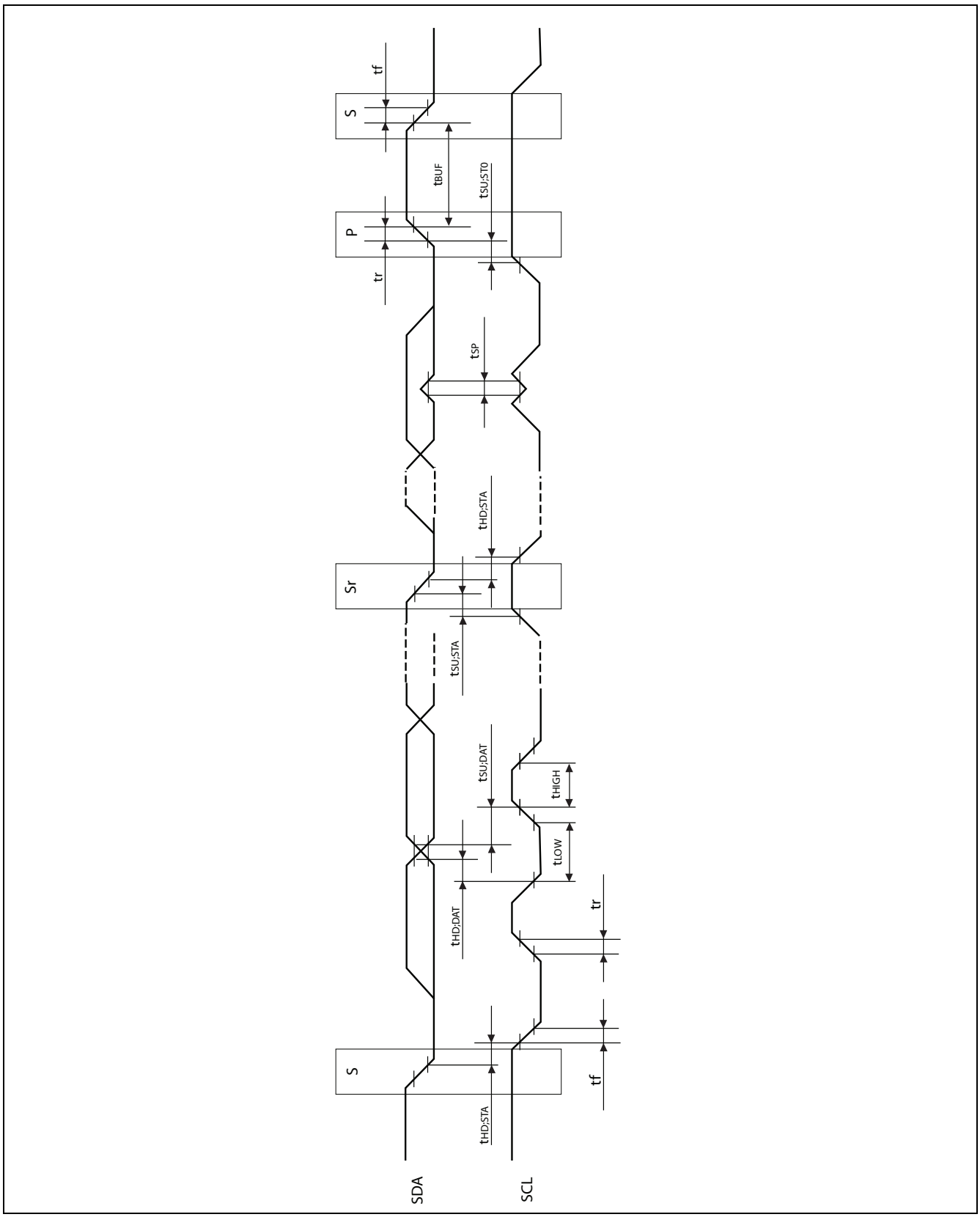
■ if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2

■ if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :

■ The above values are AC characteristics for CLK synchronous mode.

■ t_{CLKP} is the cycle time of the peripheral clock.


tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
tf
S
tHD;STA
SDA
SCL

15.7.7 External Bus AC Timings at $V_{DD}35$ = 3.0 to 5.5 V

Note: This chapter is applicable to MB91F467BA/F466BA

■ Conditions during AC measurements
All AC tests were measured under the following conditions:

- -IO_{drive} = 5 mA
- -$V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 3 mA
- -$V_{SS}5$ = 0 V
- -Ta = − 40 °C to + 125 °C
- -C_l = 50 pF
- -VOL = 0.5 × $V_{DD}35$
- -VOH = 0.5 × $V_{DD}35$
- -EPILR = 0, PILR = 1 (Automotive Level = worst case)

15.7.7.1 Basic Timing

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

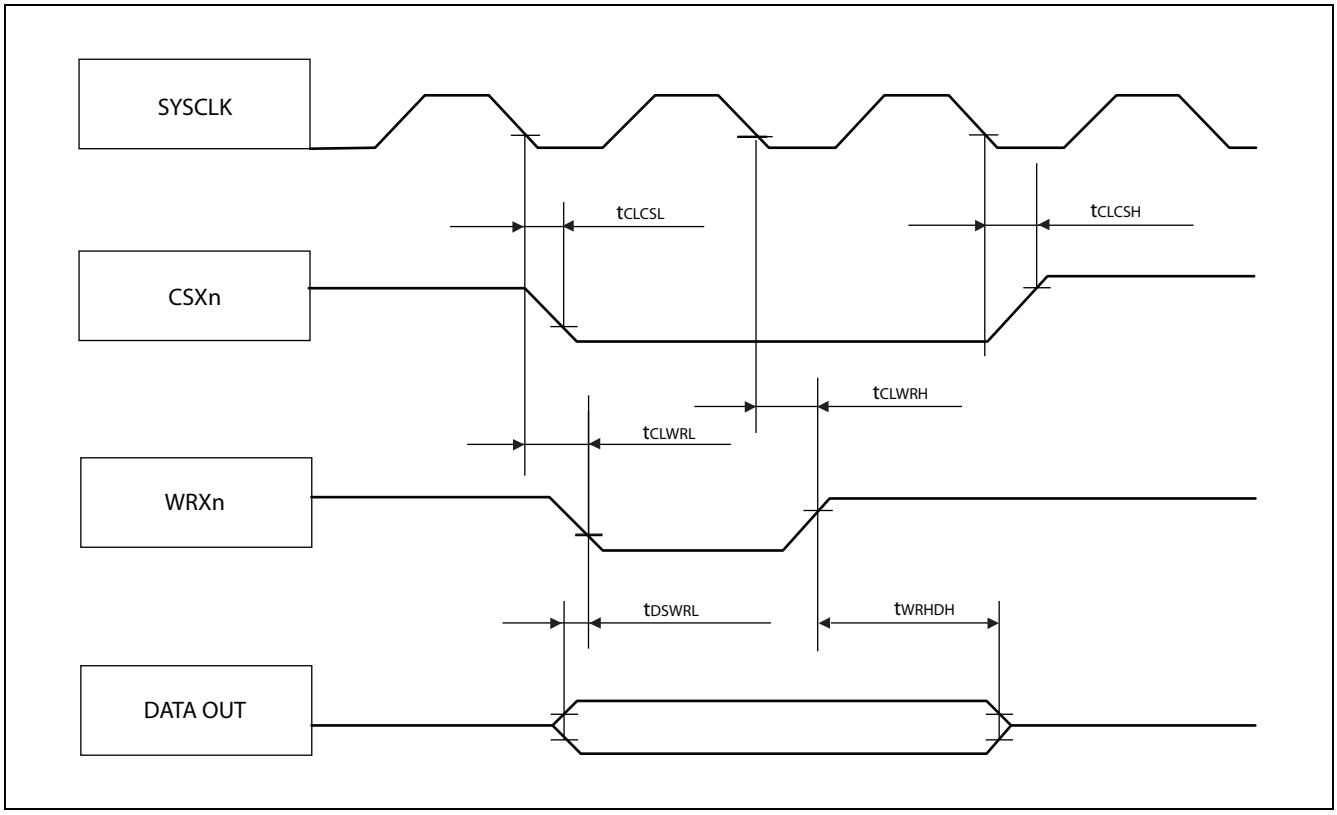
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 x t_{CLKT} - 1	1/2 × t_{CLKT} + 9	ns
	t_{CHCL}		1/2 × t_{CLKT} - 9	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	-	8	ns
	t_{CLCSH}		-	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	-	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

15.7.7.3 Synchronous write access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	-	8	ns
	TCLWRH		0	-	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	- 7	-	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} - 20	-	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	-	8	ns
	TCLCSH		-	12	ns



18. Revision History

Spansion Publication Number: DS07-16609-1E

Version	Date	Remark
2.0	2008-06-19	Initial version
2.1	2008-08-15	Proof reading results from FJ incorporated; Corrected pinout drawings; IO CIRCUIT TYPES: corrected some typos like on the other datasheets; HANDLING DEVICES: updated the section "Notes on PS register" for better understanding; Interrupt Vector Table: corrected the footnotes FLASH: added note about the operation mode switching capability in Boot ROM; corrected flash security vector FSV2 assignments, corrected section about parallel programming, corrected section pin connections in parallel programming mode so that there is only one page added section "Poweron Sequence in parallel programming mode"; ELECTRICAL CHARACTERISTICS: removed the note that analog input/output pins cannot accept +B signal input; splitted I_{LV} into external and internal LV detection current ADC Characteristics: Corrected the items about nonlinearity error; Corrected the company name
3.0	2009-01-09	Page 1: Corrected document name field in top header Block Diagram: Removed SCK0 (LIN-USART0 is asynchronous only) Added Ta=125C characteristics

19. Main Changes in this Edition

Page	Section	Change Results
104	15. Electrical Characteristics 15.4. A/D converter characteristics	Corrected the column “Value” and “Unit” of the parameter “Zero reading voltage” and “Full scale reading voltage”. (Value : AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB Unit : LSB → V)

NOTE: Please see “Document History” for later revised information.