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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w006

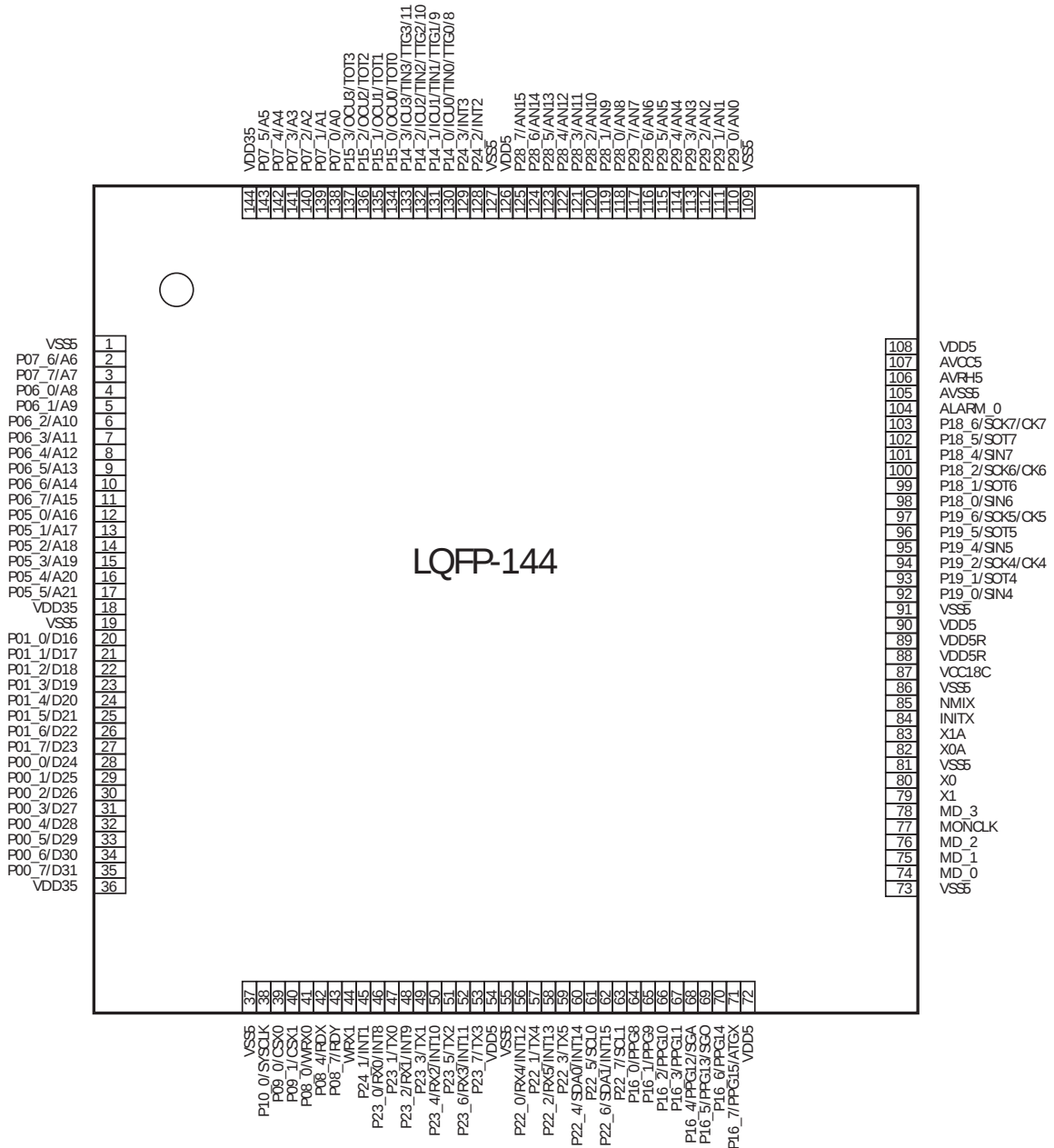
1. Product Lineup

Feature	MB91V460	MB91F465BB/464BB	MB91F467BA/466BA
Max. core frequency (CLKB)	80 MHz	100 MHz	96 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	48 MHz
Max. external bus frequency (CLKT)	40 MHz	50 MHz	48 MHz
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	48 MHz
Technology	0.35μm	0.18μm	0.18μm
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch) ^[1]	MPU (8 ch) ^[1]	MPU (8 ch) ^[1]
Flash memory	Emulation SRAM 32bit read data	MB91F465BB: 544 KByte MB91F464BB: 416 KByte	MB91F467BA: 1088 KByte MB91F466BA: 832 KByte
Satellite Flash memory	-	-	-
Flash Protection	-	yes	yes
D-RAM	64 KByte	24 KByte	24 KByte
ID-RAM	64 KByte	16 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch ^[2]	8 ch ^[2]
ICU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch ^[3]	MD_3=0: 8 ch MD_3=1: 4 ch ^[3]
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch ^[4]	MD_3=0: 8 ch MD_3=1: 4 ch ^[4]
Reload Timer	8 ch	8 ch ^[5]	8 ch ^[5]
PPG 16-bit	16 ch	MD_3=0: 16 ch MD_3=1: 8 ch ^[6]	MD_3=0: 16 ch MD_3=1: 8 ch ^[6]
PFM 16-bit	1 ch	-	-
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA ^[7]	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA ^[7]
C_CAN	6 ch (128msg)	3 ch (32msg)	6 ch (32msg)

2. Pin Assignment

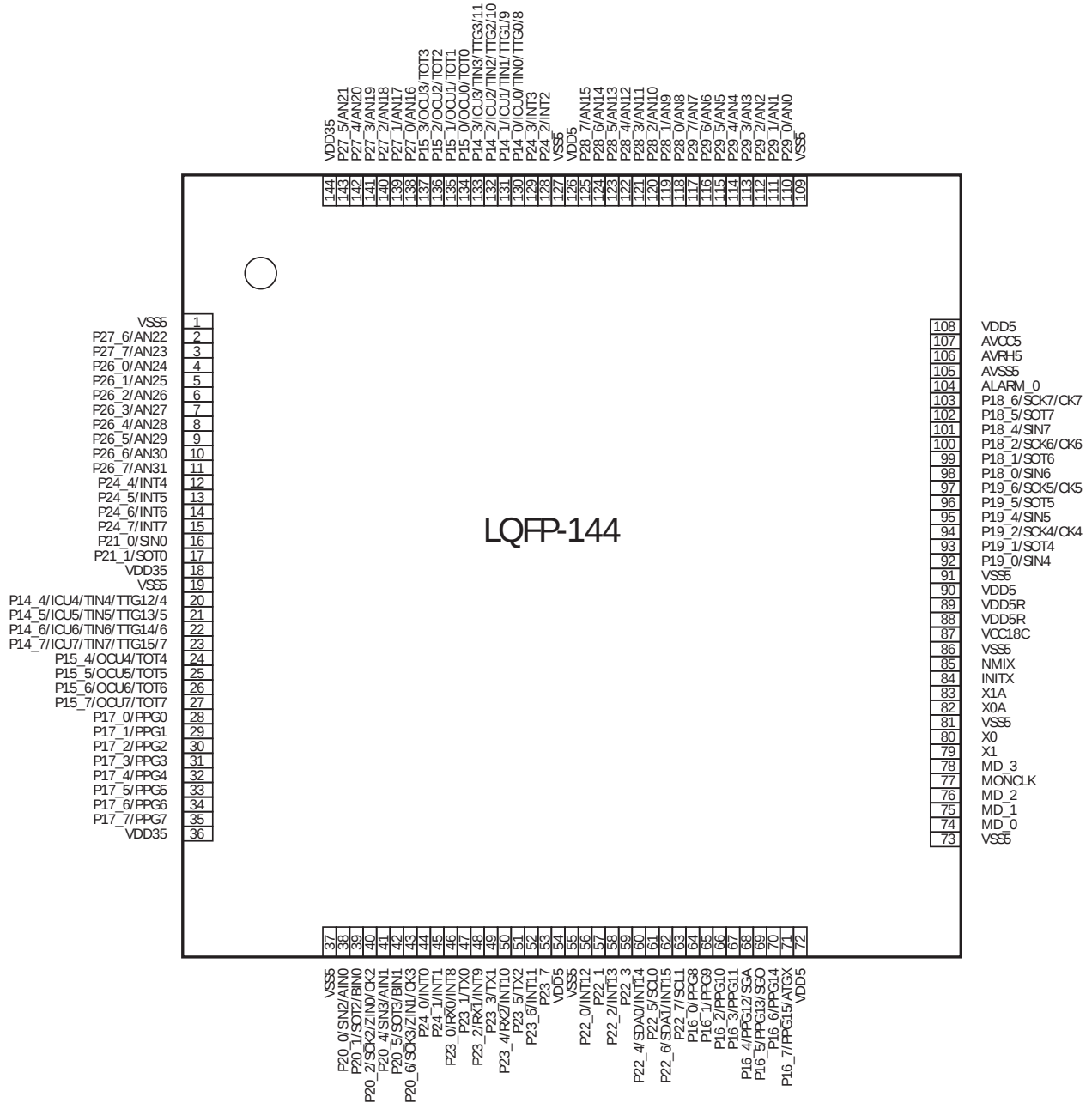
2.1 MB91F467BA/466BA with MD_3=1

(TOP VIEW)

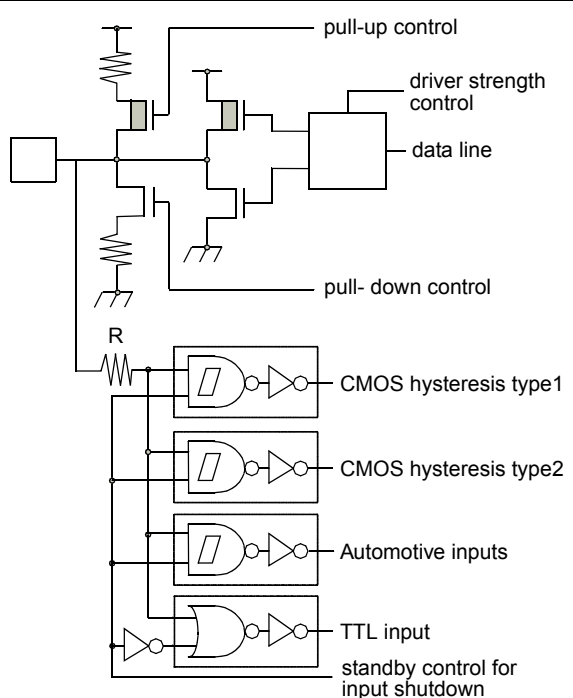
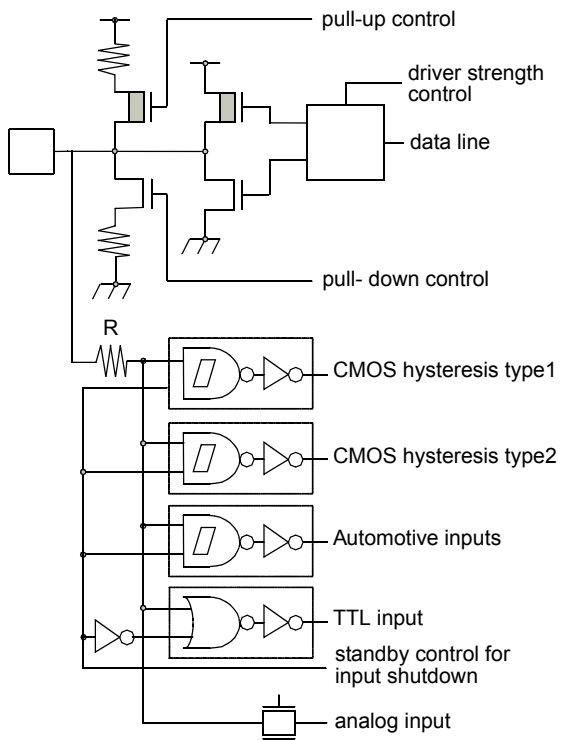


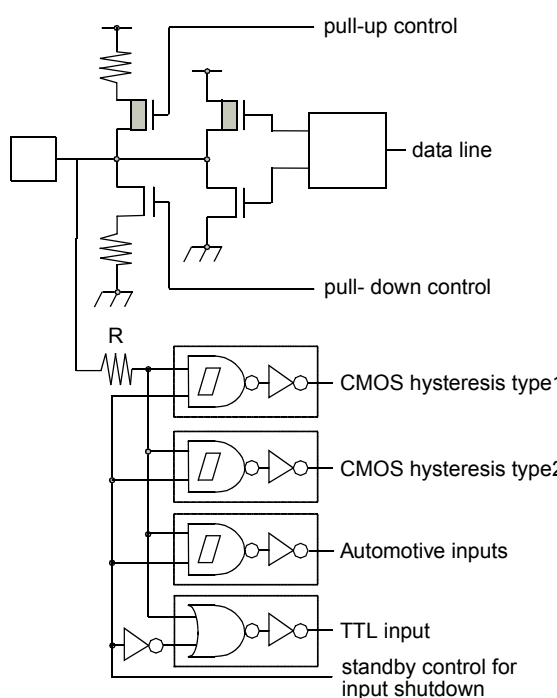
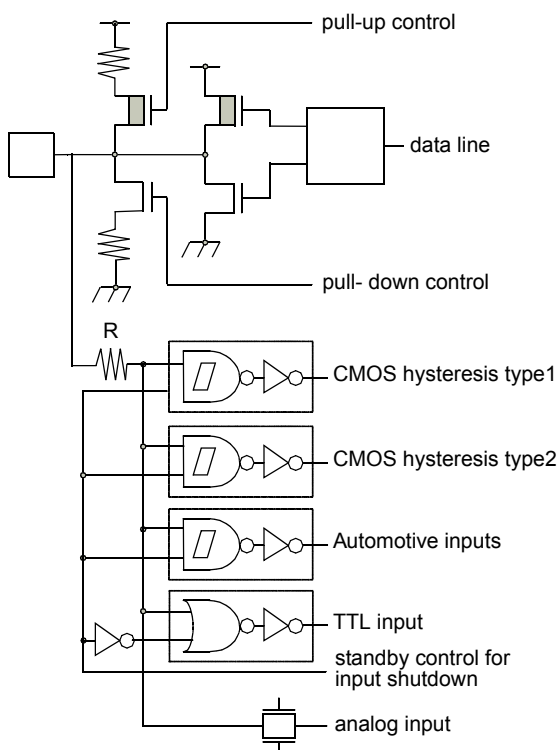
2.4 MB91F465BB/464BB with MD_3=0

(TOP VIEW)



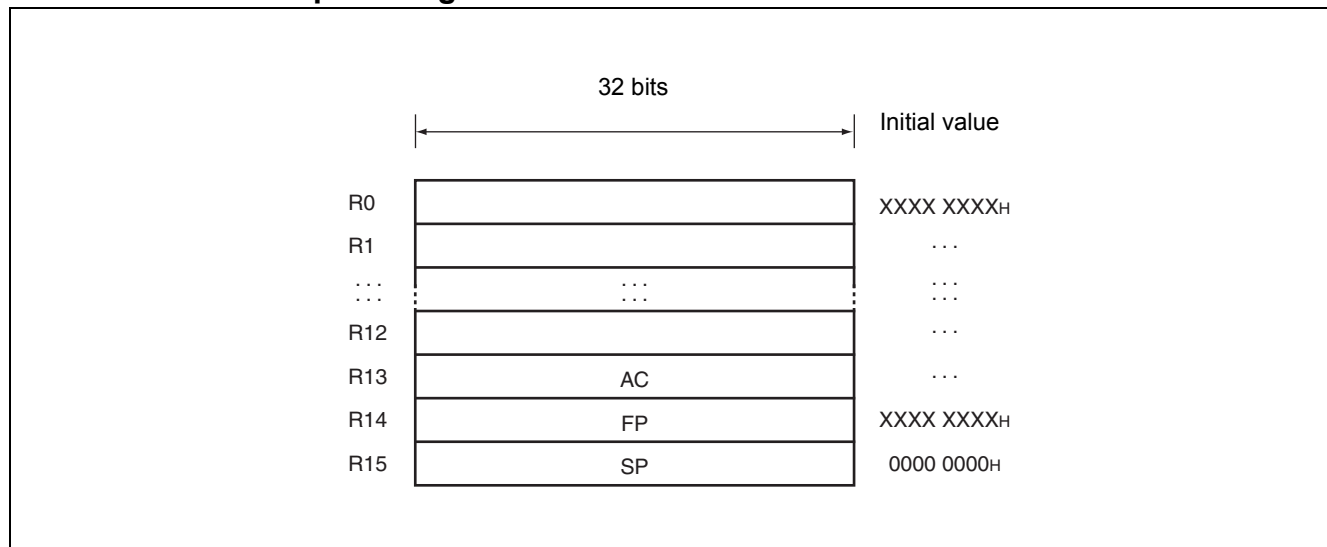
4. I/O Circuit Types

Type	Circuit	Remarks
A		CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
C		CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx.
D		CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. Analog input

8.4 Registers

8.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

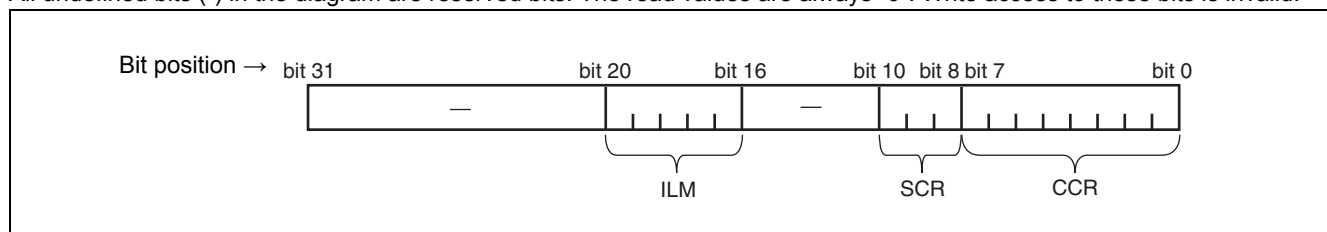
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								
Legend	Memory not available in this area				Memory available in this area				

9.3.3.3 Address Mapping MB91F465BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 - (addr/2)\%4 + addr\%4 - 0D:0000h$
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 + 00:2000h - (addr/2)\%4 + addr\%4 - 0D:0000h$
08:0000h to 0F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	$FA := addr - addr\%02:0000 + (addr\%02:0000h)/2 - (addr/2)\%4 + addr\%4$
08:0000h to 0F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	$FA := addr - addr\%02:0000h + (addr\%02:0000h)/2 + 01:0000h - (addr/2)\%4 + addr\%4$

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.3.3.4 Address Mapping MB91F464BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 - (addr/2)\%4 + addr\%4 - 0D:0000h$
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 + 00:2000h - (addr/2)\%4 + addr\%4 - 0D:0000h$
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	$FA := addr - addr\%02:0000 + (addr\%02:0000h)/2 - (addr/2)\%4 + addr\%4$
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	$FA := addr - addr\%02:0000h + (addr\%02:0000h)/2 + 01:0000h - (addr/2)\%4 + addr\%4$

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

9.6 Flash Security

9.6.1 Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
 FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

9.6.2.1 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2. Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to '0'	set to '0'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '0'	set to '1'	set to '0'	Write Protection (all device modes, without exception)
set all to '0'	set to '0'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes)
set all to '0'	set to '1'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '0'	Write Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes except INTVEC mode MD[2:0]="000")

11. Memory Maps

11.1 MB91F467BA, MB91F466BA

MB91F467BA

00000000 _H	I/O (direct addressing area)
00000400 _H	I/O
00001000 _H	DMA
00002000 _H	
00004000 _H	Flash-Cache (8 KBytes)
00006000 _H	
00007000 _H	Flash memory control
00008000 _H	
0000B000 _H	Boot ROM (4 Kbytes)
0000C000 _H	CAN
0000D000 _H	
0002A000 _H	D-RAM (0 wait, 24 Kbytes)
00030000 _H	ID-RAM (16 Kbytes)
00034000 _H	
00040000 _H	Flash memory (1088 Kbytes)
00150000 _H	
00180000 _H	External bus area
00500000 _H	External data bus
FFFFFFF _H	

Note:

Access prohibited areas

MB91F466BA

00000000 _H	I/O (direct addressing area)
00000400 _H	I/O
00001000 _H	DMA
00002000 _H	
00004000 _H	Flash-Cache (8 KBytes)
00006000 _H	
00007000 _H	Flash memory control
00008000 _H	
0000B000 _H	Boot ROM (4 Kbytes)
0000C000 _H	CAN
0000D000 _H	
0002A000 _H	D-RAM (0 wait, 24 Kbytes)
00030000 _H	ID-RAM (16 Kbytes)
00034000 _H	
00040000 _H	External bus area
00080000 _H	Flash memory (768 Kbytes)
00100000 _H	
00140000 _H	Flash memory (64 Kbytes)
00150000 _H	
00180000 _H	External bus area
00500000 _H	External data bus
FFFFFFF _H	

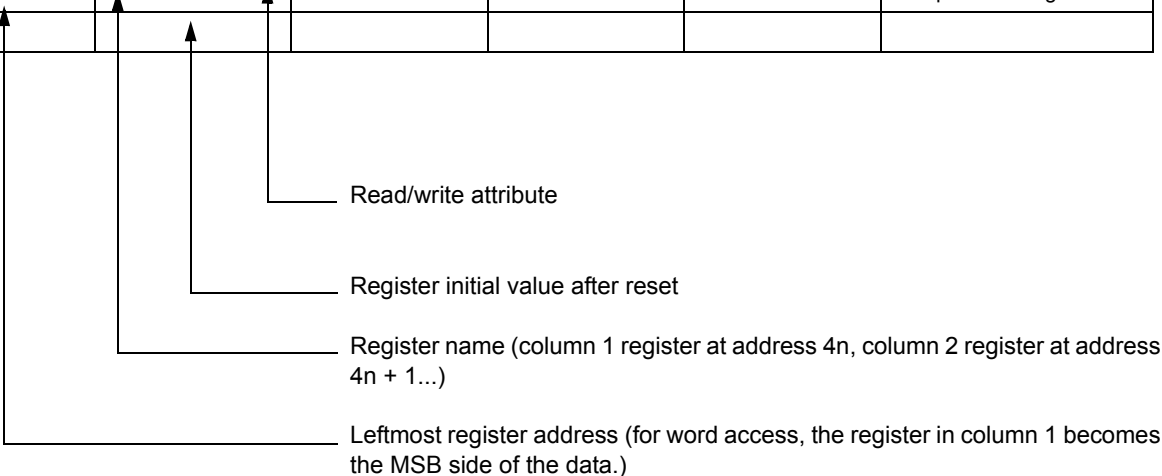
Note:

Access prohibited areas

12. I/O Map

12.1 MB91F467BA/466BA, MB91F465BB/464BB

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Read/write attribute

Register initial value after reset

Register name (column 1 register at address 4n, column 2 register at address 4n + 1...)

Leftmost register address (for word access, the register in column 1 becomes the MSB side of the data.)

Note: Initial values of register bits are represented as follows:

“ 1 ”: Initial value “ 1 ”

“ 0 ”: Initial value “ 0 ”

“ X ”: Initial value “ undefined ”

“ - ”: No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
000158 _H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015C _H	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160 _H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164 _H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168 _H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016C _H	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170 _H to 00017C _H	Reserved				Reserved
000180 _H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184 _H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188 _H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C _H	OCS01 [R/W] --- 0 -- 00 0000 -- 00		OCS23 [R/W] --- 0 -- 00 0000 -- 00		Output Compare 0 to 3
000190 _H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194 _H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198 _H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] -- 0 -- 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019C _H	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0 _H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 _H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] --- 00000	ADECH [R/W] --- 00000	
0001AC _H	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	Alarm Comparator 0 to 1
0001B0 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4 _H	Reserved		TMCSRH0 [R/W] --- 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BC _H	Reserved		TMCSRH1 [R/W] --- 00000	TMCSRL1 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
000200 _H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 _H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224 _H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 _H to 00023C _H	Reserved				
000240 _H	DMACR [R/W] 00 - - 0000	Reserved			
000244 _H to 0002CC _H	Reserved				Reserved
0002D0 _H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4 _H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8 _H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DC _H	OCS45 [R/W] --- 0 -- 00 0000 -- 00		OCS67 [R/W] --- 0 -- 00 0000 -- 00		Output Compare 4 to 7
0002E0 _H	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
0002E4 _H	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
0002E8 _H to 0002EC _H	Reserved				Reserved
0002F0 _H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
0002F4 _H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8 _H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4, OCU 5)
0002FC _H	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6, OCU 7)

Address	Register				Block
	+0	+1	+2	+3	
00C010 _H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014 _H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018 _H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01C _H	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020 _H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
00C024 _H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028 _H to 00C02C _H	Reserved				
00C030 _H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034 _H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038 _H to 00C03C _H	Reserved				
00C040 _H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044 _H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048 _H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
00C04C _H	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050 _H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054 _H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058 _H to 00C05C _H	Reserved				
00C060 _H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064 _H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068 _H to 00C07C _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C140 _H	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
00C144 _H	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
00C148 _H	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
00C14C _H	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
00C150 _H	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
00C154 _H	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
00C158 _H to 00C15C _H	Reserved				
00C160 _H	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
00C164 _H	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
00C168 _H to 00C17C _H	Reserved				
00C180 _H	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
00C184 _H to 00C18C _H	Reserved		Reserved		
00C190 _H	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
00C194 _H to 00C19C _H	Reserved		Reserved		
00C1A0 _H	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
00C1A4 _H to 00C1AC _H	Reserved		Reserved		
00C1B0 _H	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4 _H to 00C1FC _H	Reserved		Reserved		
00C200 _H	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
00C204 _H	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
00C208 _H	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
00C20C _H	BRPE2 [R/W] 00000000 00000000		CBSYNC2		

Address	Register				Block
	+0	+1	+2	+3	
00C310 _H	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register Note: Not on MB91F465BB/MB91F464 BB
00C314 _H	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
00C318 _H	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
00C31C _H	IF1MCTR3 [R/W] 00000000 00000000		Reserved		
00C320 _H	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
00C324 _H	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
00C328 _H to 00C32C _H	Reserved				
00C330 _H	IF1DTA23 [R/W] 00000000 00000000		IF1DTA13 [R/W] 00000000 00000000		
00C334 _H	IF1DTB23 [R/W] 00000000 00000000		IF1DTB13 [R/W] 00000000 00000000		
00C338 _H to 00C33C _H	Reserved				
00C340 _H	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register Note: Not on MB91F465BB/MB91F464 BB
00C344 _H	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
00C348 _H	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
00C34C _H	IF2MCTR3 [R/W] 00000000 00000000		Reserved		
00C350 _H	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
00C354 _H	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
00C358 _H to 00C35C _H	Reserved				
00C360 _H	IF2DTA23 [R/W] 00000000 00000000		IF2DTA13 [R/W] 00000000 00000000		
00C364 _H	IF2DTB23 [R/W] 00000000 00000000		IF2DTB13 [R/W] 00000000 00000000		
00C368 _H to 00C37C _H	Reserved				

12.2 Flash Memory and External Bus Area

12.2.1 MB91F467BA/466BA

64bit read	dat[63:0]								
32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000 _H to 05FFF8 _H	SA8 (64KB)				SA9 (64KB)				ROMS0
060000 _H to 07FFF8 _H	SA10 (64KB)				SA11 (64KB)				ROMS1
080000 _H to 09FFF8 _H	SA12 (64KB)				SA13 (64KB)				ROMS2
0A0000 _H to 0BFFF8 _H	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000 _H to 0DFFF8 _H	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000 _H to 0FFFF0 _H	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8 _H	FMV [R] 06 00 00 00 _H				FRV [R] 00 00 BF F8 _H				
100000 _H to 11FFF8 _H	SA20 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA21 (64KB, MB91F467BA) Reserved (MB91F466BA)				ROMS6
120000 _H to 13FFF8 _H	SA22 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA23 (64KB, MB91F467B) Reserved (MB91F466BA)				
140000 _H to 143FF8 _H	SA0 (8KB)				SA1 (8KB)				ROMS7
144000 _H to 17FF8 _H	SA2 (8KB)				SA3 (8KB)				
148000 _H to 14BFF8 _H	SA4 (8KB)				SA5 (8KB)				
14C000 _H to 14FFF8 _H	SA6 (8KB)				SA7 (8KB)				
150000 _H to 17FFF8 _H	Reserved								

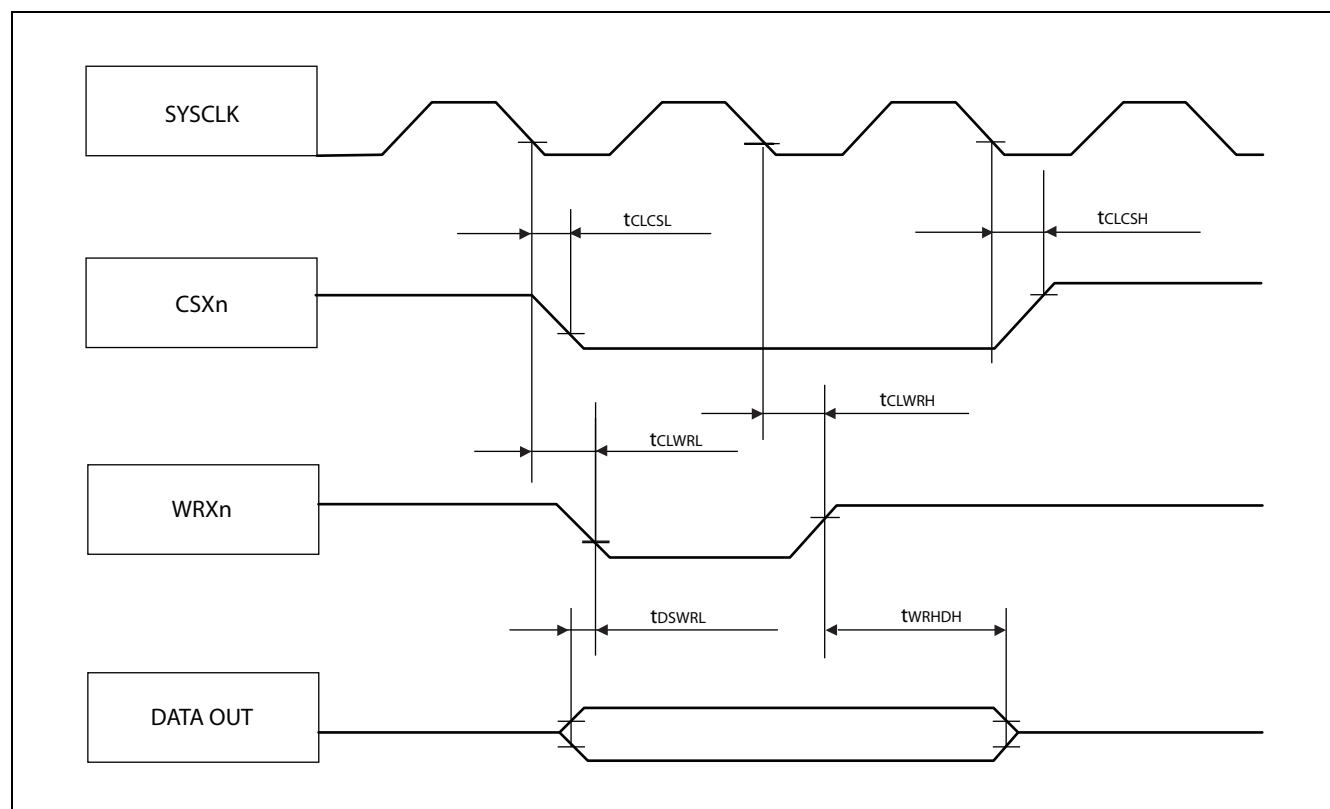
13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level ^[1]		Interrupt vector ^[2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	3FC _H	000FFFFC _H	—
Mode vector	1	01	—	—	3F8 _H	000FFFF8 _H	—
System reserved	2	02	—	—	3F4 _H	000FFFF4 _H	—
System reserved	3	03	—	—	3F0 _H	000FFFF0 _H	—
System reserved	4	04	—	—	3EC _H	000FFFE _C	—
CPU supervisor mode (INT #5 instruction) ^[5]	5	05	—	—	3E8 _H	000FFFE8 _H	—
Memory Protection exception ^[5]	6	06	—	—	3E4 _H	000FFFE4 _H	—
System reserved	7	07	—	—	3E0 _H	000FFFE0 _H	—
System reserved	8	08	—	—	3DC _H	000FFFD _C	—
System reserved	9	09	—	—	3D8 _H	000FFFD8 _H	—
System reserved	10	0A	—	—	3D4 _H	000FFFD4 _H	—
System reserved	11	0B	—	—	3D0 _H	000FFFD0 _H	—
System reserved	12	0C	—	—	3CC _H	000FFFC _C	—
System reserved	13	0D	—	—	3C8 _H	000FFFC8 _H	—
Undefined instruction exception	14	0E	—	—	3C4 _H	000FFFC4 _H	—
NMI request	15	0F	F _H fixed		3C0 _H	000FFFC0 _H	—
External Interrupt 0	16	10	ICR00	440 _H	3BC _H	000FFFB _C	0, 16
External Interrupt 1	17	11			3B8 _H	000FFFB8 _H	1, 17
External Interrupt 2	18	12	ICR01	441 _H	3B4 _H	000FFFB4 _H	2, 18
External Interrupt 3	19	13			3B0 _H	000FFFB0 _H	3, 19
External Interrupt 4	20	14	ICR02	442 _H	3AC _H	000FFFA _C	20
External Interrupt 5	21	15			3A8 _H	000FFFA8 _H	21
External Interrupt 6	22	16	ICR03	443 _H	3A4 _H	000FFFA4 _H	22
External Interrupt 7	23	17			3A0 _H	000FFFA0 _H	23
External Interrupt 8	24	18	ICR04	444 _H	39C _H	000FFF9 _C	—
External Interrupt 9	25	19			398 _H	000FFF98 _H	—
External Interrupt 10	26	1A	ICR05	445 _H	394 _H	000FFF94 _H	—
External Interrupt 11	27	1B			390 _H	000FFF90 _H	—
External Interrupt 12	28	1C	ICR06	446 _H	38C _H	000FFF8 _C	—
External Interrupt 13	29	1D			388 _H	000FFF88 _H	—
External Interrupt 14	30	1E	ICR07	447 _H	384 _H	000FFF84 _H	—
External Interrupt 15	31	1F			380 _H	000FFF80 _H	—
Reload Timer 0	32	20	ICR08	448 _H	37C _H	000FFF7 _C	4, 32
Reload Timer 1	33	21			378 _H	000FFF78 _H	5, 33
Reload Timer 2	34	22	ICR09	449 _H	374 _H	000FFF74 _H	34
Reload Timer 3	35	23			370 _H	000FFF70 _H	35

15.7.7.3 Synchronous write access

($V_{DD35} = 3.0\text{ V to } 5.5\text{ V}$, $V_{SS5} = AV_{SS5} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK $\downarrow$ to WRXn delay time	TCLWRL	SYSCLK WRXn	-	8	ns
	TCLWRH		0	-	ns
Data valid to WRXn $\downarrow$ setup time	TDSWRL	WRXn D31 to D16	-7	-	ns
WRXn $\uparrow$ to Data valid hold time	TWRHDH	WRXn D31 to D16	$t_{CLKT} - 20$	-	ns
SYSCLK $\downarrow$ to CSXn delay time	TCLCSL	SYSCLK CSXn	-	8	ns
	TCLCSH		-	12	ns



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