Infineon Technologies - MB91F467BAPMC-GSE2-W010 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

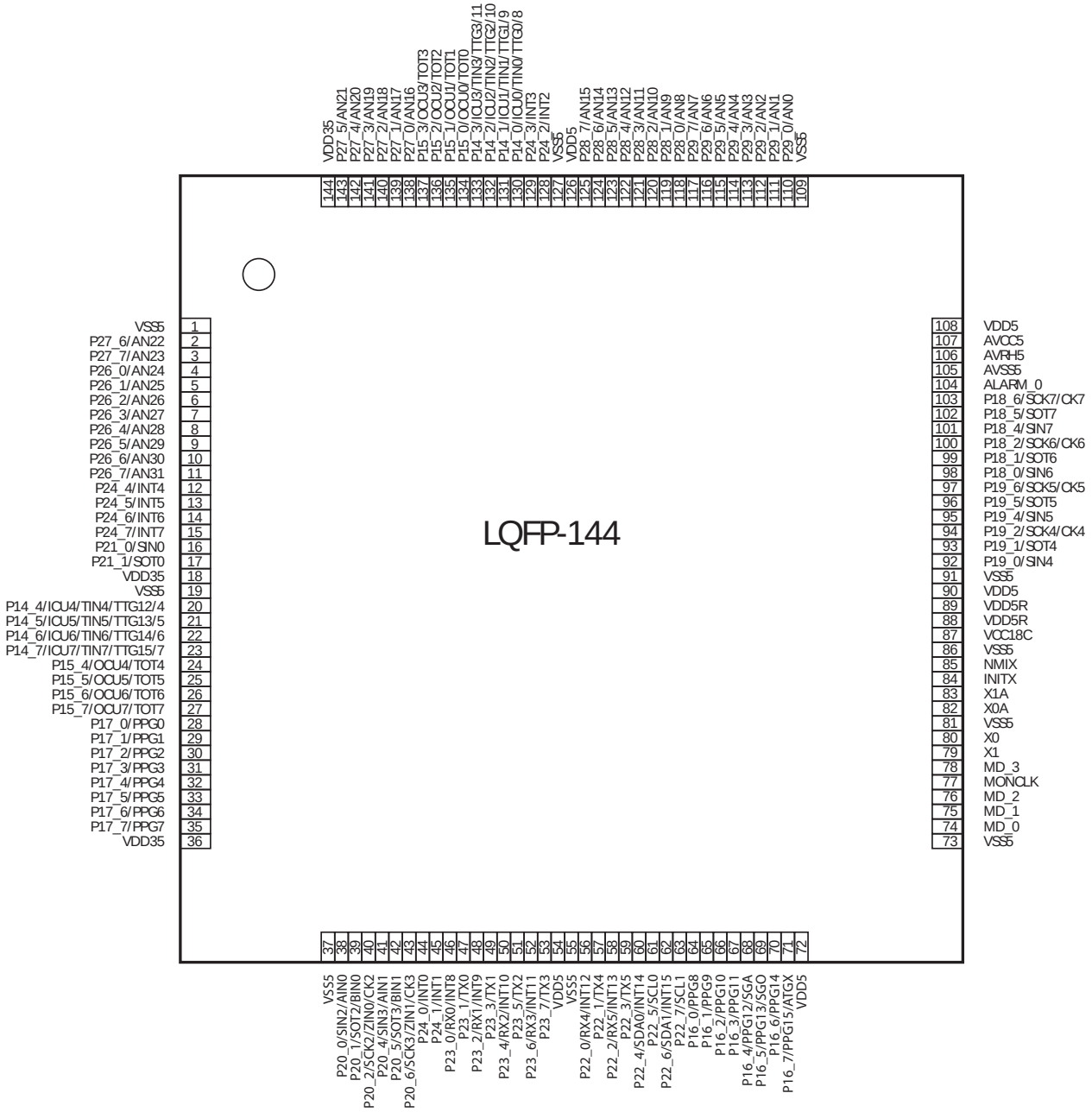
Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w010

1. Product Lineup

Feature	MB91V460	MB91F465BB/464BB	MB91F467BA/466BA
Max. core frequency (CLKB)	80 MHz	100 MHz	96 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	48 MHz
Max. external bus frequency (CLKT)	40 MHz	50 MHz	48 MHz
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	48 MHz
Technology	0.35µm	0.18µm	0.18µm
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)[1]	MPU (8 ch)[1]	MPU (8 ch)[1]
Flash memory	Emulation SRAM 32bit read data	MB91F465BB: 544 KByte MB91F464BB: 416 KByte	MB91F467BA: 1088 KByte MB91F466BA: 832 KByte
Satellite Flash memory	-	-	-
Flash Protection	-	yes	yes
D-RAM	64 KByte	24 KByte	24 KByte
ID-RAM	64 KByte	16 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch[2]	8 ch[2]
ICU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[3]	MD_3=0: 8 ch MD_3=1: 4 ch[3]
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[4]	MD_3=0: 8 ch MD_3=1: 4 ch[4]
Reload Timer	8 ch	8 ch[5]	8 ch[5]
PPG 16-bit	16 ch	MD_3=0: 16 ch MD_3=1: 8 ch[6]	MD_3=0: 16 ch MD_3=1: 8 ch[6]
PFM 16-bit	1 ch	-	-
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]
C_CAN	6 ch (128msg)	3 ch (32msg)	6 ch (32msg)

2.2 MB91F467BA/466BA with MD_3=0

(TOP VIEW)



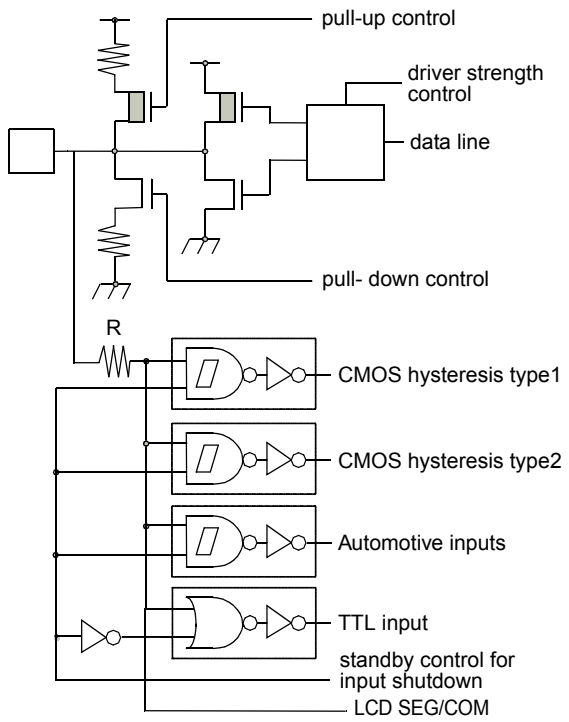
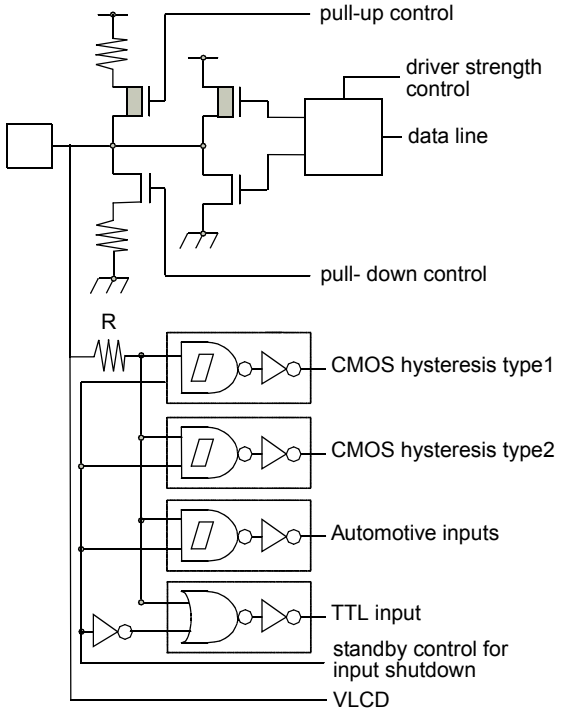
3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

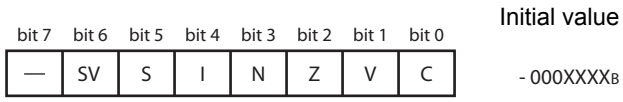
Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466BA			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

3.2 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

8.4.3 CCR (Condition Code Register)



SV: Supervisor flag

S: Stack flag

I: Interrupt enable flag

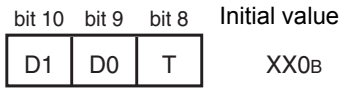
N: Negative enable flag

Z: Zero flag

V: Overflow flag

C: Carry flag

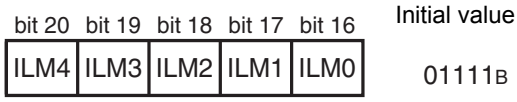
8.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

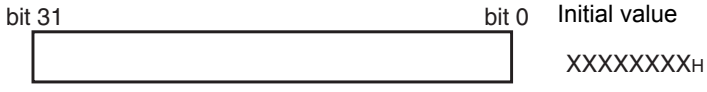
8.4.5 ILM (Interrupt Level Mask Register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111_B" at reset.

8.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

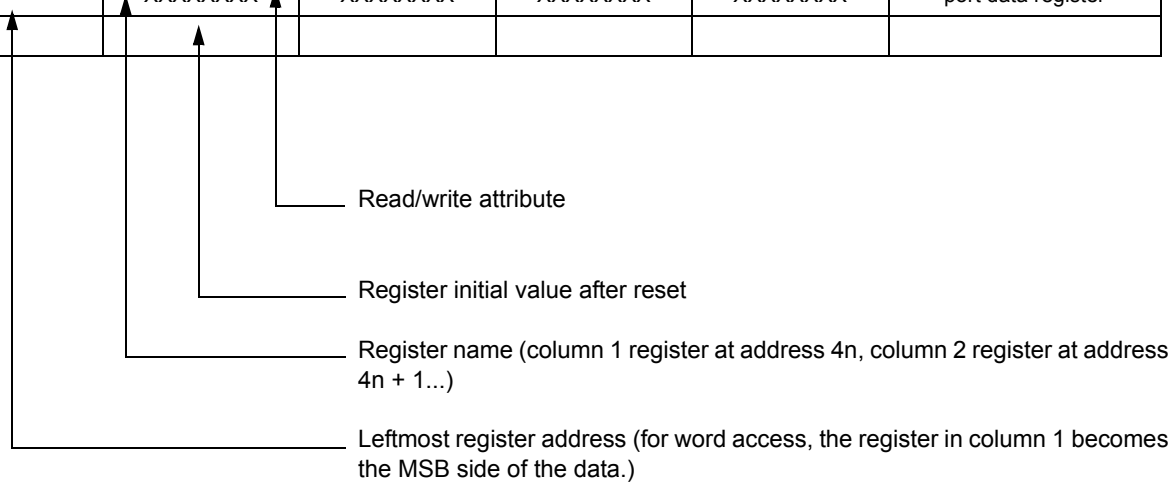
9.3.1.3 Flash Memory Map MB91F465BB

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
Legend	Memory not available in this area				Memory available in this area				

12. I/O Map

12.1 MB91F467BA/466BA, MB91F465BB/464BB

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
$0000E8_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
$0001D4_H$	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
$0001DC_H$	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
$0001E4_H$	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

Address	Register				Block
	+0	+1	+2	+3	
000300_H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308_H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
$00030C_H$ to $00031C_H$	Reserved				Reserved
000320_H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324_H to $00032C_H$	Reserved				Reserved
000330_H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334_H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338_H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
$00033C_H$	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340_H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344_H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348_H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
$00034C_H$	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350_H to $00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 00000000 (MB91F467BA/466BA) 11111111 01000011 (MB91F465BB/464BB)		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	PPER05 [R/W] - - 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 0 - - 0 - - - 0	PPER09 [R/W] - - - - - - 00	PPER10 [R/W] - - - - - - - 0	Reserved	
$000ECC_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - - - - - - 00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
$000F04_H$	Reserved	PPCR05 [R/W] - - 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 1 - - 1 - - - 1	PPCR09 [R/W] - - - - - - 11	PPCR10 [R/W] - - - - - - - 1	Reserved	
$000F0C_H$	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
$000F14_H$	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] - - - - - - 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $003FFC_H$	Reserved				Reserved
002000_H to $006FFC_H$	Flash-cache size is 8 Kbytes : 004000_H to $005FFC_H$				Flash-cache / I-RAM area
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

Address	Register				Block
	+0	+1	+2	+3	
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ to $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$ to $00C18C_H$	Reserved		Reserved		
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$ to $00C19C_H$	Reserved		Reserved		
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$ to $00C1AC_H$	Reserved		Reserved		
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$ to $00C1FC_H$	Reserved		Reserved		
$00C200_H$	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
$00C204_H$	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
$00C208_H$	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
$00C20C_H$	BRPE2 [R/W] 00000000 00000000		CBSYNC2		

Address	Register				Block
	+0	+1	+2	+3	
$00C310_H$	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register **Note**: Not on MB91F465BB/MB91F464BB
$00C314_H$	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
$00C318_H$	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
$00C31C_H$	IF1MCTR3 [R/W] 00000000 00000000		Reserved		
$00C320_H$	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
$00C324_H$	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
$00C328_H$ to $00C32C_H$	Reserved				
$00C330_H$	IF1DTA23 [R/W] 00000000 00000000		IF1DTA13 [R/W] 00000000 00000000		
$00C334_H$	IF1DTB23 [R/W] 00000000 00000000		IF1DTB13 [R/W] 00000000 00000000		
$00C338_H$ to $00C33C_H$	Reserved				
$00C340_H$	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register **Note:** Not on MB91F465BB/MB91F464BB
$00C344_H$	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
$00C348_H$	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
$00C34C_H$	IF2MCTR3 [R/W] 00000000 00000000		Reserved		
$00C350_H$	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
$00C354_H$	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
$00C358_H$ to $00C35C_H$	Reserved				
$00C360_H$	IF2DTA23 [R/W] 00000000 00000000		IF2DTA13 [R/W] 00000000 00000000		
$00C364_H$	IF2DTB23 [R/W] 00000000 00000000		IF2DTB13 [R/W] 00000000 00000000		
$00C368_H$ to $00C37C_H$	Reserved				

15.3 DC Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	CMOS hysteresis input
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	-	V_{DD} + 0.3	V	4.5 V ? V_{DD} ? 5.5 V
				0.74 × V_{DD}	-	V_{DD} + 0.3	V	3 V ? V_{DD} < 4.5 V
		-	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	
		-	Port inputs if TTL input is selected	2.0	-	V_{DD} + 0.3	V	
	V_{IHR}	INITX	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	-	V_{DD} - 0.3	-	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	-	2.5	-	V_{DD} + 0.3	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	-	0.2 × V_{DD}	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	-	0.3 × V_{DD}	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	-	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} - 0.3	-	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		-	Port inputs if TTL input is selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILR}	INITX	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	-	V_{SS} - 0.3	-	0.5	V	External clock in "Oscillation mode"

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 1.6mA	V_{DD} - 0.5	-	-	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	
Output “L“ voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 1.6mA	-	-	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 3mA	-	-	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 3mA	-	-	0.4	V	
Input leakage current	I_{IL}	Pnn_m[1]	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	- 3	-	+ 3		
Analog input leakage current	I_{AIN}	ANn[2]	3.0V ≤ V_{DD} ≤ 5.5V T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V T_A=125 °C	- 3	-	+ 3	mA	
Pull-up resistance	R_{UP}	Pnn_m [3] INITX	3.0V ≤ V_{DD} ≤ 3.6V	40	100	160	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m [4]	3.0V ≤ V_{DD} ≤ 3.6V	40	100	180	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	

15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:

- ❒ - IO_{drive} = 5 mA
- ❒ - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ - $V_{SS}5$ = 0 V
- ❒ - T_a = -40 °C to +125× °C
- ❒ - C_l = 50 pF (load capacity value of pins when testing)
- ❒ - VOL = 0.2 x $V_{DD}5$
- ❒ - VOH = 0.8 x $V_{DD}5$
- ❒ - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	-	4 t_{CLKP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		- 30	30	- 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} - 30[1]	-	m × t_{CLKP} - 20[1]	-	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	-	t_{CLKP} + 45	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	-	0	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
Serial clock“L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		-	2 t_{CLKP} + 55	-	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	-	10	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK rising time	t_{FE}	SCKn		-	20	-	20	ns
SCK falling time	t_{RE}	SCKn		-	20	-	20	ns

1. Parameter m depends on t_{SCYCI} and can be calculated as :

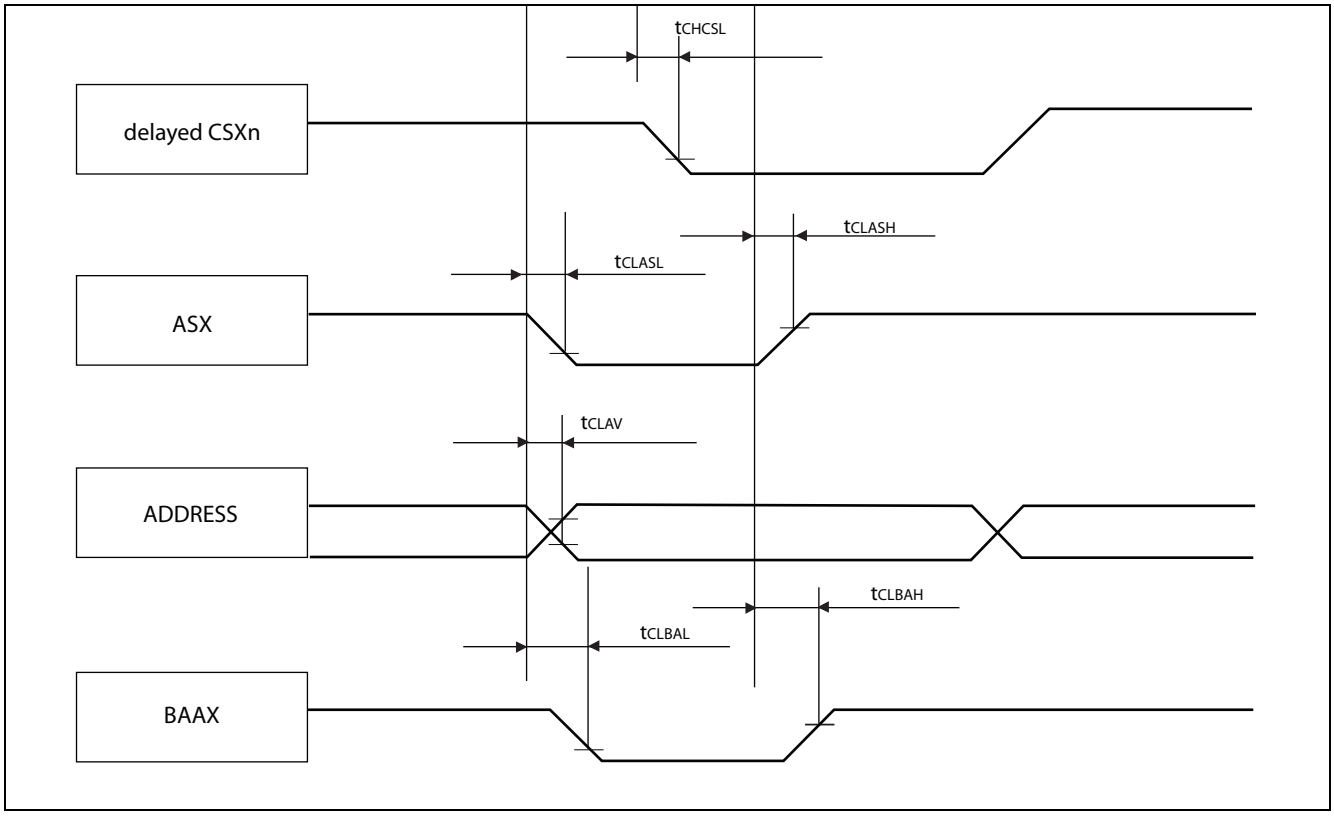
■ if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2

■ if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :

■ The above values are AC characteristics for CLK synchronous mode.

■ t_{CLKP} is the cycle time of the peripheral clock.


tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Document History

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