Infineon Technologies - MB91F467BAPMC-GSE2-W012 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

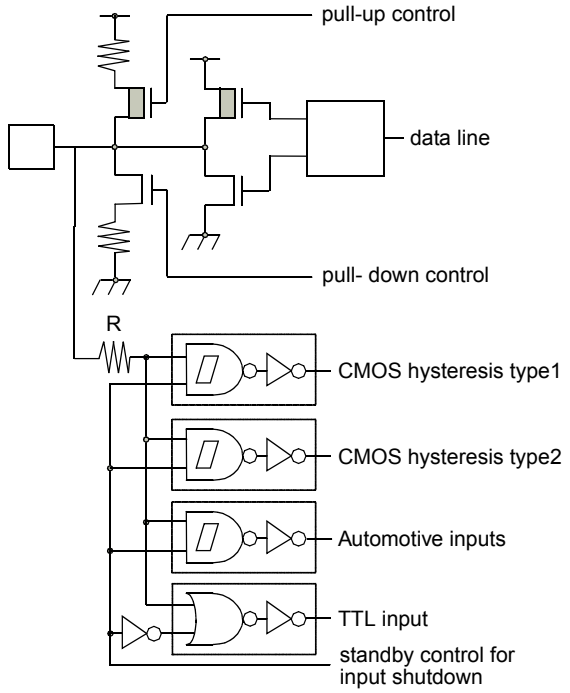
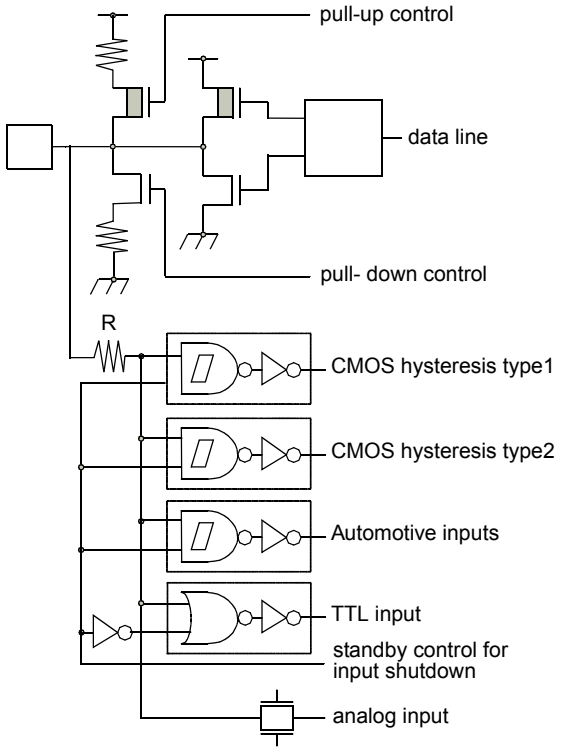
Applications of "Embedded - Microcontrollers"

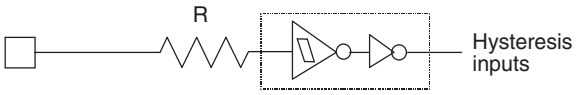
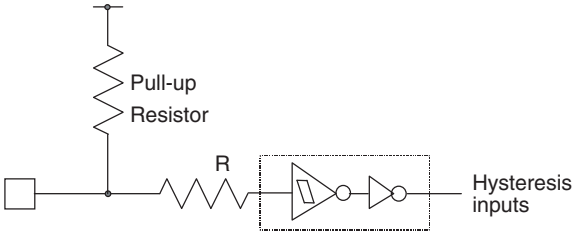
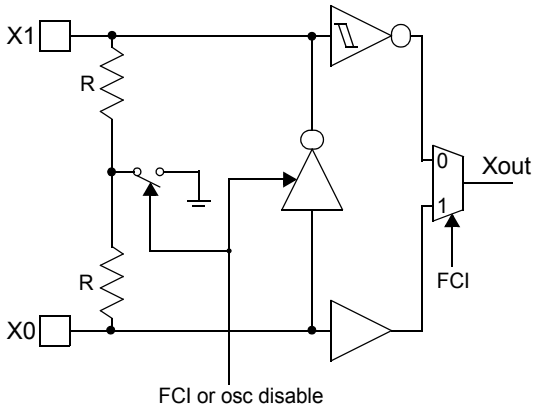
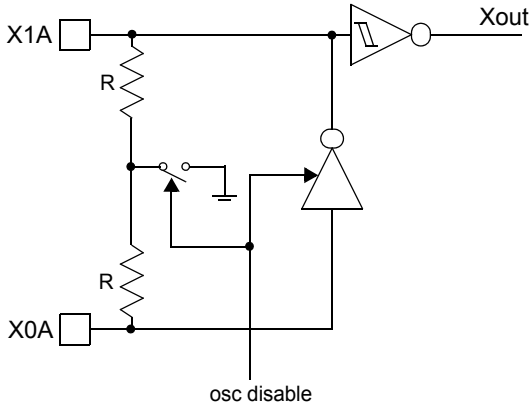
Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w012

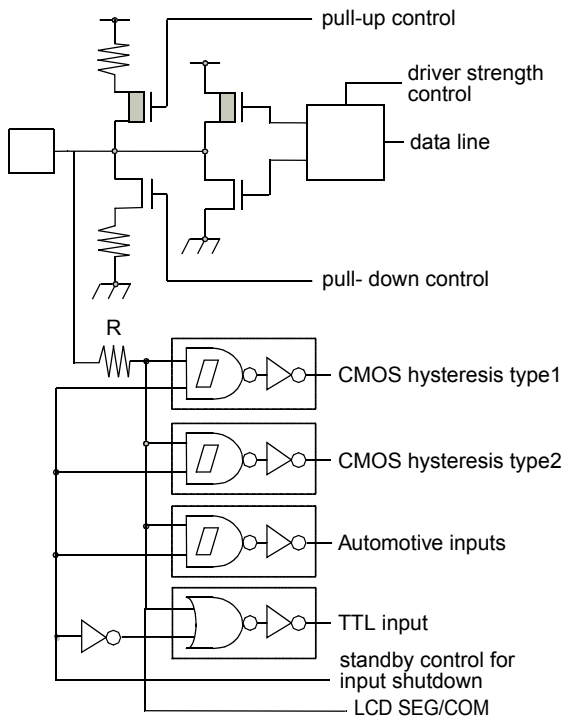
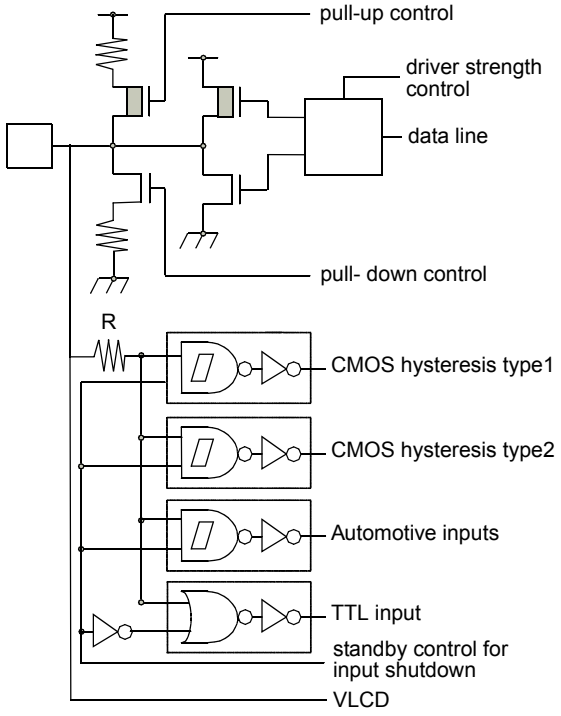
3.2.1 Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

1. For information about the I/O circuit type, refer to “I/O Circuit Types”.

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: ■ Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,the operation before and after the EIT always proceeds according to specification.

- **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**
  (a) a user interrupt or NMI is accepted;
  (b) single-step execution is performed;
  (c) execution breaks due to a data event or from the emulator menu.
  1. D0 and D1 flags are updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

- **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**
  1. The PS register is updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

9.3 Flash Access in CPU mode

9.3.1 Flash Configuration

9.3.1.1 Flash Memory Map MB91F467BA

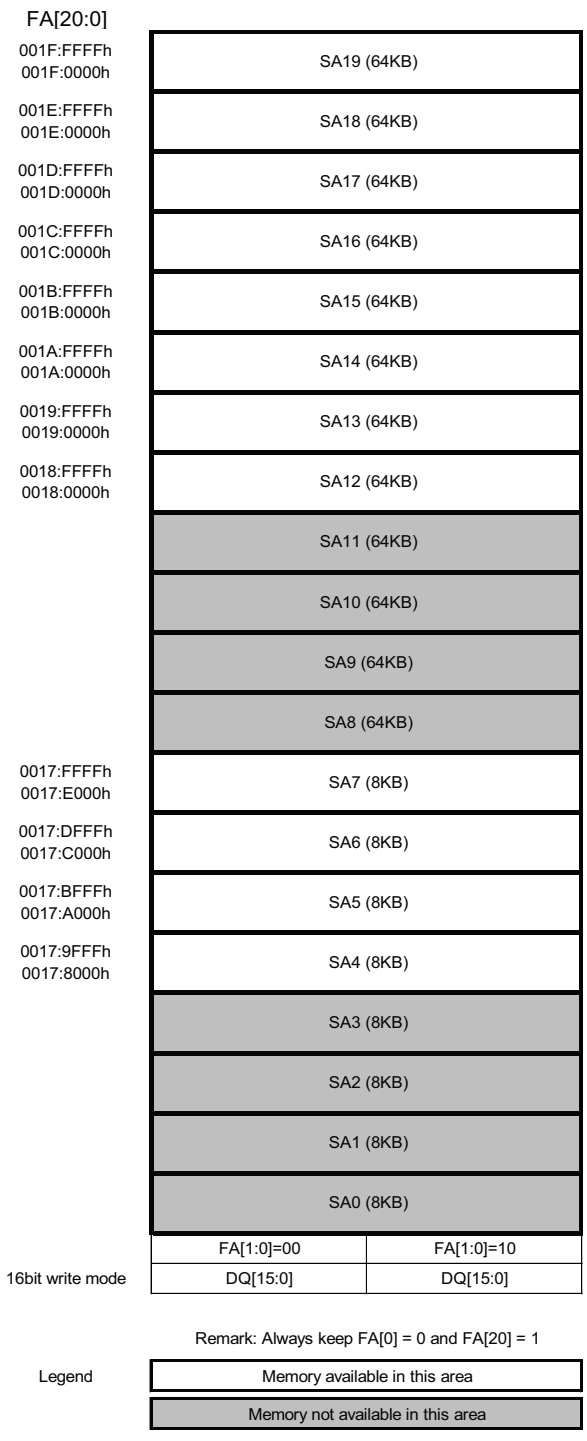
Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

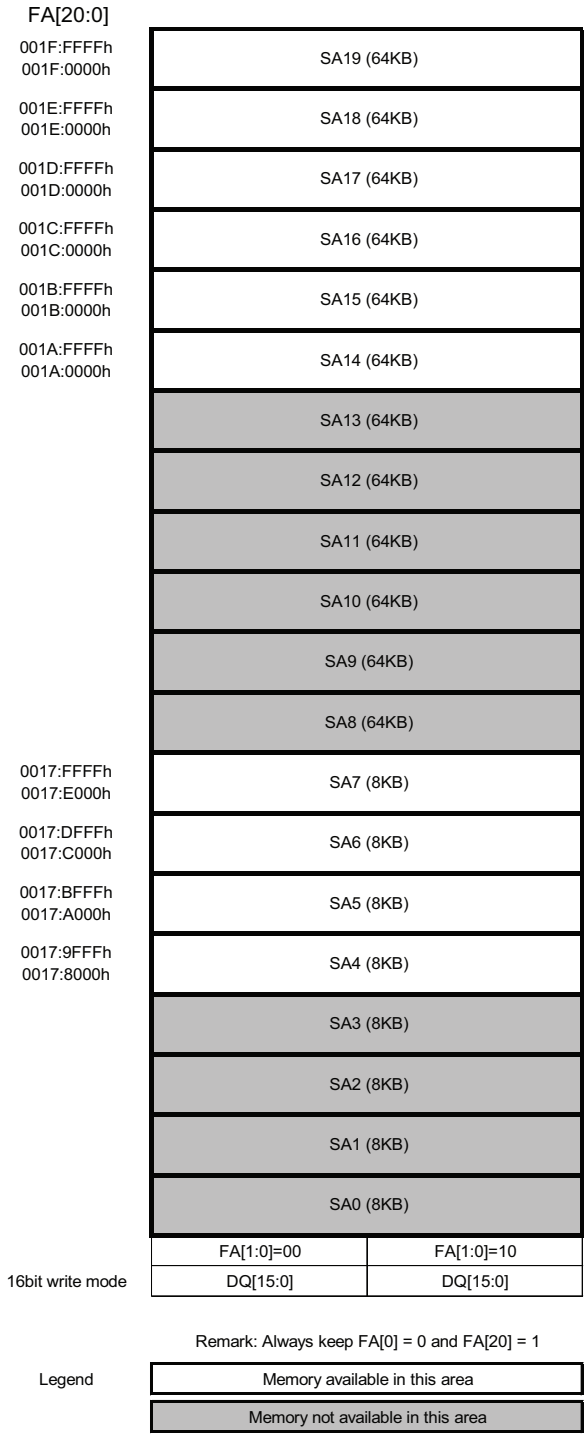
Legend	Memory not available in this area	Memory available in this area

MB91F465BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

MB91F464BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

9.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

9.6 Flash Security

9.6.1 Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

9.6.2.1 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2. Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to ‘0’	set to ‘0’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘0’	Write Protection (all device modes, without exception)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes)
set all to ‘0’	set to ‘1’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘0’	Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”)

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34[R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control

Address	Register				Block
	+0	+1	+2	+3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$ to $000D3C_H$	Reserved				
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - -0	Reserved	
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D7C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags **Note:** Not on MB91F465BB/MB91F464BB
$00C584_H$ to $00C58C_H$	Reserved				
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
$00C594_H$ to $00C59C_H$	Reserved				
$00C5A0_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
$00C5A4_H$ to $00C5AC_H$	Reserved				
$00C5B0_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
$00C5B4_H$ to $00EFFC_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--000000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved

12.2 Flash Memory and External Bus Area

12.2.1 MB91F467BA/466BA

64bit read	dat[63:0]								
32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFF8_H$	SA8 (64KB)				SA9 (64KB)				ROMS0
060000_H to $07FFF8_H$	SA10 (64KB)				SA11 (64KB)				ROMS1
080000_H to $09FFF8_H$	SA12 (64KB)				SA13 (64KB)				ROMS2
$0A0000_H$ to $0BFFF8_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
$0C0000_H$ to $0DFFF8_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
$0E0000_H$ to $0FFFF0_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				FRV [R] $00\ 00\ BF\ F8_H$				
100000_H to $11FFF8_H$	SA20 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA21 (64KB, MB91F467BA) Reserved (MB91F466BA)				ROMS6
120000_H to $13FFF8_H$	SA22 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA23 (64KB, MB91F467B) Reserved (MB91F466BA)				
140000_H to $143FF8_H$	SA0 (8KB)				SA1 (8KB)				ROMS7
144000_H to $17FF8_H$	SA2 (8KB)				SA3 (8KB)				
148000_H to $14BFF8_H$	SA4 (8KB)				SA5 (8KB)				
$14C000_H$ to $14FFF8_H$	SA6 (8KB)				SA7 (8KB)				
150000_H to$17FFF8_H$	Reserved								

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
PPG 2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG 3	115	73			230_H	$000FFE30_H$	99
PPG 4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG 5	117	75			228_H	$000FFE28_H$	101
PPG 6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG 7	119	77			220_H	$000FFE20_H$	103
PPG 8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG 9	121	79			218_H	$000FFE18_H$	105
PPG 10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG 11	123	7B			210_H	$000FFE10_H$	107
PPG 12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG 13	125	7D			208_H	$000FFE08_H$	109
PPG 14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG 15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—
Reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Reserved	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
System reserved	135	87			$1E0_H$	$000FFDE0_H$	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Reserved	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
Reserved	139	8B			$1D0_H$	$000FFDD0_H$	—
Time base Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

1. The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
2. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.
3. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])
4. Used by REALOS
5. Memory Protection Unit (MPU) support

14. Recommended Settings

14.1 PLL and Clock Gear Settings

Please note that for MB91F467BA/466BA and MB91F465BB/464BB the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Table 7. Recommended PLL divider and clock gear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	Not on MB91F467BA/466BA
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 1.6mA	V_{DD} - 0.5	-	-	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	
Output “L“ voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 1.6mA	-	-	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 3mA	-	-	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 3mA	-	-	0.4	V	
Input leakage current	I_{IL}	Pnn_m[1]	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	- 3	-	+ 3		
Analog input leakage current	I_{AIN}	ANn[2]	3.0V ≤ V_{DD} ≤ 5.5V T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V T_A=125 °C	- 3	-	+ 3	mA	
Pull-up resistance	R_{UP}	Pnn_m [3] INITX	3.0V ≤ V_{DD} ≤ 3.6V	40	100	160	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m [4]	3.0V ≤ V_{DD} ≤ 3.6V	40	100	180	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current F467BA F466BA	I_{CC}	$V_{DD}5R$	CLKB: 96 MHz CLKP: 48 MHz CLKT: 48 MHz CLKCAN: 48 MHz	–	120	150	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	–	30	150	µA	At stop mode [5]
			T_A = + 105 °C	–	0.4	2.0	mA	
			T_A = + 125 °C	–	1.0	5.0	mA	
			T_A = + 25 °C	–	100	500	µA	RTC: 4 MHz mode [5]
			T_A = + 105 °C	–	0.5	2.4	mA	
			T_A = + 125 °C	–	1.1	5.4	mA	
			T_A = + 25 °C	–	50	250	µA	RTC: 100 kHz mode [5]
			T_A = + 105 °C	–	0.45	2.2	mA	
			T_A = + 125 °C	–	1.05	5.2	mA	
	I_{LVE}	$V_{DD}5$	–	–	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	–	–	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	–	–	250	500	µA	Main clock (4 MHz)
			–	–	20	40	µA	Sub clock (32 kHz)
Power supply current F465BB F464BB	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	-	30	150	µA	At stop mode [5]
			T_A = + 105 °C	-	0.3	2.0	mA	
			T_A = + 125 °C	-	0.75	5.0	mA	
			T_A = + 25 °C	-	100	500	µA	RTC: 4 MHz mode [5]
			T_A = + 105 °C	-	0.5	2.4	mA	
			T_A = + 125 °C	-	0.85	5.4	mA	
			T_A = + 25 °C	-	50	250	µA	RTC: 100 kHz mode[5]
			T_A = + 105 °C	-	0.4	2.2	mA	
			T_A = + 125 °C	-	0.8	5.2	mA	
	I_{LVE}	$V_{DD}5$	–	–	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	–	–	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

16. Ordering Information

Part number	Package	Remarks
MB91F465BBPMC-GSE2 MB91F467BAPMC-GSE2	144-pin plastic LQFP (FPT-144P-M08)	Lead-free package

18. Revision History

Spansion Publication Number: DS07-16609-1E

Version	Date	Remark
2.0	2008-06-19	Initial version
2.1	2008-08-15	Proof reading results from FJ incorporated; Corrected pinout drawings; IO CIRCUIT TYPES: corrected some typos like on the other datasheets; HANDLING DEVICES: updated the section "Notes on PS register" for better understanding; Interrupt Vector Table: corrected the footnotes FLASH: added note about the operation mode switching capability in Boot ROM; corrected flash security vector FSV2 assignments, corrected section about parallel programming, corrected section pin connections in parallel programming mode so that there is only one page added section "Poweron Sequence in parallel programming mode"; ELECTRICAL CHARACTERISTICS: removed the note that analog input/output pins cannot accept +B signal input; splitted I_{LV} into external and internal LV detection current ADC Characteristics: Corrected the items about nonlinearity error; Corrected the company name
3.0	2009-01-09	Page 1: Corrected document name field in top header Block Diagram: Removed SCK0 (LIN-USART0 is asynchronous only) Added Ta=125C characteristics

19. Main Changes in this Edition

Page	Section	Change Results
104	15. Electrical Characteristics 15.4. A/D converter characteristics	Corrected the column “Value” and “Unit” of the parameter “Zero reading voltage” and “Full scale reading voltage”. (Value : AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB Unit : LSB → V)

NOTE: Please see “Document History” for later revised information.