Infineon Technologies - MB91F467BAPMC-GSE2-W013 Datasheet

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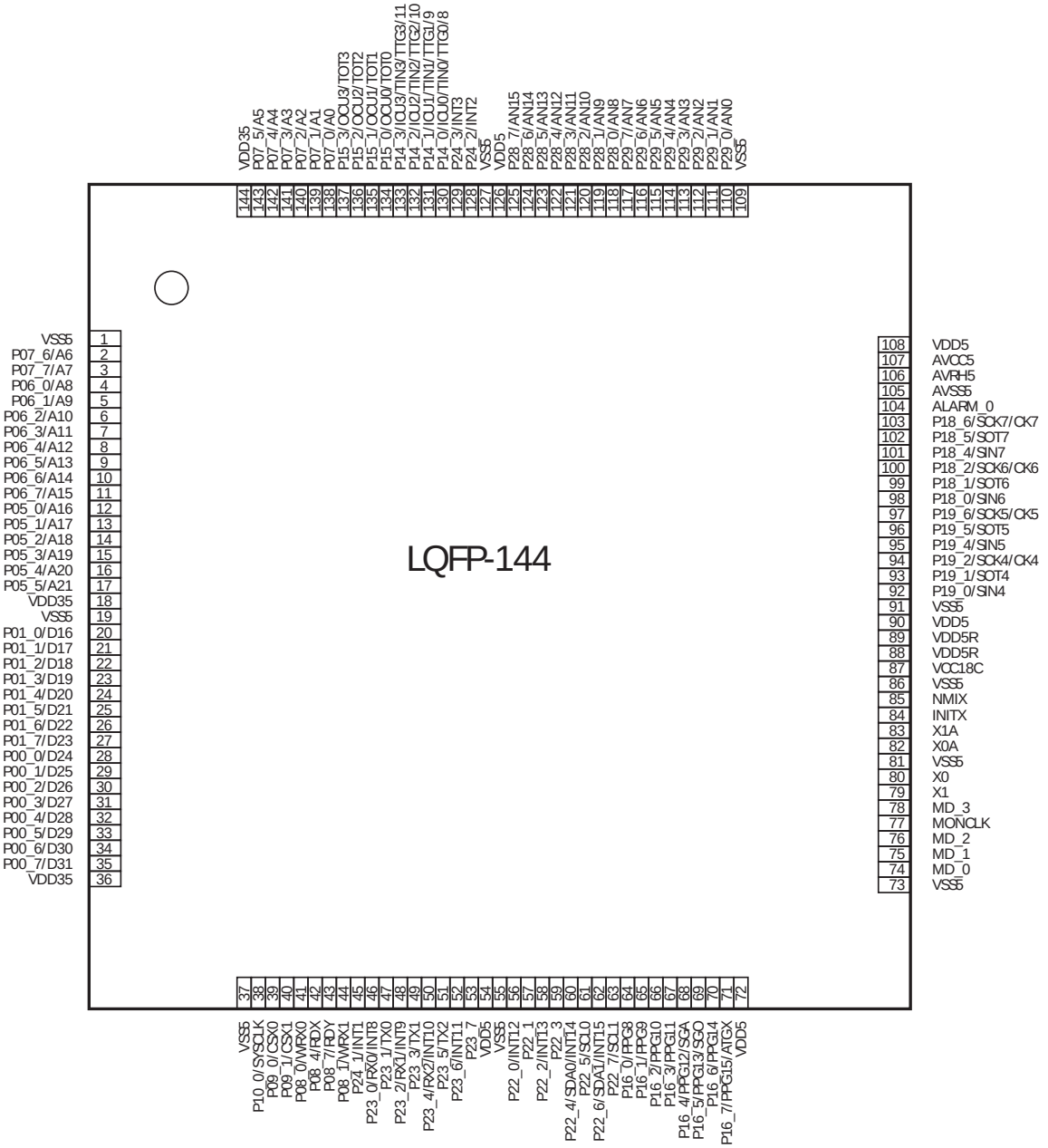
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w013

2.3 MB91F465BB/464BB with MD_3=1

(TOP VIEW)



3.2.1 Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

1. For information about the I/O circuit type, refer to “I/O Circuit Types”.

9.3 Flash Access in CPU mode

9.3.1 Flash Configuration

9.3.1.1 Flash Memory Map MB91F467BA

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

9.6.3 Security Vector FSV2 MB91F467BA/466BA

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 5. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to “0”	set to “1”	
FSV2[1]	SA9	set to “0”	set to “1”	
FSV2[2]	SA10	set to “0”	set to “1”	
FSV2[3]	SA11	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[12]	SA20 (MB91F467BA)	set to “0”	set to “1”	
FSV2[13]	SA21 (MB91F467BA)	set to “0”	set to “1”	
FSV2[14]	SA22 (MB91F467BA)	set to “0”	set to “1”	
FSV2[15]	SA23 (MB91F467BA)	set to “0”	set to “1”	
FSV2[31:16]	–	set to “0”	set to “1”	not available

Note: See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.4 Security Vector FSV2 MB91F465BB/464BB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

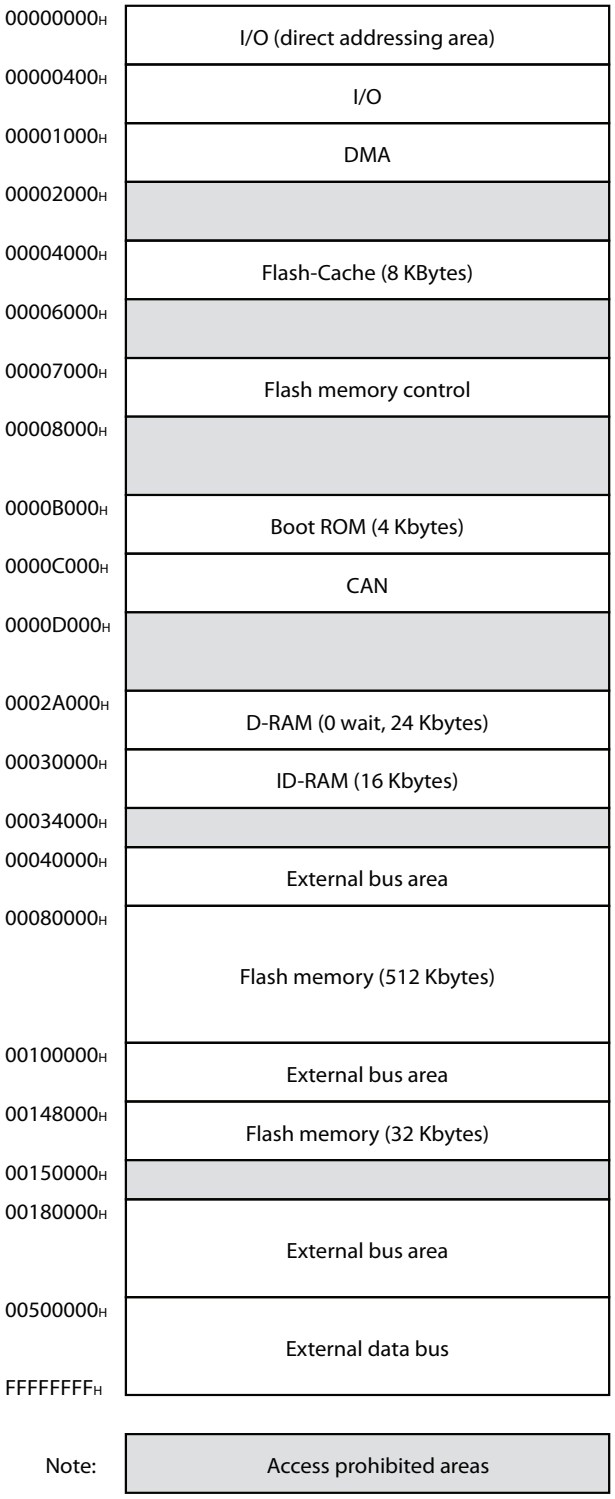
Table 6. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[3:0]	–	–	–	not available
FSV2[4]	SA12 (MB91F465BB)	set to “0”	set to “1”	
FSV2[5]	SA13 (MB91F465BB)	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	–	–	–	not available

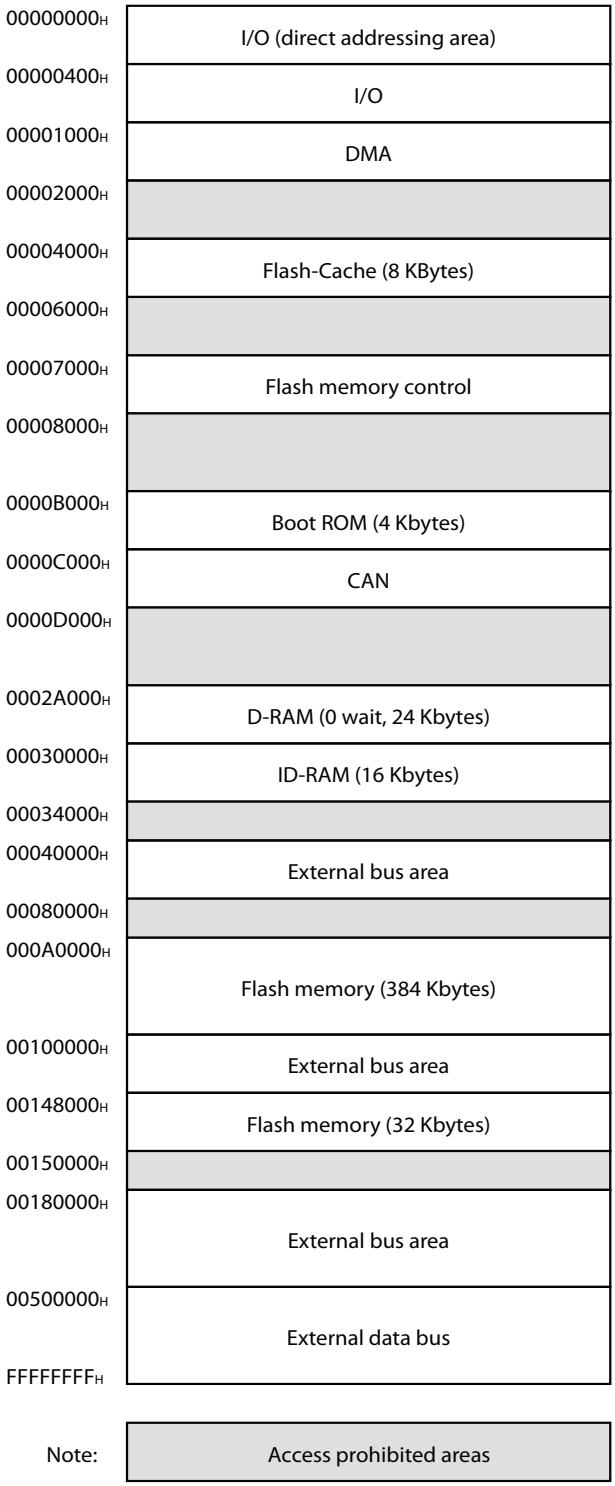
Note: See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

11.2 MB91F465BB, MB91F464BB

MB91F465BB



MB91F464BB



Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004_H	Reserved	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	Reserved	
$00000C_H$	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020_H to $00002C_H$	Reserved				
000030_H	EIRR0 [R/W] MB91F467BA: 00000000:MD3=0 11110000:MD3=1 MB91F465BB: XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034_H	EIRR1 [R/W] MB91F467BA: 00000000 MB91F465BB: XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC		Delay interrupt
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048_H $00004C_H$	Reserved				Reserved
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved		Reserved		
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved		Reserved		
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved		Reserved		
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved		Reserved		
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$ to $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$ to $00C13C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C510_H$	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF 1 Register **Note:** Not on MB91F465BB/MB91F464BB
$00C514_H$	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
$00C518_H$	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		
$00C51C_H$	IF1MCTR5 [R/W] 00000000 00000000		Reserved		
$00C520_H$	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		
$00C524_H$	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		
$00C528_H$ to $00C52C_H$	Reserved				
$00C530_H$	IF1DTA25 [R/W] 00000000 00000000		IF1DTA15 [R/W] 00000000 00000000		
$00C534_H$	IF1DTB25 [R/W] 00000000 00000000		IF1DTB15 [R/W] 00000000 00000000		
$00C538_H$ to $00C53C_H$	Reserved				
$00C540_H$	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF 2 Register **Note**: Not on MB91F465BB/MB91F464BB
$00C544_H$	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
$00C548_H$	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
$00C54C_H$	IF2MCTR5 [R/W] 00000000 00000000		Reserved		
$00C550_H$	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
$00C554_H$	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
$00C558_H$ to $00C55C_H$	Reserved				
$00C560_H$	IF2DTA25 [R/W] 00000000 00000000		IF2DTA15 [R/W] 00000000 00000000		
$00C564_H$	IF2DTB25 [R/W] 00000000 00000000		IF2DTB15 [R/W] 00000000 00000000		
$00C568_H$ to $00C57C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags **Note:** Not on MB91F465BB/MB91F464BB
$00C584_H$ to $00C58C_H$	Reserved				
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
$00C594_H$ to $00C59C_H$	Reserved				
$00C5A0_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
$00C5A4_H$ to $00C5AC_H$	Reserved				
$00C5B0_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
$00C5B4_H$ to $00EFFC_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--000000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $01FFFC_H$	Reserved				EDSU / MPU
020000_H to $02FFFC_H$	D-RAM size is 24 Kbytes : $02A000_H$ - $02FFFC_H$ (data access is 0 wait cycles)				D-RAM area
030000_H to $03FFFC_H$	ID-RAM size is 16 Kbytes : 030000_H - $033FFC_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

1. depends on the number of available CAN channels

2. ACR0 [11 : 10] depends on Mode vector fetch information on bus width

3. TCR [3 : 0] INIT value = 0000, keeps value after RST

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) [5]	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception [5]	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
I^2C 0	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	—
I^2C 1	75	4B			$2D0_H$	$000FFED0_H$	—
Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
Reserved	89	59			298_H	$000FFE98_H$	77
Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Output Compare 5	105	69			258_H	$000FFE58_H$	93
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Output Compare 7	107	6B			250_H	$000FFE50_H$	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	—
Reserved	109	6D			248_H	$000FFE48_H$	—
System Reserved	110	6E	ICR47 [3]	$46F_H$	244_H	$000FFE44_H$	—
System Reserved	111	6F			240_H	$000FFE40_H$	—
PPG 0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG 1	113	71			238_H	$000FFE38_H$	97

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	64	47.6	97.6 Not on MB91F467BA/466BA
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9 Not on MB91F467BA/466BA
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9 Not on MB91F467BA/466BA
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7

15.3 DC Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	CMOS hysteresis input
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	-	V_{DD} + 0.3	V	4.5 V ? V_{DD} ? 5.5 V
				0.74 × V_{DD}	-	V_{DD} + 0.3	V	3 V ? V_{DD} < 4.5 V
		-	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	-	V_{DD} + 0.3	V	
		-	Port inputs if TTL input is selected	2.0	-	V_{DD} + 0.3	V	
	V_{IHR}	INITX	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	-	V_{DD} - 0.3	-	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	-	2.5	-	V_{DD} + 0.3	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	-	0.8 × V_{DD}	-	V_{DD} + 0.3	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	-	0.2 × V_{DD}	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	-	0.3 × V_{DD}	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	-	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} - 0.3	-	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		-	Port inputs if TTL input is selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILR}	INITX	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	-	V_{SS} - 0.3	-	0.5	V	External clock in "Oscillation mode"

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	-	V_{SS} - 0.3	-	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 1.6mA	V_{DD} - 0.5	-	-	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	
Output “L“ voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 1.6mA	-	-	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 3mA	-	-	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 3mA	-	-	0.4	V	
Input leakage current	I_{IL}	Pnn_m[1]	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	- 3	-	+ 3		
Analog input leakage current	I_{AIN}	ANn[2]	3.0V ≤ V_{DD} ≤ 5.5V T_A=25 °C	- 1	-	+ 1	mA	
			3.0V ≤ V_{DD} ≤ 5.5V T_A=125 °C	- 3	-	+ 3	mA	
Pull-up resistance	R_{UP}	Pnn_m [3] INITX	3.0V ≤ V_{DD} ≤ 3.6V	40	100	160	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m [4]	3.0V ≤ V_{DD} ≤ 3.6V	40	100	180	kW	
			4.5V ≤ V_{DD} ≤ 5.5V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	-	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	-	$AV_{CC}5$ × 0.25	V	
Power supply current per ADC macro [3]	I_A	$AV_{CC}5$	-	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	-	-	5	µA	A/D Converter not operated [1]
Reference voltage current per ADC macro [3]	I_R	AVRH5	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	-	-	5	µA	A/D Converter not operated [2]

1. Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5$ = AVRH = 5.0 V)
2. Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5$ = AVRH = 5.0 V)
3. The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation

T_{samp} = (2.6 kOhm + R_{EXT}) × 11pF × 7; for 4.5V ≤ $AV_{CC}5$ ≤ 5.5V

T_{samp} = (12.1 kOhm + R_{EXT}) × 11pF × 7; for 3.0V ≤ $AV_{CC}5$ ≤ 4.5V

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

15.4.1 Definition of A/D Converter Terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

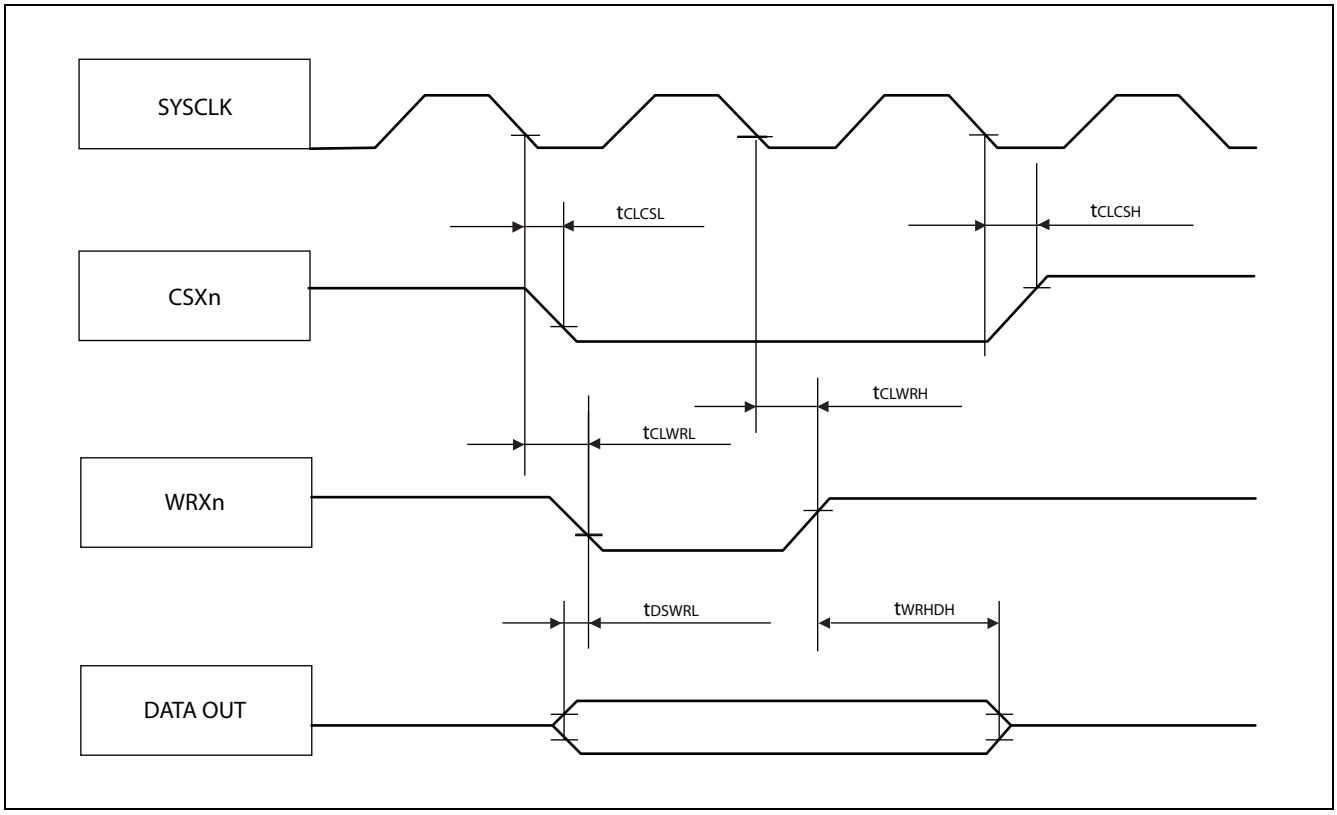
■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

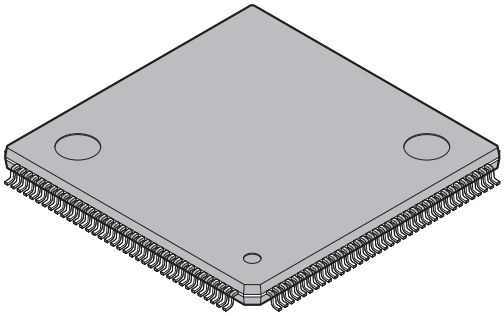
15.7.7.3 Synchronous write access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

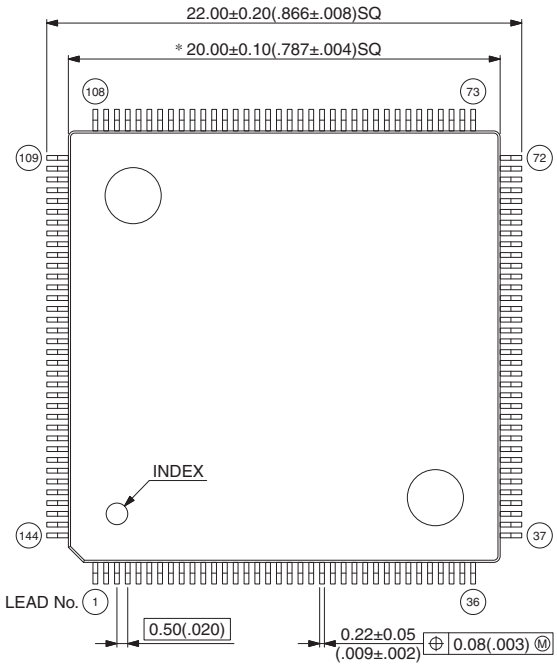
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	-	8	ns
	TCLWRH		0	-	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	- 7	-	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} - 20	-	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	-	8	ns
	TCLCSH		-	12	ns



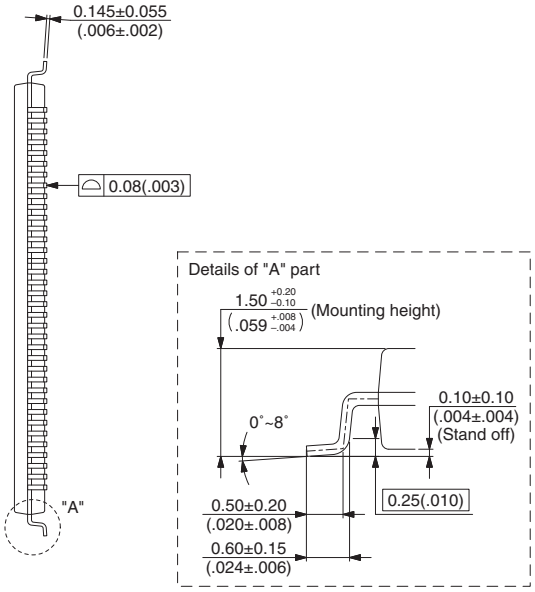
17. Package Dimension

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.