Infineon Technologies - MB91F467BAPMC-GSE2-W014 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w014

and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

- Clock modulator
- Clock monitor
- Sub-clock calibration
  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

Package and Technology

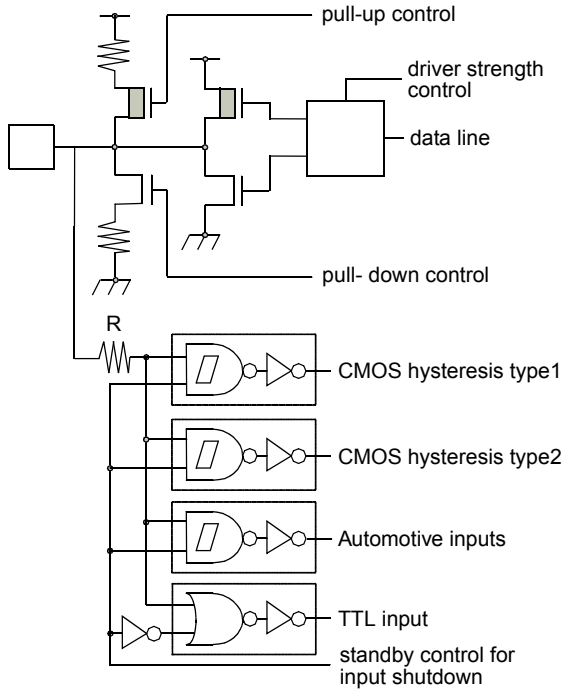
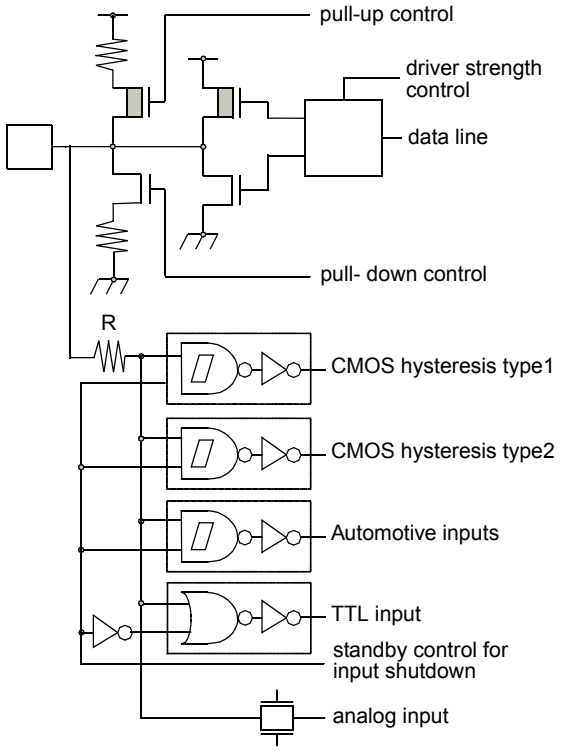
- Package: QFP-144
- CMOS 180 nm technology

- Main oscillator stabilization timer
  Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 125°C

3.2 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

9.3.2 Flash Access Timing Settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

9.3.2.1 Flash Read Timing Settings (Synchronous Read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F467BA/MB91F466BA

9.3.2.2 Flash Write Timing Settings (Synchronous Write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F467BA/MB91F466BA

9.3.3 Address Mapping from CPU to Parallel Programming Mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

9.3.3.1 Address Mapping MB91F467BA

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

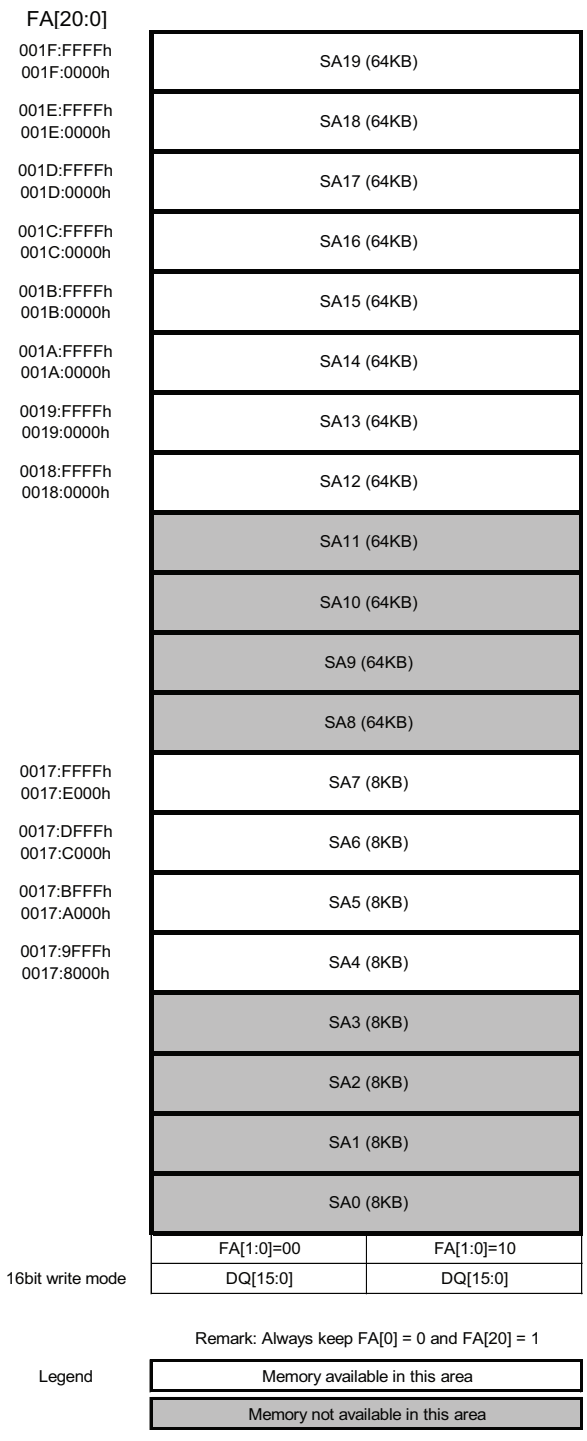
Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

9.3.3.2 Address Mapping MB91F466BA

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h
04:0000h to 0F:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 0F:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

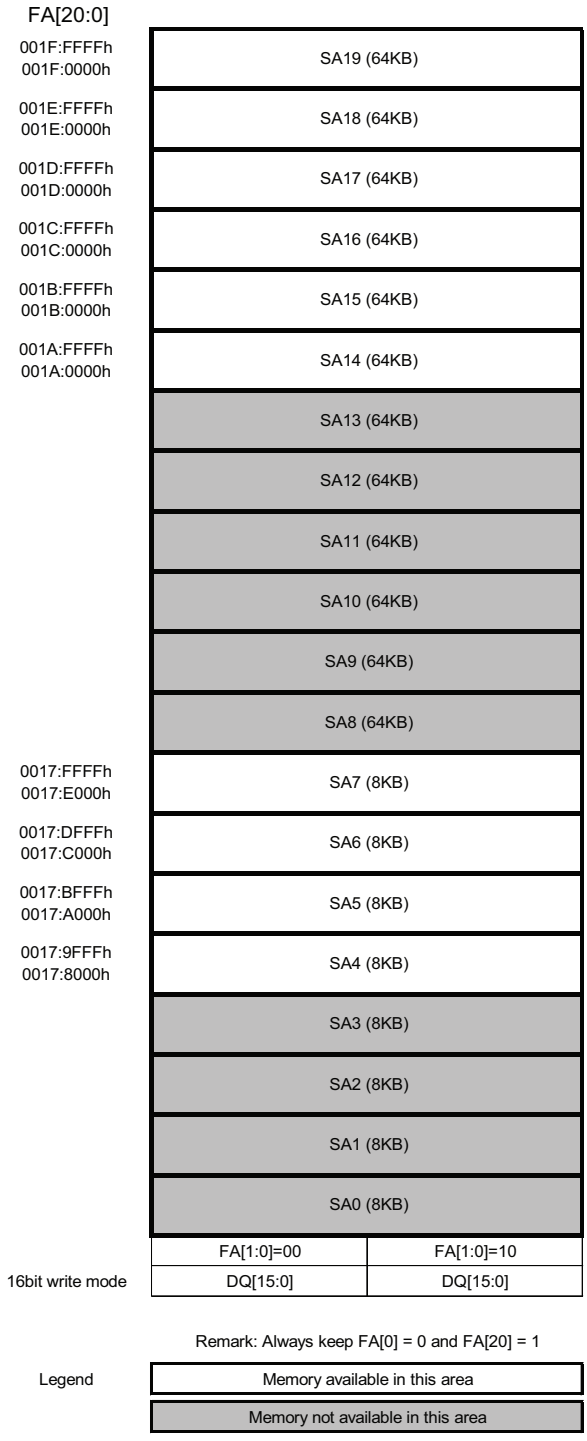
Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

MB91F465BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

MB91F464BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

9.6.3 Security Vector FSV2 MB91F467BA/466BA

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 5. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to “0”	set to “1”	
FSV2[1]	SA9	set to “0”	set to “1”	
FSV2[2]	SA10	set to “0”	set to “1”	
FSV2[3]	SA11	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[12]	SA20 (MB91F467BA)	set to “0”	set to “1”	
FSV2[13]	SA21 (MB91F467BA)	set to “0”	set to “1”	
FSV2[14]	SA22 (MB91F467BA)	set to “0”	set to “1”	
FSV2[15]	SA23 (MB91F467BA)	set to “0”	set to “1”	
FSV2[31:16]	–	set to “0”	set to “1”	not available

Note: See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.4 Security Vector FSV2 MB91F465BB/464BB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 6. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[3:0]	–	–	–	not available
FSV2[4]	SA12 (MB91F465BB)	set to “0”	set to “1”	
FSV2[5]	SA13 (MB91F465BB)	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	–	–	–	not available

Note: See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

Address	Register				Block
	+0	+1	+2	+3	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	Alarm Comparator 0 to 1
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34[R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control

Address	Register				Block
	+0	+1	+2	+3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$ to $000D3C_H$	Reserved				
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - -0	Reserved	
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D7C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000D80_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		R-bus Port Function Register
$000D84_H$	Reserved	PFR05 [R/W] - - 111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
$000D88_H$	PFR08 [R/W] 1 - - 1 - - 11	PFR09 [R/W] - - - - - - 11	PFR10 [R/W] - - - - - - - -1	Reserved	
$000D8C_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
$000D90_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - - - - - - 00	PFR22 [R/W] 0000-0-0	PFR23 [R/W] -0000000	
$000D98_H$	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$ to $000DC4_H$	Reserved				
$000DC8_H$	Reserved		EPFR10 [R/W] - - - - - - - 0	Reserved	R-bus Port Extra Function Register
$000DCC_H$	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
$000DD0_H$	EPFR16 [R/W] 0 - 00 - - - -	Reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
$000DD4_H$	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - - - - - - - -	Reserved		
$000DD8_H$	Reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
$000DDC_H$ to $000DFC_H$	Reserved				Reserved
$000E00_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
$000E04_H$	Reserved	PODR05 [R/W] - - 000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
$000E08_H$	PODR08 [R/W] 0 - - 0 - - - 0	PODR09 [R/W] - - - - - - 00	PODR10 [R/W] - - - - - - - 0	Reserved	
$000E0C_H$	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
$000E14_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - - - - - - 00	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
$000E18_H$	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
$000E20_H$ to $000E3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
$000E44_H$	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - - 00	PILR10 [R/W] - - - - - - - 0	Reserved	
$000E4C_H$	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
$000E58_H$	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
$000E60_H$ to $000E7C_H$	Reserved				Reserved
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
$000E84_H$	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 0 - - 0- - - 0	EPILR09 [R/W] - - - - - - 00	EPILR10 [R/W] - - - - - - - 0	Reserved	
$000E8C_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EBC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00C310_H$	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register **Note**: Not on MB91F465BB/MB91F464BB
$00C314_H$	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
$00C318_H$	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
$00C31C_H$	IF1MCTR3 [R/W] 00000000 00000000		Reserved		
$00C320_H$	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
$00C324_H$	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
$00C328_H$ to $00C32C_H$	Reserved				
$00C330_H$	IF1DTA23 [R/W] 00000000 00000000		IF1DTA13 [R/W] 00000000 00000000		
$00C334_H$	IF1DTB23 [R/W] 00000000 00000000		IF1DTB13 [R/W] 00000000 00000000		
$00C338_H$ to $00C33C_H$	Reserved				
$00C340_H$	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register **Note:** Not on MB91F465BB/MB91F464BB
$00C344_H$	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
$00C348_H$	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
$00C34C_H$	IF2MCTR3 [R/W] 00000000 00000000		Reserved		
$00C350_H$	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
$00C354_H$	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
$00C358_H$ to $00C35C_H$	Reserved				
$00C360_H$	IF2DTA23 [R/W] 00000000 00000000		IF2DTA13 [R/W] 00000000 00000000		
$00C364_H$	IF2DTB23 [R/W] 00000000 00000000		IF2DTB13 [R/W] 00000000 00000000		
$00C368_H$ to $00C37C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C380_H$	TREQR23 [R] 00000000 00000000		TREQR13 [R] 00000000 00000000		CAN 3 Status Flags **Note**: Not on MB91F465BB/MB91F464BB
$00C384_H$ to $00C38C_H$	Reserved				
$00C390_H$	NEWDT23 [R] 00000000 00000000		NEWDT13 [R] 00000000 00000000		
$00C394_H$ to $00C39C_H$	Reserved				
$00C3A0_H$	INTPND23 [R] 00000000 00000000		INTPND13 [R] 00000000 00000000		
$00C3A4_H$ to $00C3AC_H$	Reserved				
$00C3B0_H$	MSGVAL23 [R] 00000000 00000000		MSGVAL13 [R] 00000000 00000000		
$00C3B4_H$ to $00C3FC_H$	Reserved				
$00C400_H$	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register **Note**: Not on MB91F465BB/MB91F464BB
$00C404_H$	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
$00C408_H$	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
$00C40C_H$	BRPE4 [R/W] 00000000 00000000		CBSYNC4		
$00C410_H$	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register **Note:** Not on MB91F465BB/MB91F464BB
$00C414_H$	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
$00C418_H$	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
$00C41C_H$	IF1MCTR4 [R/W] 00000000 00000000		Reserved		
$00C420_H$	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
$00C424_H$	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
$00C428_H$ to $00C42C_H$	Reserved				
$00C430_H$	IF1DTA24 [R/W] 00000000 00000000		IF1DTA14 [R/W] 00000000 00000000		
$00C434_H$	IF1DTB24 [R/W] 00000000 00000000		IF1DTB14 [R/W] 00000000 00000000		
$00C438_H$ to $00C43C_H$	Reserved				

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
PPG 2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG 3	115	73			230_H	$000FFE30_H$	99
PPG 4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG 5	117	75			228_H	$000FFE28_H$	101
PPG 6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG 7	119	77			220_H	$000FFE20_H$	103
PPG 8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG 9	121	79			218_H	$000FFE18_H$	105
PPG 10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG 11	123	7B			210_H	$000FFE10_H$	107
PPG 12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG 13	125	7D			208_H	$000FFE08_H$	109
PPG 14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG 15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—
Reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Reserved	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
System reserved	135	87			$1E0_H$	$000FFDE0_H$	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Reserved	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
Reserved	139	8B			$1D0_H$	$000FFDD0_H$	—
Time base Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

1. The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
2. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.
3. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])
4. Used by REALOS
5. Memory Protection Unit (MPU) support

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9 Not on MB91F467BA/466BA
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6

15. Electrical Characteristics

15.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	–	–	50	V/ms	
Power supply voltage 1[1]	$V_{DD}5R$	– 0.3	+ 6.0	V	
Power supply voltage 2[1]	$V_{DD}5$	– 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output.
		$V_{SS}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	All pins of the Ports 26 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage[1]	$AV_{CC}5$	– 0.3	+ 6.0	V	[2]
Analog reference power supply voltage[1]	AVRH	– 0.3	+ 6.0	V	[2]
Input voltage 1[1]	V_{I1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Analog pin input voltage[1]	V_{IA}	AVss5 – 0.3	AVcc5 + 0.3	V	
Output voltage 1[1]	V_{O1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 4.0	+ 4.0	mA	[3]
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	–	20	mA	[3]
"L" level maximum output current[4]	I_{OL}	–	10	mA	
"L" level average output current[5]	I_{OLAV}	–	8	mA	
"L" level total maximum output current	ΣI_{OL}	–	100	mA	
"L" level total average output current[6]	ΣI_{OLAV}	–	50	mA	
"H" level maximum output current[4]	I_{OH}	–	– 10	mA	
"H" level average output current[5]	I_{OHAV}	–	– 4	mA	
"H" level total maximum output current	ΣI_{OH}	–	– 100	mA	
"H" level total average output current[6]	ΣI_{OHAV}	–	– 25	mA	
Permitted operating frequency MB91F465BB/F464BB	$f_{max, CLKB}$	–	100	MHz	$T_A \leq 105$ °C
	$f_{max, CLKP}$	–	50		
	$f_{max, CLKT}$	–	50		
	$f_{max, CLKCAN}$	–	50		
Permitted operating frequency MB91F465BB/F464BB	$f_{max, CLKB}$	–	96	MHz	$T_A \leq 125$ °C
	$f_{max, CLKP}$	–	48		
	$f_{max, CLKT}$	–	48		
	$f_{max, CLKCAN}$	–	48		
Permitted operating frequency MB91F467BA/F466BA	$f_{max, CLKB}$	–	96	MHz	$T_A \leq 105$ °C
	$f_{max, CLKP}$	–	48		
	$f_{max, CLKT}$	–	48		
	$f_{max, CLKCAN}$	–	48		

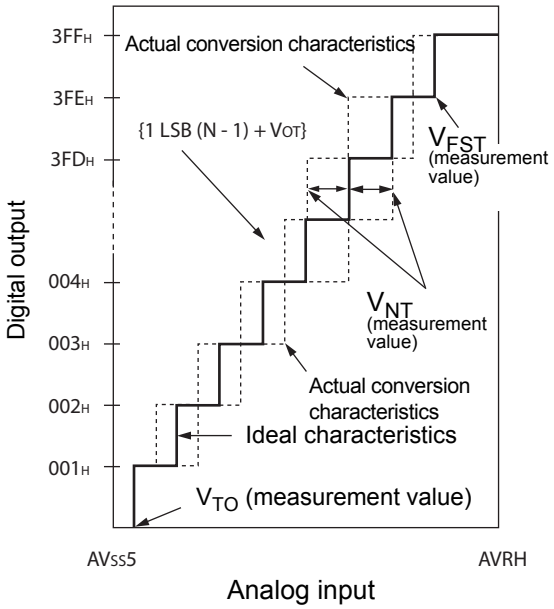
15.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

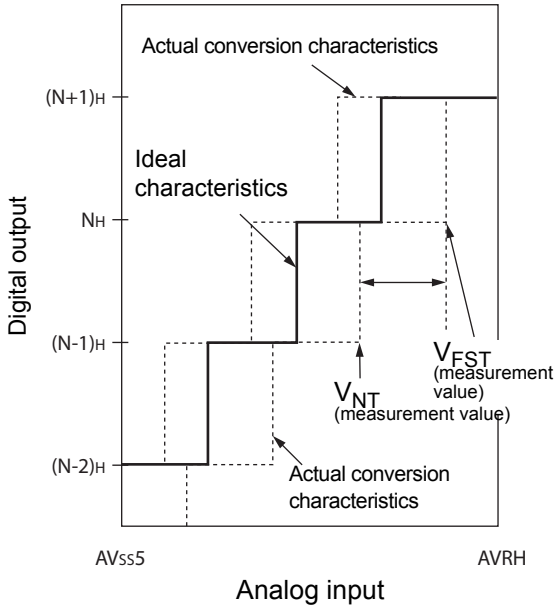
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	– 3	–	+ 3	LSB	
Nonlinearity error	–	–	– 2.5	–	+ 2.5	LSB	
Differential nonlinearity error	–	–	– 1.9	–	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	–	0.6	–	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	–	0.4	–	–	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	–	1.0	–	–	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	–	–	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	–	–	11	pF	
Input resistance	R_{IN}	ANn	–	–	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			–	–	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	– 1	–	+ 1	µA	T_A = + 25 °C
			– 3	–	+ 3	µA	T_A = + 125 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	–	AVRH	V	
Offset between input channels	–	ANn	–	–	4	LSB	

Note: The accuracy gets worse as AVRH - AVRL becomes smaller

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value
V_{OT}: Voltage at which the digital output changes from 000_H to 001_H.
V_{FST}: Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

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