

Welcome to **E-XFL.COM** 

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

| <b>Details</b> Product Status |  |
|-------------------------------|--|
|                               | Obsolete   |
| Core Processor                | FR60 RISC  |
| Core Size                     | 32-Bit Single-Core   |
| Speed                         | 96MHz  |
| Connectivity                  | CANbus, EBI/EMI, I <sup>2</sup> C, LINbus, UART/USART                              |
| Peripherals                   | DMA, LVD, PWM, WDT   |
| Number of I/O                 | 108  |
| Program Memory Size           | 1.0625MB (1.0625M x 8)   |
| Program Memory Type           | FLASH  |
| EEPROM Size                   | -  |
| RAM Size                      | 48K x 8  |
| Voltage - Supply (Vcc/Vdd)    | 3V ~ 5.5V  |
| Data Converters               | A/D 32x10b   |
| Oscillator Type               | External   |
| Operating Temperature         | -40°C ~ 125°C (TA)   |
| Mounting Type                 | Surface Mount  |
| Package / Case                | 144-LQFP   |
| Supplier Device Package       | 144-LQFP (20x20)   |
| Purchase URL                  | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w016 |

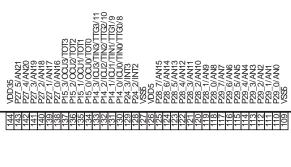
Email: info@E-XFL.COM

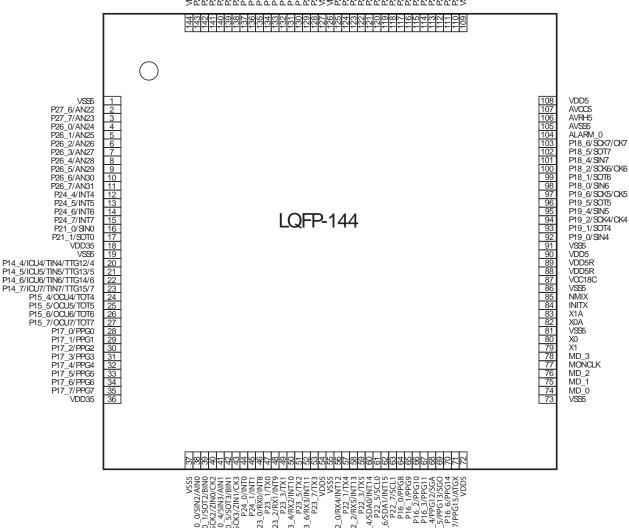
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### 2.2 MB91F467BA/466BA with MD 3=0

(TOP VIEW)





P20 0/SINZ/AINO
P20 1/SOTZ/BINO
P20 4/S/Z/NIN/CK2
P20 6/SC/Z/Z/NIN/CK2
P24 0/NIN/Z/IN/CK3
P24 0/NIN/Z/IN/CK3
P24 1/IN/T/Z
P23 4/R/Z/IN/T/Z
P23 4/R/Z/IN/T/Z
P23 4/R/Z/IN/T/Z
P23 4/R/Z/IN/T/Z
P23 4/R/Z/IN/T/Z
P22 4/S/Z/IN/T/Z
P22 5/S/CL
P16 1/PPGB
P16 3/PPGT/Z
P17 3/PPGT/Z P20\_ P20\_



| Pin no. | Pin name                       | I/O | I/O circuit type <sup>[1]</sup> | Function   |
|---------|--------------------------------|-----|---------------------------------|--|
|         | P23_2                          |     |                                 | General-purpose input/output port                        |
| 48      | RX1                            | I/O | A                               | RX input pin of CAN1                                     |
|         | INT9                           |     |                                 | External interrupt input pins                            |
| 49      | P23_3                          | I/O | A                               | General-purpose input/output port                        |
| 49      | TX1                            | 1/0 | ^                               | TX output pin of CAN1                                    |
|         | P23_4                          |     |                                 | General-purpose input/output port                        |
| 50      | RX2                            | I/O | Α                               | RX input pin of CAN2                                     |
|         | INT10                          |     |                                 | External interrupt input pin                             |
| 51      | P23_5                          | I/O | А                               | General-purpose input/output port                        |
| 31      | TX2                            | 1/0 | ^                               | TX output pin of CAN2                                    |
|         | P23_6                          |     |                                 | General-purpose input/output port                        |
| 52      | INT11                          | I/O | Α                               | External interrupt input pin                             |
|         | MB91F467BA/MB91F466<br>BA: RX3 |     |                                 | RX input pin of CAN3                                     |
|         | P23_7                          |     | А                               | General-purpose input/output port                        |
| 53      | MB91F467BA/MB91F466<br>BA: TX3 | I/O |                                 | TX output pin of CAN3                                    |
|         | P22_0                          | I/O | А                               | General-purpose input/output port                        |
| 56      | INT12                          |     |                                 | External interrupt input pin                             |
| 00      | MB91F467BA/MB91F466<br>BA: RX4 |     |                                 | RX input pin of CAN4                                     |
|         | P22_1                          |     | А                               | General-purpose input/output port                        |
| 57      | MB91F467BA/MB91F466<br>BA: TX4 | I/O |                                 | TX output pin of CAN4                                    |
|         | P22_2                          |     |                                 | General-purpose input/output port                        |
| 58      | INT13                          | I/O | Α                               | External interrupt input pin                             |
| 00      | MB91F467BA/MB91F466<br>BA: RX5 | "." |                                 | RX input pin of CAN5                                     |
|         | P22_3                          |     |                                 | General-purpose input/output port                        |
| 59      | MB91F467BA/MB91F466<br>BA: TX5 | I/O | A                               | TX output pin of CAN5                                    |
|         | P22_4                          |     |                                 | General-purpose input/output port                        |
| 60      | SDA0                           | I/O | С                               | I <sup>2</sup> C bus DATA input/output pin (open drain)  |
|         | INT14                          |     |                                 | External interrupt input pin                             |
| 61      | P22_5                          | I/O | С                               | General-purpose input/output port                        |
| 01      | SCL0                           | 1/0 |                                 | I <sup>2</sup> C bus clock input/output pin (open drain) |
|         | P22_6                          |     |                                 | General-purpose input/output port                        |
| 62      | SDA1                           | I/O | С                               | I <sup>2</sup> C bus DATA input/output pin (open drain)  |
|         | INT15                          |     |                                 | External interrupt input pin                             |
| 62      | P22_7                          | I/O | С                               | General-purpose input/output port                        |
| 63      | SCL1                           |     |                                 | I <sup>2</sup> C bus clock input/output pin (open drain) |



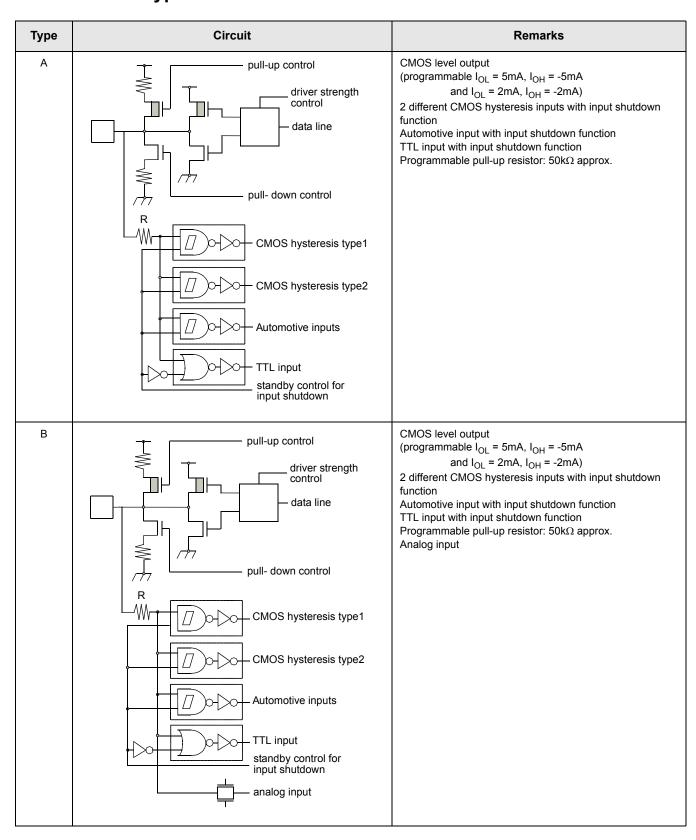
| Pin no.    | Pin name          | I/O   | I/O circuit type <sup>[1]</sup> | Function                                     |
|------------|-------------------|-------|---------------------------------|--|
| O.F.       | P19_4             | 1/0   | А                               | General-purpose input/output ports           |
| 95         | SIN5              | 1/0   | ^                               | Data input pin of USART5                     |
| 96         | P19_5             | I/O   |                                 | General-purpose input/output ports           |
| 90         | SOT5              | 1/0   | A                               | Data output pin of USART5                    |
|            | P19_6             |       |                                 | General-purpose input/output ports           |
| 97         | SCK5              | I/O   | Α                               | Clock input/output pin of USART5             |
|            | CK5               |       |                                 | External clock input pin of free-run timer 5 |
| 98         | P18_0             | 1/0   | ^                               | General-purpose input/output ports           |
| 98         | SIN6              | 1/0   | A                               | Data input pin of USART6                     |
| 00         | P18_1             | 1/0   |                                 | General-purpose input/output ports           |
| 99         | SOT6              | 1/0   | A                               | Data output pin of USART6                    |
|            | P18_2             |       |                                 | General-purpose input/output ports           |
| 100        | SCK6              | I/O   | Α                               | Clock input/output pin of USART6             |
|            | CK6               |       |                                 | External clock input pin of free-run timer 6 |
| 404        | P18_4             | I/O   | А                               | General-purpose input/output ports           |
| 101        | SIN7              |       |                                 | Data input pin of USART7                     |
| 400        | P18_5             | - I/O | А                               | General-purpose input/output ports           |
| 102        | SOT7              |       |                                 | Data output pin of USART7                    |
|            | P18_6             | I/O   | А                               | General-purpose input/output ports           |
| 103        | SCK7              |       |                                 | Clock input/output pin of USART7             |
|            | CK7               |       |                                 | External clock input pin of free-run timer 7 |
| 104        | ALARM_0           | I     | N                               | Alarm comparator input pin                   |
| 110 1- 117 | P29_0 to P29_7    |       | В                               | General-purpose input/output ports           |
| 110 to 117 | AN0 to AN7        | 1/0   |                                 | Analog input pins of A/D converter           |
| 110 += 105 | P28_0 to P28_7    | 1/0   | В                               | General-purpose input/output ports           |
| 118 to 125 | AN8 to AN15       | 1/0   |                                 | Analog input pins of A/D converter           |
| 400        | P24_2             | 1/0   | Δ.                              | General-purpose input/output ports           |
| 128        | INT2              | 1/0   | A                               | External interrupt input pin                 |
| 400        | P24_3             | 1/0   |                                 | General-purpose input/output ports           |
| 129        | INT3              | 1/0   | A                               | External interrupt input pin                 |
|            | P14_0 to P14_3    |       |                                 | General-purpose input/output ports           |
| 100 / 100  | ICU0 to ICU3      |       |                                 | Input capture input pins                     |
| 130 to 133 | TIN0 to TIN3      | I/O   | A                               | External trigger input pins of reload timer  |
|            | TTG0/8 to TTG3/11 | 1     |                                 | External trigger input pins of PPG timer     |
|            | P15_0 to P15_3    |       |                                 | General-purpose input/output ports           |
| 134 to 137 | OCU0 to OCU3      | I/O   | Α                               | Output compare output pins                   |
| ļ          | TOT0 to TOT3      | 1     |                                 | Reload timer output pins                     |
| 120 1- 110 | P27_0 to P27_5    | - 1/0 |                                 | General-purpose input/output ports           |
| 138 to 143 | AN16 to AN21      |       | В                               | Analog input pins of A/D converter           |

<sup>1.</sup> For information about the I/O circuit type, refer to "I/O Circuit Types".

Document Number: 002-04608 Rev. \*A



# 4. I/O Circuit Types





| Туре | Circuit           | Remarks   |
|------|-------------------|---|
| М    | tri-state control | CMOS level tri-state output (I <sub>OL</sub> = 5mA, I <sub>OH</sub> = -5mA) |
| N    | analog input line | Analog input pin with protection  |



# 5. Handling Devices

#### 5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than  $(V_{DD}5, V_{DD}35 \text{ or } HV_{DD}5^{[1]})$  or less than  $(V_{SS}5 \text{ or } HV_{SS}5^{[1]})$  is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

**Note:** 1.  $HV_{DD}$ 5,  $HV_{SS}$ 5 are available only on devices having Stepper Motor Controller.

### 5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor ( $2K\Omega$  to  $10K\Omega$ ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD\_x can be connected to  $V_{SS}5$  or  $V_{DD}5$  directly. Unused ALARM input pins can be connected to  $AV_{SS}5$  directly.

# 5.3 Power Supply Pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance. It is also recommended to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a bypass capacitor between power supply pin and ground pin near this device. This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7  $\mu$ F (use a X7R ceramic capacitator) to VCC18C pin for the regulator.

# 5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

# 5.5 Notes on using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Figure 1. Example of using opposite phase supply

X0 (X0A)

X1 (X1A)

Document Number: 002-04608 Rev. \*A Page 27 of 126



# 5.6 Mode Pins (MD\_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

# 5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

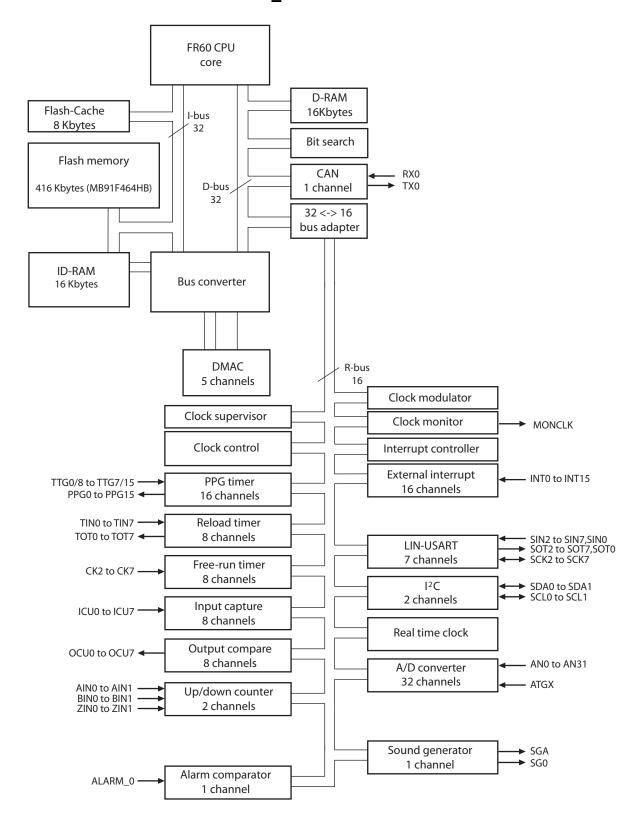
# 5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

Document Number: 002-04608 Rev. \*A Page 28 of 126



# 7.4 MB91F465BB/464BB with MD\_3=0





# 9.3.1.2 Flash Memory Map MB91F466BA

| Addr                     |                             |                 |                   |   |             |               |                  |        |       |
|--------------------------|-----------------------------|-----------------|-------------------|---|-------------|---------------|------------------|--------|-------|
| 0014:FFFFh<br>0014:C000h |                             | SA6             | (8KB)             |   | SA7 (8KB)   |               |                  |        |       |
| 0014:BFFFh<br>0014:8000h |                             | SA4             | (8KB)             |   | SA5 (8KB)   |               |                  |        | ROMS7 |
| 0014:7FFFh<br>0014:4000h |                             | SA2             | (8KB)             |   | SA3 (8KB)   |               |                  |        |       |
| 0014:3FFFh<br>0014:0000h |                             | SA0             | (8KB)             |   |             | SA1           | (8KB)            |        |       |
| 0013:FFFFh<br>0012:0000h |                             | SA22            | (64KB)            |   |             | SA23          | (64KB)           |        | ROMS6 |
| 0011:FFFFh<br>0010:0000h |                             | SA20            | (64KB)            |   | SA21 (64KB) |               |                  |        | KOW56 |
| 000F:FFFFh<br>000E:0000h |                             | SA18            | (64KB)            |   | SA19 (64KB) |               |                  | ROMS5  |       |
| 000D:FFFFh<br>000C:0000h |                             | SA16            | (64KB)            |   | SA17 (64KB) |               |                  | ROMS4  |       |
| 000B:FFFFh<br>000A:0000h |                             | SA14            | (64KB)            |   | SA15 (64KB) |               |                  | ROMS3  |       |
| 0009:FFFFh<br>0008:0000h |                             | SA12            | (64KB)            |   | SA13 (64KB) |               |                  | ROMS2  |       |
| 0007:FFFFh<br>0006:0000h |                             | SA10            | (64KB)            |   | SA11 (64KB) |               |                  | ROMS1  |       |
| 0005:FFFFh<br>0004:0000h | SA8 (64KB)                  |                 |                   |   | SA9 (64KB)  |               |                  |        | ROMS0 |
| '                        | addr+0 addr+1 addr+2 addr+3 |                 |                   |   | addr+4      | addr+5        | addr+6           | addr+7 |       |
| 16bit read/write         | dat[31:16] dat[15:0]        |                 |                   |   | dat[3       | 1:16]         | dat[             | 15:0]  |       |
| 32bit read               | dat[31:0] dat[31:0]         |                 |                   |   |             |               |                  |        |       |
| 64bit read               | dat[63:0]                   |                 |                   |   |             |               |                  |        |       |
| Legend                   | М                           | lemory not avai | lable in this are | a |             | Memory availa | ble in this area |        |       |



#### MB91F465BB

#### MB91F464BB

| FA[20:0]                 |             |            |  |  |  |  |  |
|--------------------------|-------------|------------|--|--|--|--|--|
| 001F:FFFFh<br>001F:0000h | SA19        | (64KB)     |  |  |  |  |  |
| 001E:FFFFh<br>001E:0000h | SA18        | (64KB)     |  |  |  |  |  |
| 001D:FFFFh<br>001D:0000h | SA17        | (64KB)     |  |  |  |  |  |
| 001C:FFFFh<br>001C:0000h | SA16 (64KB) |            |  |  |  |  |  |
| 001B:FFFFh<br>001B:0000h | SA15        | (64KB)     |  |  |  |  |  |
| 001A:FFFFh<br>001A:0000h | SA14        | (64KB)     |  |  |  |  |  |
| 0019:FFFFh<br>0019:0000h | SA13        | (64KB)     |  |  |  |  |  |
| 0018:FFFFh<br>0018:0000h | SA12        | (64KB)     |  |  |  |  |  |
|                          | SA11        | (64KB)     |  |  |  |  |  |
|                          | SA10 (64KB) |            |  |  |  |  |  |
|                          | SA9 (64KB)  |            |  |  |  |  |  |
|                          | SA8 (       | 64KB)      |  |  |  |  |  |
| 0017:FFFFh<br>0017:E000h | SA7 (8KB)   |            |  |  |  |  |  |
| 0017:DFFFh<br>0017:C000h | SA6         | (8KB)      |  |  |  |  |  |
| 0017:BFFFh<br>0017:A000h | SA5         | (8KB)      |  |  |  |  |  |
| 0017:9FFFh<br>0017:8000h | SA4         | (8KB)      |  |  |  |  |  |
|                          | SA3         | (8KB)      |  |  |  |  |  |
| SA2 (8KB)                |             |            |  |  |  |  |  |
|                          | (8KB)       |            |  |  |  |  |  |
|                          | SA0         | (8KB)      |  |  |  |  |  |
|                          | FA[1:0]=00  | FA[1:0]=10 |  |  |  |  |  |
| 16bit write mode         | DQ[15:0]    | DQ[15:0]   |  |  |  |  |  |
| . 13% milodo             | 2 %[10.0]   | 2 3 [10.0] |  |  |  |  |  |

| FA[20:0]                 |             |            |  |  |  |  |  |  |
|--------------------------|-------------|------------|--|--|--|--|--|--|
| 001F:FFFFh<br>001F:0000h | SA19        | (64KB)     |  |  |  |  |  |  |
| 001E:FFFFh<br>001E:0000h | SA18        | (64KB)     |  |  |  |  |  |  |
| 001D:FFFFh<br>001D:0000h | SA17 (64KB) |            |  |  |  |  |  |  |
| 001C:FFFFh<br>001C:0000h | SA16        | (64KB)     |  |  |  |  |  |  |
| 001B:FFFFh<br>001B:0000h | SA15        | (64KB)     |  |  |  |  |  |  |
| 001A:FFFFh<br>001A:0000h | SA14        | (64KB)     |  |  |  |  |  |  |
|                          | SA13        | (64KB)     |  |  |  |  |  |  |
|                          | SA12        | (64KB)     |  |  |  |  |  |  |
|                          | SA11 (64KB) |            |  |  |  |  |  |  |
|                          | SA10 (64KB) |            |  |  |  |  |  |  |
|                          | SA9 (64KB)  |            |  |  |  |  |  |  |
|                          | SA8 (64KB)  |            |  |  |  |  |  |  |
| 0017:FFFFh<br>0017:E000h | SA7         | (8KB)      |  |  |  |  |  |  |
| 0017:DFFFh<br>0017:C000h | SA6         | (8KB)      |  |  |  |  |  |  |
| 0017:BFFFh<br>0017:A000h | SA5         | (8KB)      |  |  |  |  |  |  |
| 0017:9FFFh<br>0017:8000h | SA4         | (8KB)      |  |  |  |  |  |  |
|                          | SA3         | (8KB)      |  |  |  |  |  |  |
|                          | SA2         | SA2 (8KB)  |  |  |  |  |  |  |
|                          | (8KB)       |            |  |  |  |  |  |  |
|                          | SA0         | (8KB)      |  |  |  |  |  |  |
|                          | FA[1:0]=00  | FA[1:0]=10 |  |  |  |  |  |  |
| 16bit write mode         | DQ[15:0]    | DQ[15:0]   |  |  |  |  |  |  |
|                          |             |            |  |  |  |  |  |  |

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

| Memory available in this area     |  |
|-----------------------------------|--|
| Memory not available in this area |  |

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

| Memory available in this area     |
|-----------------------------------|
| Memory not available in this area |



### 9.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

| MBM29LV400TCE xternal pins | FR-CPU mode   | MB91F4            | Comment                               |            |              |
|----------------------------|---|-------------------|---------------------------------------|------------|--------------|
|                            |   | Flash memory mode | Normal function                       | Pin number |              |
| -                          | INITX   | -                 | INITX                                 | 84         |              |
| RESET                      | -   | FRSTX             | GP16_6                                | 70         |              |
| -                          | -   | MD2               | MD2                                   | 76         | Set to '1'   |
| -                          | -   | MD1               | MD1                                   | 75         | Set to '1'   |
| -                          | -   | MD0               | MD0                                   | 74         | Set to '1'   |
| RY/BY                      | FMCS:RDY bit  | RY/BYX            | GP18_2                                | 100        |              |
| BYTE                       | Internally fixed to 'H'                                 | BYTEX             | GP16_4                                | 68         |              |
| WE                         |   | WEX               | GP16_7                                | 71         |              |
| OE                         |   | OEX               | GP07_7                                | 3          |              |
| CE                         |   | CEX               | GP07_6                                | 2          |              |
| -                          | Internal control signal + control via interface circuit | ATDIN             | GP18_6                                | 103        | Set to '0'   |
| -                          | Control via interface on out                            | EQIN              | GP18_5                                | 102        | Set to '0'   |
| -                          |   | TESTX             | GP16_5                                | 69         | Set to '1'   |
| -                          |   | RDYI              | GP18_4                                | 101        | Set to '0'   |
| A-1                        |   | FA0               | GP05_5                                | 17         | Set to '0'   |
| A0 to A3                   |   | FA1 to FA4        | GP19_0 to GP19_2,<br>GP19_4           | 92 to 95   |              |
| A4 to A7                   |   | FA5 to FA8        | GP19_5 to GP19_6,<br>GP18_0 to GP18_1 | 96 to 99   |              |
| A8 to A11                  | Internal address bus                                    | FA9 to FA12       | GP06_0 to GP06_3                      | 4 to 7     |              |
| A12 to A15                 |   | FA13 to FA16      | GP06_4 to GP06_7                      | 8 to 11    |              |
| A16 to A18                 |   | FA17 to FA19      | GP05_0 to GP05_2                      | 12 to 14   |              |
| A19                        |   | FA20              | GP05_3                                | 15         | See note [1] |
| -                          |   | FA21              | GP05_4                                | 16         | See note [2] |
| DQ0 to DQ7                 | lateman deta bus  | DQ0 to DQ7        | GP00_0 to GP00_7                      | 28 to 35   |              |
| DQ8 to DQ15                | Internal data bus                                       | DQ8 to DQ15       | GP01_0 to GP01_7                      | 20 to 27   |              |

<sup>1.</sup> A19 is used as address bit on MB91F467BA/F466BA. For MB91F465BB/F464BB, set this pin to '1'.

<sup>2.</sup> For MB91F467BA/F466BA, set this pin to '1'. For MB91F465BB/F464BB, this pin can be left open.



### 9.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

#### 9.6 Flash Security

#### 9.6.1 Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004 FSV2: 0x14:8008 BSV2: 0x14:800C

### 9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

#### 9.6.2.1 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2. Explanation of the bits in the Flash Security Vector FSV1[31:16]

| FSV1[31:19]    | FSV1[18]<br>Write Protection<br>Level | ection Write Protection Read Protection |            | Flash Security Mode   |
|----------------|---------------------------------------|---|------------|---|
| set all to '0' | set to '0'                            | set to '0'                              | set to '1' | Read Protection (all device modes, except INTVEC mode MD[2:0]="000")  |
| set all to '0' | set to '0'                            | set to '1'                              | set to '0' | Write Protection (all device modes, without exception)  |
| set all to '0' | set to '0'                            | set to '1'                              | set to '1' | Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes)                                  |
| set all to '0' | set to '1'                            | set to '0'                              | set to '1' | Read Protection (all device modes, except INTVEC mode MD[2:0]="000")  |
| set all to '0' | set to '1'                            | set to '1'                              | set to '0' | Write Protection (all device modes, except INTVEC mode MD[2:0]="000")   |
| set all to '0' | set to '1'                            | set to '1'                              | set to '1' | Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes except INTVEC mode MD[2:0]="000") |

Document Number: 002-04608 Rev. \*A Page 50 of 126



| Address                                       |   | Block                           |   |  |   |  |
|---|---|---------------------------------|---|--|---|--|
|   | +0  | +1                              | +2  | +3                                     |   |  |
| 000000 <sub>H</sub>                           | PDR00 [R/W]<br>XXXXXXXX   | PDR01 [R/W]<br>XXXXXXXX         | Reserved  | Reserved                               |   |  |
| 000004 <sub>H</sub>                           | Reserved  | PDR05 [R/W]<br>XXXXXX           | PDR06 [R/W]<br>XXXXXXXX                           |  |   |  |
| 000008 <sub>H</sub>                           | PDR08 [R/W]<br>X X X  | PDR09 [R/W]<br>XX               | PDR10 [R/W] Reserved                              |  |   |  |
| 00000C <sub>H</sub>                           | Reserved  | Reserved                        | PDR14 [R/W]<br>XXXXXXXX                           | xxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxx |   |  |
| 000010 <sub>H</sub>                           | PDR16 [R/W]<br>XXXXXXXX   | PDR17 [R/W]<br>XXXXXXXX         | PDR18 [R/W]<br>- XXX - XXX                        | PDR19 [R/W]<br>- XXX - XXX             | R-bus Port Data Register                |  |
| 000014 <sub>H</sub>                           | PDR20 [R/W]<br>- XXX - XXX  | PDR21 [R/W]<br>XX               | PDR22 [R/W]<br>XXXXXXXX                           | PDR23 [R/W]<br>XXXXXXXX                |   |  |
| 000018 <sub>H</sub>                           | PDR24 [R/W]<br>XXXXXXXX   | Reserved                        | PDR26 [R/W]<br>XXXXXXXX                           | PDR27 [R/W]<br>XXXXXXXX                |   |  |
| 00001C <sub>H</sub>                           | PDR28 [R/W]<br>XXXXXXXX   | PDR29 [R/W]<br>XXXXXXXX         | Reserved  | Reserved                               |   |  |
| 000020 <sub>H</sub> to<br>00002C <sub>H</sub> |   | Rese                            | erved   |  |   |  |
| 000030 <sub>H</sub>                           | EIRR0 [R/W]<br>MB91F467BA:<br>00000000:MD3=0<br>11110000:MD3=1<br>MB91F465BB:<br>XXXXXXXX | ENIR0 [R/W]<br>00000000         | ELVR0 [R/W]<br>000000000 000000000                |  | External interrupt<br>(INT 0 to INT 7)  |  |
| 000034 <sub>H</sub>                           | EIRR1 [R/W]<br>MB91F467BA:<br>00000000<br>MB91F465BB:<br>XXXXXXXX                         | ENIR1 [R/W]<br>00000000         | ELVR1 [R/W]<br>00000000 00000000                  |  | External interrupt<br>(INT 8 to INT 15) |  |
| 000038 <sub>H</sub>                           | DICR [R/W]<br>0   | HRCL [R/W]<br>0 11111           | RBS   | SYNC                                   | Delay interrupt                         |  |
| 00003C <sub>H</sub>                           |   | Rese                            | erved   |  | Reserved                                |  |
| 000040 <sub>H</sub>                           | SCR00 [R/W,W]<br>00000000   | SMR00 [R/W,W]<br>00000000       | SSR00 [R/W,R]<br>00001000                         | RDR00/TDR00 [R/W]<br>00000000          |   |  |
| 000044 <sub>H</sub>                           | ESCR00 [R/W]<br>00000X00  | ECCR00<br>[R/W,R,W]<br>-00000XX | Reserved  |  | LIN-USART 0                             |  |
| 000048 <sub>H</sub><br>00004C <sub>H</sub>    |   | Rese                            | Reserved  |  |   |  |
| 000050 <sub>H</sub>                           | SCR02 [R/W,W]<br>00000000   | SMR02 [R/W,W]<br>00000000       | SSR02 [R/W,R] RDR02/TDR02 [R/W] 00001000 00000000 |  |   |  |
| 000054 <sub>H</sub>                           | ESCR02 [R/W]<br>00000X00  | ECCR02<br>[R/W,R,W]<br>-00000XX | Reso  | erved                                  | LIN-USART 2                             |  |



| Address                                       |  | Block                   |                                 |                            |                      |  |
|---|--|-------------------------|---------------------------------|----------------------------|----------------------|--|
|   | +0   | +1                      | +2 +3                           |                            |                      |  |
| 000D00 <sub>H</sub>                           | DD00 <sub>H</sub> PDRD00 [R] PDRD01 [R] XXXXXXXX |                         | Reserved                        |                            |                      |  |
| 000D04 <sub>H</sub>                           | Reserved   | PDRD05 [R]<br>XXXXXX    | PDRD06 [R]<br>XXXXXXXX          | PDRD07 [R]<br>XXXXXXXX     |                      |  |
| 000D08 <sub>H</sub>                           | PDRD08 [R]<br>X XX                               | PDRD09 [R]<br>XX        | PDRD10 [R]<br>X                 | Reserved                   |                      |  |
| 000D0C <sub>H</sub>                           | Rese   | erved                   | PDRD14 [R] PDRD15 [R] XXXXXXXXX |                            | R-bus Port Data      |  |
| 000D10 <sub>H</sub>                           | PDRD16 [R]<br>XXXXXXXX                           | PDRD17 [R]<br>XXXXXXXX  | PDRD18 [R]<br>- XXX - XXX       | PDRD19 [R]<br>- XXX - XXX  | Direct Read Register |  |
| 000D14 <sub>H</sub>                           | PDRD20 [R]<br>- XXX - XXX                        | PDRD21 [R]<br>X         | PDRD22 [R]<br>XXXXXXXX          | PDRD23 [R]<br>XXXXXXXX     |                      |  |
| 000D18 <sub>H</sub>                           | PDRD24 [R]<br>XXXXXXXX                           | Reserved                | PDRD26 [R]<br>XXXXXXXX          | PDRD27 [R]<br>XXXXXXXX     |                      |  |
| 000D1C <sub>H</sub>                           | PDRD28 [R]<br>XXXXXXXX                           |                         |                                 |                            |                      |  |
| 000D20 <sub>H</sub> to<br>000D3C <sub>H</sub> |  |                         |                                 |                            |                      |  |
| 000D40 <sub>H</sub>                           | DDR00 [R/W] DDR01 [R/W] 000000000 000000000      |                         | Reserved                        |                            |                      |  |
| 000D44 <sub>H</sub>                           | Reserved   | DDR05 [R/W]<br>000000   | DDR06 [R/W]<br>00000000         | DDR07 [R/W]<br>00000000    |                      |  |
| 000D48 <sub>H</sub>                           | DDR08 [R/W]<br>0 00                              | DDR09 [R/W]<br>00       | DDR10 [R/W]                     | Reserved                   |                      |  |
| 000D4C <sub>H</sub>                           | Rese   | erved                   | DDR14 [R/W]<br>00000000         | DDR15 [R/W]<br>00000000    | R-bus Port Direction |  |
| 000D50 <sub>H</sub>                           | DDR16 [R/W]<br>00000000                          | DDR17 [R/W]<br>00000000 | DDR18 [R/W]<br>- 000 - 000      | DDR19 [R/W]<br>- 000 - 000 | Register             |  |
| 000D54 <sub>H</sub>                           | DDR20 [R/W]<br>- 000 - 000                       | DDR21 [R/W]             | DDR22 [R/W]<br>00000000         | DDR23 [R/W]<br>00000000    |                      |  |
| 000D58 <sub>H</sub>                           | DDR24 [R/W] Reserved                             |                         | DDR26 [R/W]<br>00000000         | DDR27 [R/W]<br>00000000    |                      |  |
| 000D5C <sub>H</sub>                           | DDR28 [R/W] DDR29 [R/W] 000000000 000000000      |                         | Reserved                        |                            |                      |  |
| 000D60 <sub>H</sub> to<br>000D7C <sub>H</sub> |  | Reserved                |                                 |                            |                      |  |



| Address                                       |   |   | Block                                       |                              |                        |  |
|---|---|---|---|------------------------------|------------------------|--|
|   | +0  | +1  | +2 +3                                       |                              |                        |  |
| 000E40 <sub>H</sub>                           | PILR00 [R/W] PILR01 [R/W] 000000000 000000000   |   | Reserved                                    |                              |                        |  |
| 000E44 <sub>H</sub>                           | Reserved  | PILR05 [R/W] PILR06 [R/W] 0000000 000000000 |   | PILR07 [R/W]<br>00000000     |                        |  |
| 000E48 <sub>H</sub>                           | PILR08 [R/W]<br>0 0 0                           | PILR09 [R/W]<br>00                          | PILR10 [R/W]                                | Reserved                     |                        |  |
| 000E4C <sub>H</sub>                           | Rese  | ved   | PILR14 [R/W] PILR15 [R/W] 00000000 00000000 |                              | R-bus Port Input Level |  |
| 000E50 <sub>H</sub>                           | PILR16 [R/W]<br>00000000                        | PILR17 [R/W]<br>00000000                    | PILR18 [R/W]<br>000                         | PILR19 [R/W]<br>- 000 - 000  | Select Register        |  |
| 000E54 <sub>H</sub>                           | PILR20 [R/W]<br>- 000 - 000                     | PILR21 [R/W]<br>00                          | PILR22 [R/W]<br>00000000                    | PILR23 [R/W]<br>00000000     |                        |  |
| 000E58 <sub>H</sub>                           | PILR24 [R/W]<br>00000000                        | Reserved                                    | PILR26 [R/W]<br>00000000                    | PILR27 [R/W]<br>00000000     |                        |  |
| 000E5C <sub>H</sub>                           | PILR28 [R/W] PILR29 [R/W] Reserved              |   |   |                              |                        |  |
| 000E60 <sub>H</sub><br>to 000E7C <sub>H</sub> |   | Reserved                                    |   |                              |                        |  |
| 000E80 <sub>H</sub>                           | EPILR00 [R/W] EPILR01 [R/W] 000000000 000000000 |   | Reserved                                    |                              |                        |  |
| 000E84 <sub>H</sub>                           | Reserved  | EPILR05 [R/W]<br>000000                     | EPILR06 [R/W]<br>00000000                   | EPILR07 [R/W]<br>00000000    |                        |  |
| 000E88 <sub>H</sub>                           | EPILR08 [R/W]<br>0 0 0                          | EPILR09 [R/W]<br>00                         | EPILR10 [R/W]<br>0                          | Reserved                     |                        |  |
| 000E8C <sub>H</sub>                           | Rese  | ved   | EPILR14 [R/W]<br>00000000                   | EPILR15 [R/W]<br>00000000    | R-bus Port Extra Input |  |
| 000E90 <sub>H</sub>                           | EPILR16 [R/W]<br>00000000                       | EPILR17 [R/W]<br>00000000                   | EPILR18 [R/W]<br>000                        | EPILR19 [R/W]<br>- 000 - 000 | Level Select Register  |  |
| 000E94 <sub>H</sub>                           | EPILR20 [R/W]<br>- 000 - 000                    | EPILR21 [R/W]                               | EPILR22 [R/W]<br>00000000                   | EPILR23 [R/W]<br>00000000    |                        |  |
| 000E98 <sub>H</sub>                           | EPILR24 [R/W]<br>00000000                       | Reserved                                    | EPILR26 [R/W]<br>00000000                   | EPILR27 [R/W]<br>00000000    |                        |  |
| 000E9C <sub>H</sub>                           | EPILR28 [R/W] EPILR29 [R/W] 00000000 00000000   |   | Reserved                                    |                              |                        |  |
| 000EA0 <sub>H</sub><br>to 000EBC <sub>H</sub> | Reserved  |   |   |                              | Reserved               |  |



| Address                                       |                                   | Block |                                   |                                  |   |
|---|-----------------------------------|-------|-----------------------------------|----------------------------------|---|
|   | +0                                | +1    | +2                                | +3                               |   |
| 00C280 <sub>H</sub>                           | TREQR<br>00000000                 |       |                                   | TREQR12 [R]<br>00000000 00000000 |   |
| 00C284 <sub>H</sub> to<br>00C28C <sub>H</sub> | Rese                              | ved   | Res                               | Reserved                         |   |
| 00C290 <sub>H</sub>                           | NEWDT<br>00000000                 |       |                                   | NEWDT12 [R]<br>00000000 00000000 |   |
| 00C294 <sub>H</sub> to<br>00C29C <sub>H</sub> | Rese                              | ved   | Res                               | Reserved                         |   |
| 00C2A0 <sub>H</sub>                           | INTPNE<br>00000000                |       | INTPND12 [R]<br>00000000 00000000 |                                  |   |
| 00C2A4 <sub>H</sub> to<br>00C2AC <sub>H</sub> | Rese                              | ved   | Reserved                          |                                  |   |
| 00C2B0 <sub>H</sub>                           | MSGVA<br>00000000                 | • •   | MSGVAL12 [R]<br>00000000 00000000 |                                  |   |
| 00C2B4 <sub>H</sub> to<br>00C2FC <sub>H</sub> |                                   | Res   | erved                             |                                  | Reserved                                  |
| 00C300 <sub>H</sub>                           | CTRLR3 [R/W]<br>00000000 00000001 |       |                                   | R3 [R/W]<br>00000000             | CAN 3                                     |
| 00C304 <sub>H</sub>                           | ERRCNT3 [R]<br>00000000 00000000  |       | BTR3 [R/W]<br>00100011 00000001   |                                  | Control Register                          |
| 00C308 <sub>H</sub>                           | INTR3 [R]<br>00000000 00000000    |       | TESTR3 [R/W]<br>00000000 X0000000 |                                  | Note: Not on<br>MB91F465BB/MB91F464<br>BB |
| 00C30C <sub>H</sub>                           | BRPE3<br>00000000                 |       | CBS                               | YNC3                             | ВВ  |



| Address  |   | Block                |                                     |                                     |   |
|--|---|----------------------|-------------------------------------|-------------------------------------|---|
|  | +0  | +1                   | +2                                  | +3                                  |   |
| 00C380 <sub>H</sub>                              | TREQR23 [R] TREQR13 [R] 000000000 000000000 000000000 |                      |                                     |                                     |   |
| 00C384 <sub>H</sub> to<br>00C38C <sub>H</sub>    |   |                      |                                     |                                     |   |
| 00C390 <sub>H</sub>                              |   | T23 [R]<br>00000000  |                                     | DT13 [R]<br>0 00000000              | CAN 3                                     |
| 00C394 <sub>H</sub> to<br>00C39C <sub>H</sub>    |   | Res                  | erved                               |                                     | Status Flags                              |
| 00C3A0 <sub>H</sub>                              |   | D23 [R]<br>00000000  |                                     | ND13 [R]<br>0 00000000              | Note: Not on<br>MB91F465BB/MB91F464<br>BB |
| 00C3A4 <sub>H</sub> to<br>00C3AC <sub>H</sub>    |   | Res                  | erved                               |                                     | DD  |
| 00C3B0 <sub>H</sub>                              |   | AL23 [R]<br>00000000 |                                     | 'AL13 [R]<br>0 00000000             |   |
| 00C3B4 <sub>H</sub><br>to 00C3FC <sub>H</sub>    |   | Res                  | erved                               |                                     |   |
| 00C400 <sub>H</sub>                              |   | 84 [R/W]<br>00000001 |                                     | R4 [R/W]<br>0 00000000              | 24114                                     |
| 00C404 <sub>H</sub>                              |   | NT4 [R]<br>00000000  |                                     | 4 [R/W]<br>00000001                 | CAN 4 Control Register                    |
| 00C408 <sub>H</sub>                              |   | R4 [R]<br>00000000   | TEST<br>00000000                    | Note: Not on<br>MB91F465BB/MB91F464 |   |
| 00C40C <sub>H</sub>                              |   | 4 [R/W]<br>00000000  | CBS                                 | SYNC4                               | BB  |
| 00C410 <sub>H</sub>                              |   | Q4 [R/W]<br>00000001 |                                     | SK4 [R/W]<br>0 00000000             |   |
| 00C414 <sub>H</sub>                              |   | 24 [R/W]<br>11111111 | IF1MSK14 [R/W]<br>11111111 11111111 |                                     |   |
| 00C418 <sub>H</sub>                              |   | 24 [R/W]<br>00000000 |                                     | 314 [R/W]<br>0 00000000             |   |
| 00C41C <sub>H</sub>                              |   | R4 [R/W]<br>00000000 | Res                                 | served                              |   |
| 00C420 <sub>H</sub>                              |   | 14 [R/W]<br>00000000 |                                     | A24 [R/W]<br>0 00000000             | CAN 4 IF 1 Register                       |
| 00C424 <sub>H</sub>                              |   | 14 [R/W]<br>00000000 |                                     | 324 [R/W]<br>0 00000000             | Note: Not on                              |
| 00C428 <sub>H</sub><br>to<br>00C42C <sub>H</sub> | Reserved  |                      |                                     |                                     | MB91F465BB/MB91F464<br>BB                 |
| 00C430 <sub>H</sub>                              |   | 24 [R/W]<br>00000000 |                                     | A14 [R/W]<br>0 00000000             |   |
| 00C434 <sub>H</sub>                              |   | 24 [R/W]<br>00000000 | IF1DTB14 [R/W]<br>00000000 00000000 |                                     |   |
| 00C438 <sub>H</sub><br>to<br>00C43C <sub>H</sub> | Reserved  |                      |                                     |                                     |   |



# 15.7.4 $I^{2}C$ AC Timings at $V_{DD}5 = 3.0$ to 5.5 V

■ Conditions during AC measurements
All AC tests were measured under the following conditions:

 $\Box$  -IO<sub>drive</sub> = 3 mA

 $\Box$  -V<sub>DD</sub>5 = 3.0 V to 5.5 V, I<sub>load</sub> = 3 mA

□ -V<sub>SS</sub>5 = 0 V □ -Ta = -40 °C to + 125 °C

 $\Box$  -C<sub>I</sub> = 50 pF

 $\Box$  -VOL = 0.3 ×  $V_{DD}$ 5

 $\Box$  -VOH = 0.7 ×  $V_{DD}$ 5

 $\Box$  -EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 ×  $V_{DD}5/0.7 \times V_{DD}5$ )

#### 15.7.4.1 Fast mode:

(V\_DD5 = 3.5 V to 5.5 V, V\_SS5 = AV\_SS5 = 0 V, T\_A = -40 °C to  $\,$  + 125 °C)

| Parameter  | Symbol Pin name     |            | Value      |                            | Unit | Domonik |
|--|---------------------|------------|------------|----------------------------|------|---------|
| Parameter  | Symbol              | Pin name   | Min        | Max                        | Unit | Remark  |
| SCL clock frequency  | f <sub>SCL</sub>    | SCLn       | 0          | 400                        | kHz  |         |
| Hold time (repeated) START condition.<br>After this period, the first clock pulse is generated | t <sub>HD;STA</sub> | SCLn, SDAn | 0.6        | _                          | μ\$  |         |
| LOW period of the SCL clock  | t <sub>LOW</sub>    | SCLn       | 1.3        | =                          | μ\$  |         |
| HIGH period of the SCL clock   | t <sub>HIGH</sub>   | SCLn       | 0.6        | =                          | μ\$  |         |
| Setup time for a repeated START condition  | t <sub>SU;STA</sub> | SCLn, SDAn | 0.6        | -                          | μS   |         |
| Data hold time for I <sup>2</sup> C-bus devices  | t <sub>HD;DAT</sub> | SCLn, SDAn | 0          | 0.9                        | μS   |         |
| Data setup time  | t <sub>SU;DAT</sub> | SCLn SDAn  | 100        | =                          | ns   |         |
| Rise time of both SDA and SCL signals  | t <sub>r</sub>      | SCLn, SDAn | 20 + 0.1Cb | 300                        | ns   |         |
| Fall time of both SDA and SCL signals  | t <sub>f</sub>      | SCLn, SDAn | 20 + 0.1Cb | 300                        | ns   |         |
| Setup time for STOP condition  | t <sub>SU;STO</sub> | SCLn, SDAn | 0.6        | -                          | μS   |         |
| Bus free time between a STOP and START condition   | t <sub>BUF</sub>    | SCLn, SDAn | 1.3        | -                          | μ\$  |         |
| Capacitive load for each bus line  | C <sub>b</sub>      | SCLn, SDAn | -          | 400                        | pF   |         |
| Pulse width of spike suppressed by input filter  | t <sub>SP</sub>     | SCLn, SDAn | 0          | (11.5) × t <sub>CLKP</sub> | ns   | [1]     |

<sup>1.</sup> The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I<sup>2</sup>C signals (SDA, SCL) and peripheral clock.

**Note:**  $t_{CLKP}$  is the cycle time of the peripheral clock.

Document Number: 002-04608 Rev. \*A



# **Document History**

|  | Document Title: MB91F467BA/466BA, MB91F465BB/464BB, FR60 MB91460B Series, 32-bit Microcontroller Datasheet Document Number: 002-04608 |      |                       |  |  |  |
|--|---|------|-----------------------|--|--|--|
| Revision ECN Orig. of Change Submission Date |   |      | Description of Change |  |  |  |
| **   | _   | AKIH | 08/17/2009            | Migrated to Cypress and assigned document number 002-04608.<br>No change to document contents or format. |  |  |
| *A   | 5221423   | AKIH | 04/25/2016            | Updated to Cypress template  |  |  |

Document Number: 002-04608 Rev. \*A Page 125 of 126



#### Sales, Solutions, and Legal Information

#### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

cypress.com/usb

cypress.com/wireless

#### **Products**

**USB Controllers** 

Wireless/RF

ARM® Cortex® Microcontrollers cypress.com/arm Automotive cypress.com/automotive Clocks & Buffers cypress.com/clocks Interface cypress.com/interface Lighting & Power Control cypress.com/powerpsoc Memory cypress.com/memory **PSoC** cypress.com/psoc Touch Sensing cypress.com/touch

#### PSoC<sup>®</sup>Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

#### **Cypress Developer Community**

Forums | Projects | Video | Blogs | Training | Components

#### **Technical Support**

cypress.com/support

ARM and Cortex are the trademarks of ARM Limited in the EU and other countries

© Cypress Semiconductor Corporation 2009-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you under its copyright rights in the Software, a personal, non-exclusive, nontransferable license (without the right to sublicense) (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units. Cypress also grants you a personal, non-exclusive, nontransferable, license (without the right to sublicense) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely to the minimum extent that is necessary for you to exercise your rights under the copyright license granted in the previous sentence. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and Company shall and hereby does release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. Company shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.