Infineon Technologies - MB91F467BAPMC-GSE2-W019 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

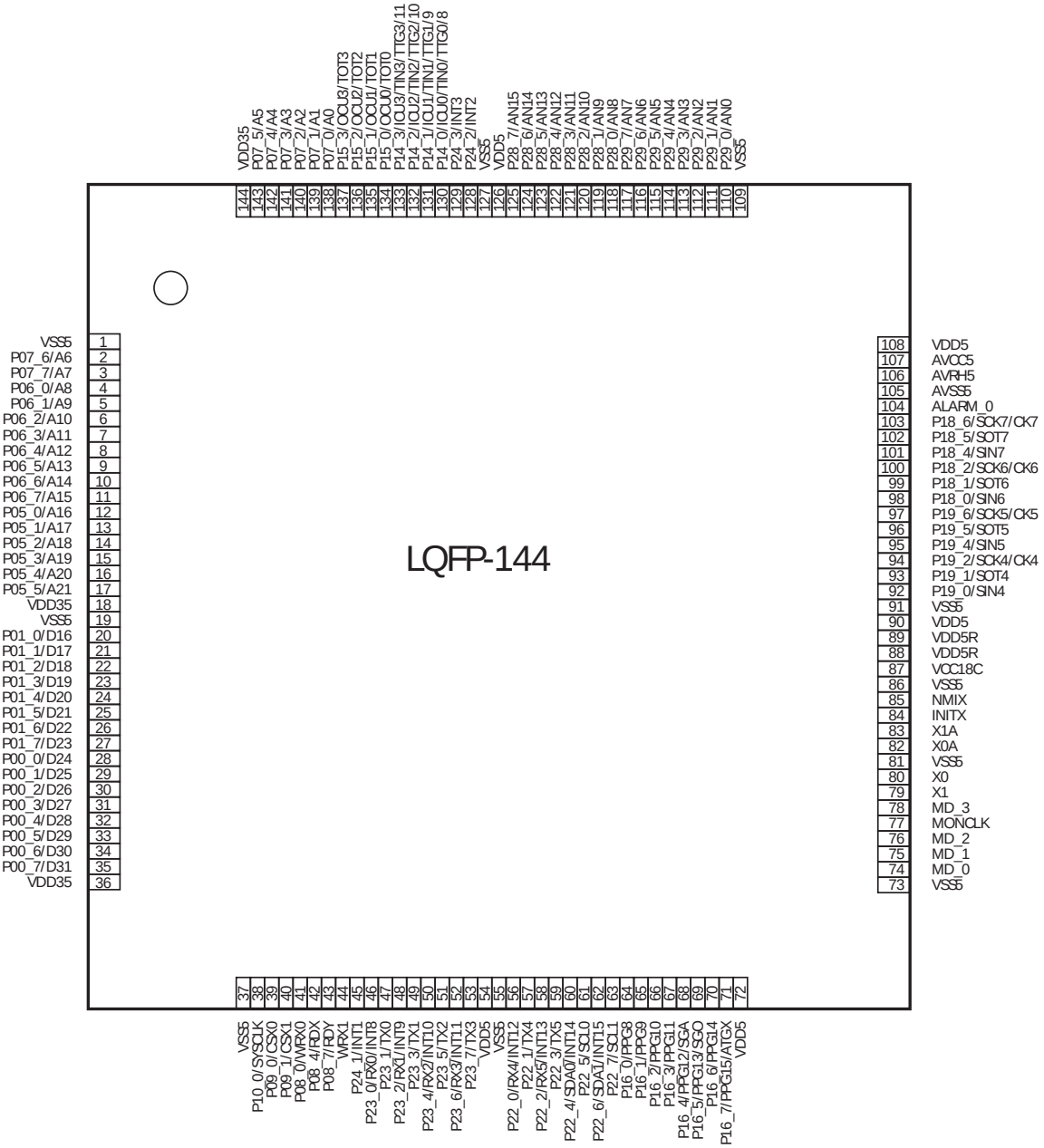
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w019

2. Pin Assignment

2.1 MB91F467BA/466BA with MD_3=1

(TOP VIEW)



3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466BA			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
97	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	O	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output port
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output port
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output port
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output port
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output port
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P07_0 to P07_5	I/O	B	General-purpose input/output port
	A0 to A5			Signal pins of external address bus (bit0 to bit5)

5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

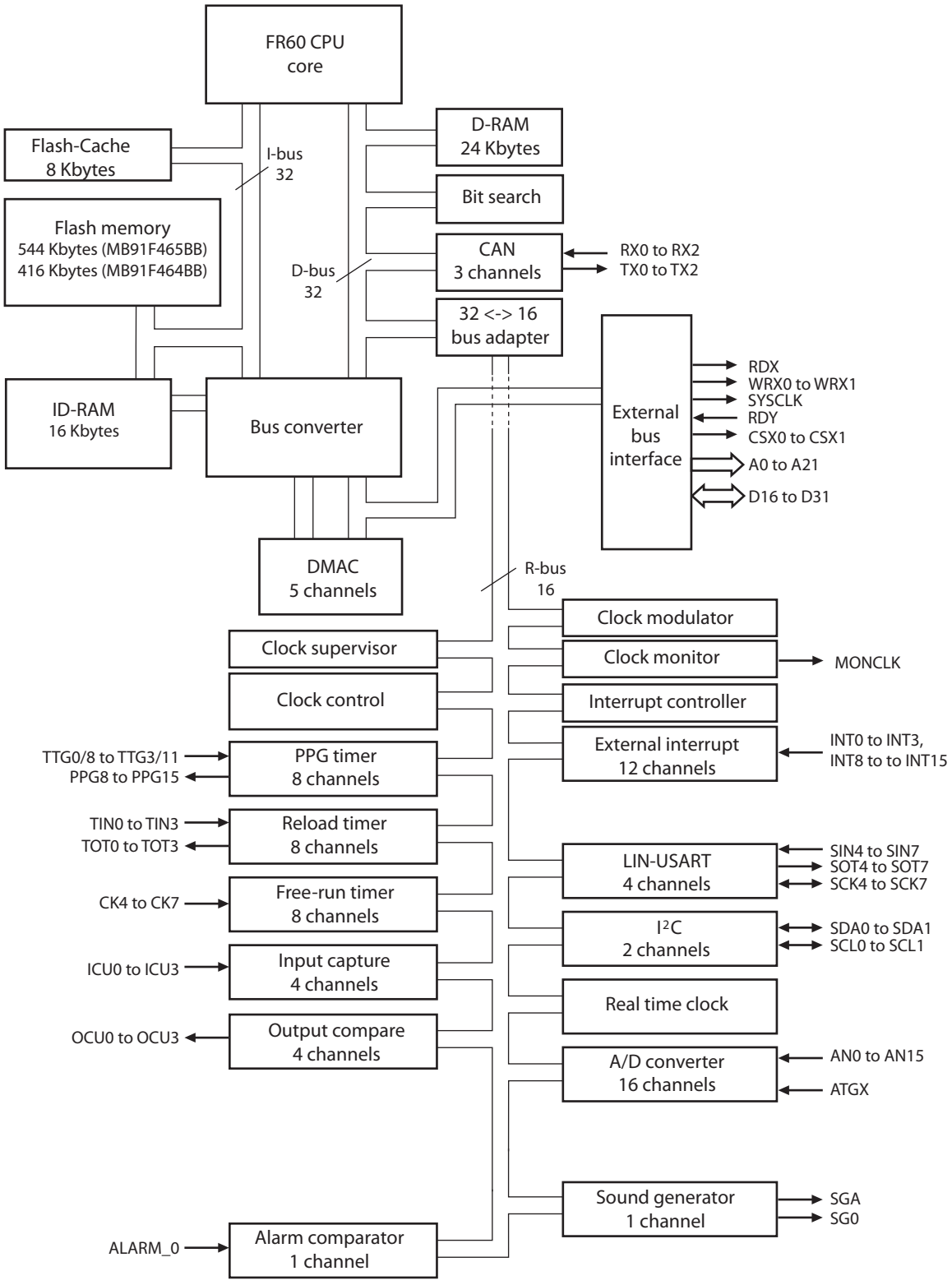
5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

7.3 MB91F465BB/464BB with MD_3=1



8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

9. Embedded Program/Data Memory (Flash)

9.1 Flash features

- MB91F467BA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.5 Mbits)
- MB91F466BA: 832 Kbytes (12 × 64 Kbytes + 8 × 8 Kbytes = 6.5 Mbits)
- MB91F465BB: 544 Kbytes (8 × 64 Kbytes + 4 × 8 Kbytes = 4.25 Mbits)
- MB91F464BB: 416 Kbytes (6 × 64 Kbytes + 4 × 8 Kbytes = 3.25 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes

9.2.1 64-bit CPU mode (available on MB91F467BA/466BA only) :

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

9.2.2 32-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

9.2.3 16-bit CPU mode:

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in word (16-bit) length units.

9.2.4 Flash Memory Mode (External Access to Flash Memory Enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

Legend	Memory not available in this area	Memory available in this area

9.3.2 Flash Access Timing Settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

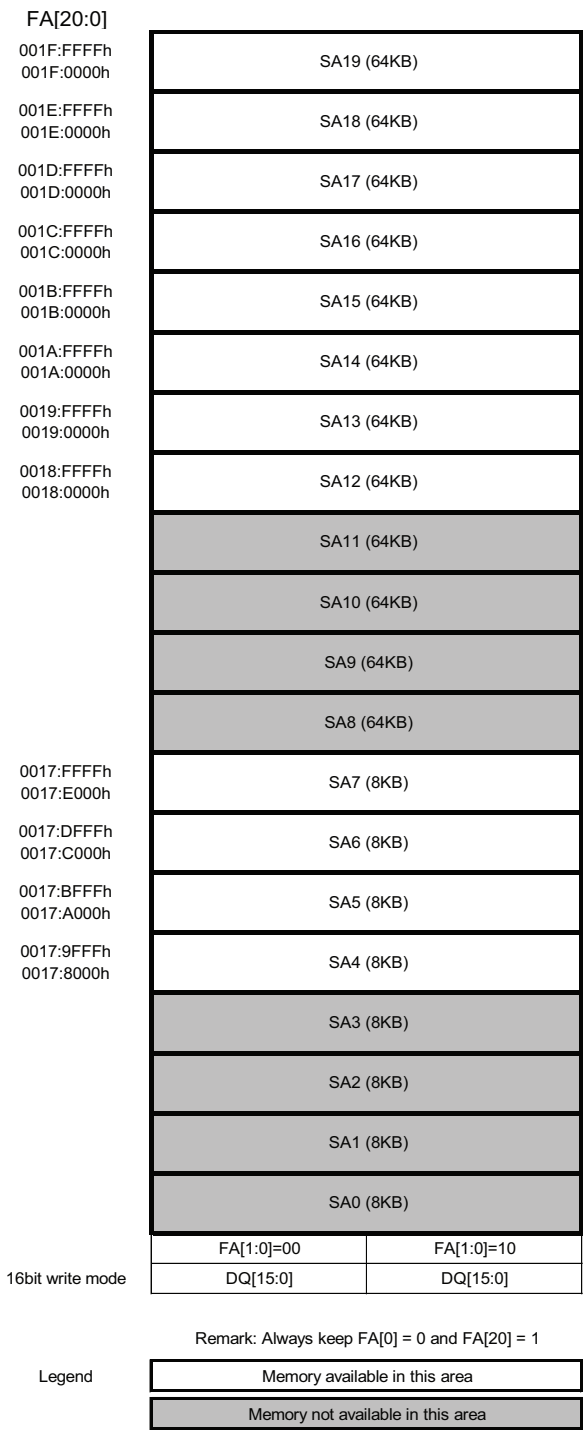
9.3.2.1 Flash Read Timing Settings (Synchronous Read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F467BA/MB91F466BA

9.3.2.2 Flash Write Timing Settings (Synchronous Write)

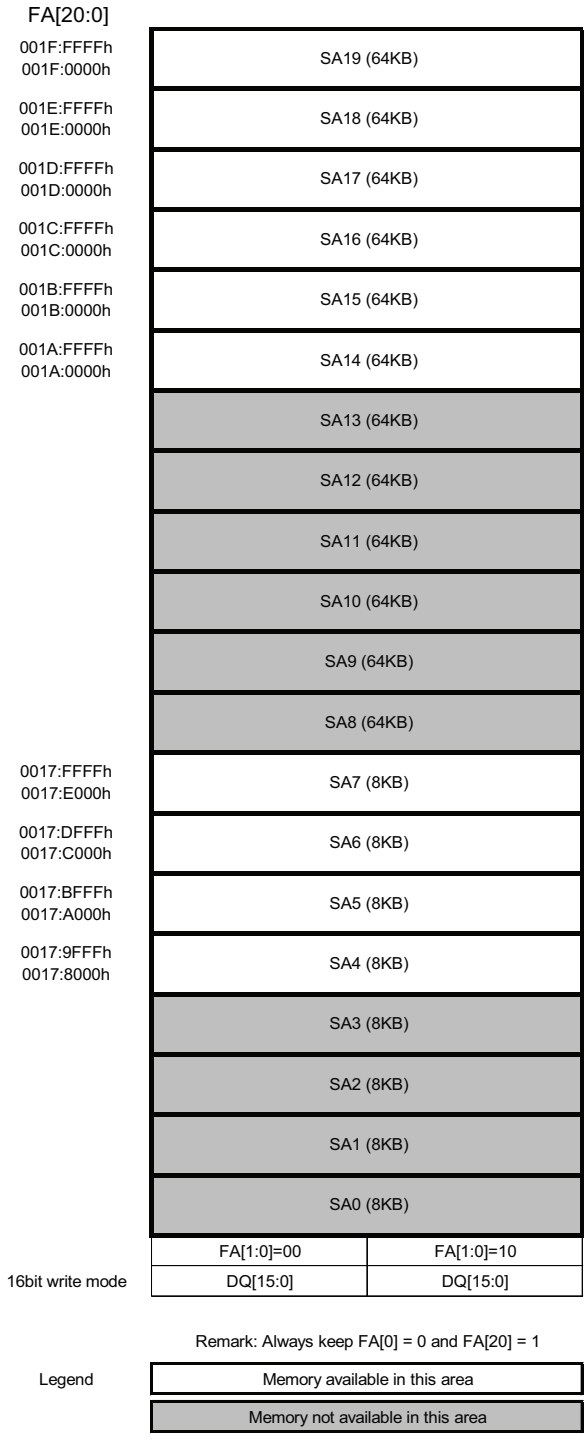
Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F467BA/MB91F466BA

MB91F465BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

MB91F464BB



Remark: Always keep FA[0] = 0 and FA[20] = 1

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area
The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access: 000_H to $0FF_H$

Half word access: 000_H to $1FF_H$

Word data access: 000_H to $3FF_H$

Address	Register				Block
	+0	+1	+2	+3	
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	PPER05 [R/W] - - 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 0 - - 0 - - - 0	PPER09 [R/W] - - - - - - 00	PPER10 [R/W] - - - - - - - 0	Reserved	
$000ECC_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - - - - - - 00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
$000F04_H$	Reserved	PPCR05 [R/W] - - 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 1 - - 1 - - - 1	PPCR09 [R/W] - - - - - - 11	PPCR10 [R/W] - - - - - - - 1	Reserved	
$000F0C_H$	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
$000F14_H$	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] - - - - - - 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ to $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$ to $00C03C_H$	Reserved				
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ to $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ to $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$ to $00C18C_H$	Reserved		Reserved		
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$ to $00C19C_H$	Reserved		Reserved		
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$ to $00C1AC_H$	Reserved		Reserved		
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$ to $00C1FC_H$	Reserved		Reserved		
$00C200_H$	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
$00C204_H$	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
$00C208_H$	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
$00C20C_H$	BRPE2 [R/W] 00000000 00000000		CBSYNC2		

Address	Register				Block
	+0	+1	+2	+3	
$00C510_H$	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF 1 Register **Note:** Not on MB91F465BB/MB91F464BB
$00C514_H$	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
$00C518_H$	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		
$00C51C_H$	IF1MCTR5 [R/W] 00000000 00000000		Reserved		
$00C520_H$	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		
$00C524_H$	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		
$00C528_H$ to $00C52C_H$	Reserved				
$00C530_H$	IF1DTA25 [R/W] 00000000 00000000		IF1DTA15 [R/W] 00000000 00000000		
$00C534_H$	IF1DTB25 [R/W] 00000000 00000000		IF1DTB15 [R/W] 00000000 00000000		
$00C538_H$ to $00C53C_H$	Reserved				
$00C540_H$	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF 2 Register **Note**: Not on MB91F465BB/MB91F464BB
$00C544_H$	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
$00C548_H$	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
$00C54C_H$	IF2MCTR5 [R/W] 00000000 00000000		Reserved		
$00C550_H$	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
$00C554_H$	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
$00C558_H$ to $00C55C_H$	Reserved				
$00C560_H$	IF2DTA25 [R/W] 00000000 00000000		IF2DTA15 [R/W] 00000000 00000000		
$00C564_H$	IF2DTB25 [R/W] 00000000 00000000		IF2DTB15 [R/W] 00000000 00000000		
$00C568_H$ to $00C57C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags **Note:** Not on MB91F465BB/MB91F464BB
$00C584_H$ to $00C58C_H$	Reserved				
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
$00C594_H$ to $00C59C_H$	Reserved				
$00C5A0_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
$00C5A4_H$ to $00C5AC_H$	Reserved				
$00C5B0_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
$00C5B4_H$ to $00EFFC_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--000000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

4. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
5. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
6. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.
7. The maximum permitted power dissipation depends onm the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} + I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

8. Worst case value for the QFP package mounted on a 4-layer PCB at specified T_A without air flow.
9. Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	-	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	-	$AV_{CC}5$ × 0.25	V	
Power supply current per ADC macro [3]	I_A	$AV_{CC}5$	-	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	-	-	5	µA	A/D Converter not operated [1]
Reference voltage current per ADC macro [3]	I_R	AVRH5	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	-	-	5	µA	A/D Converter not operated [2]

1. Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5$ = AVRH = 5.0 V)
2. Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5$ = AVRH = 5.0 V)
3. The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation

T_{samp} = (2.6 kOhm + R_{EXT}) × 11pF × 7; for 4.5V ≤ $AV_{CC}5$ ≤ 5.5V

T_{samp} = (12.1 kOhm + R_{EXT}) × 11pF × 7; for 3.0V ≤ $AV_{CC}5$ ≤ 4.5V

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

15.4.1 Definition of A/D Converter Terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

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