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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

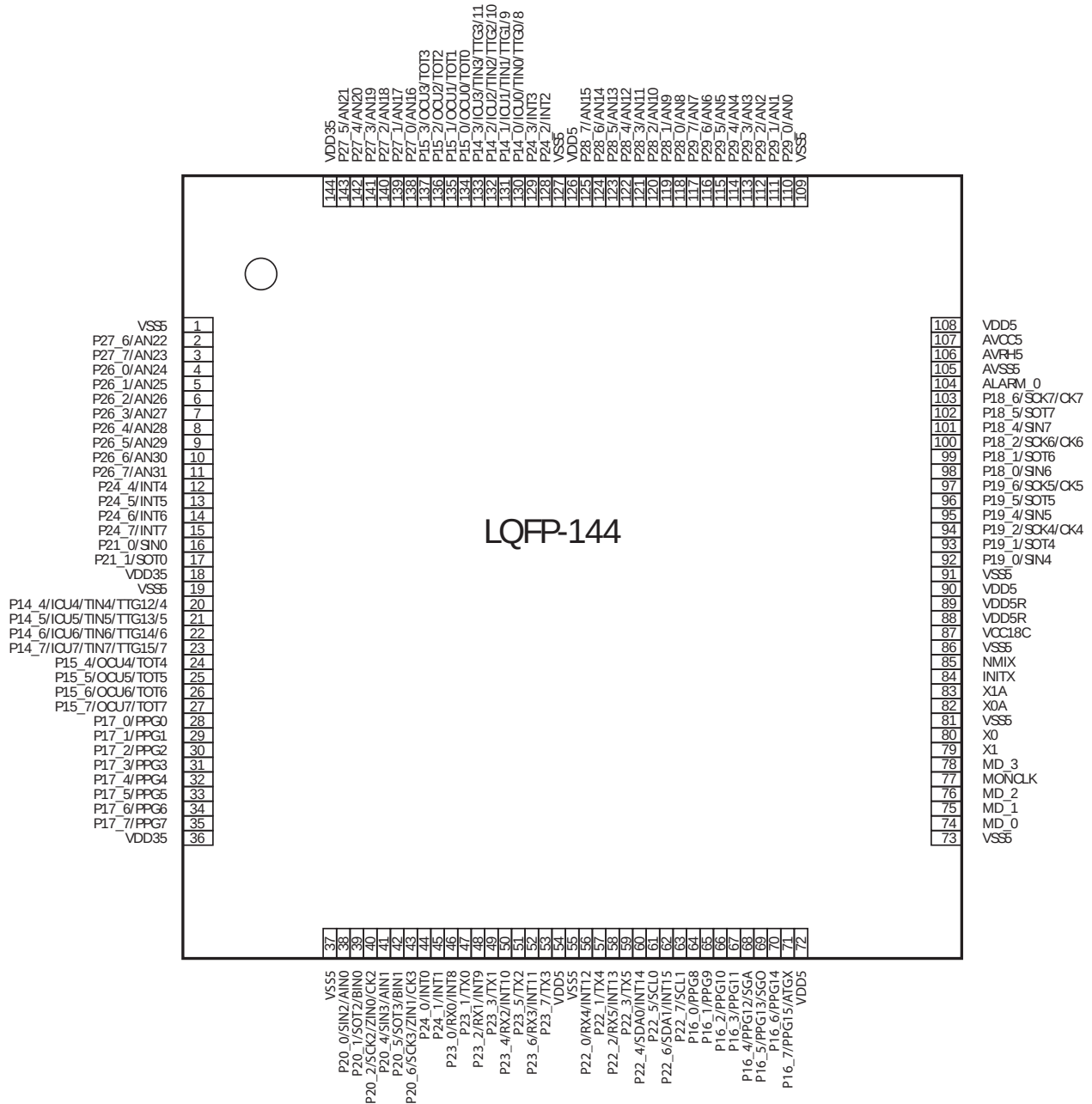
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w020

2.2 MB91F467BA/466BA with MD_3=0

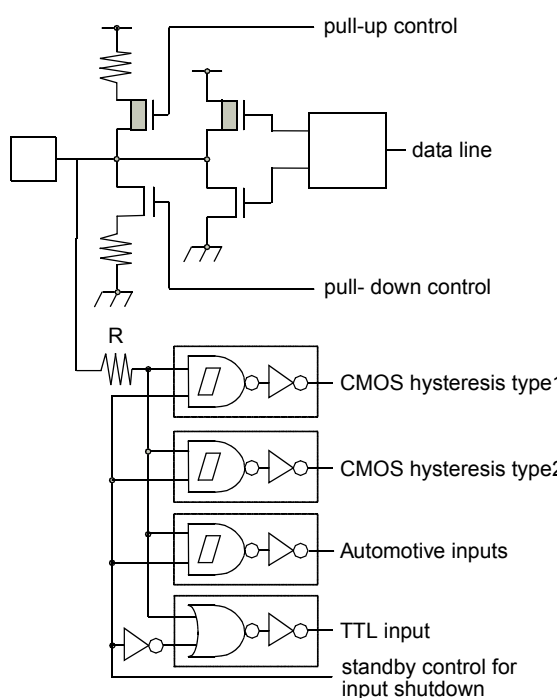
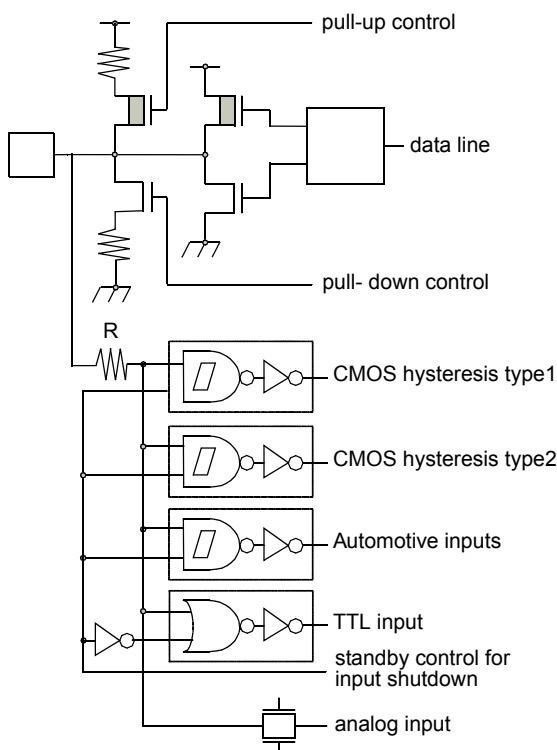
(TOP VIEW)



Pin no.	Pin name	I/O	I/O circuit type ^[1]	Function
64	P16_0	I/O	A	General-purpose input/output port
	PPG8			Output pins of PPG timer
65	P16_1	I/O	A	General-purpose input/output port
	PPG9			Output pins of PPG timer
66	P16_2	I/O	A	General-purpose input/output port
	PPG10			Output pins of PPG timer
67	P16_3	I/O	A	General-purpose input/output port
	PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pins of PPG timer
	SG0			SG0 output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output port
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pin
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5

Pin no.	Pin name	I/O	I/O circuit type ^[1]	Function
95	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output ports
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output ports
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output ports
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P27_0 to P27_5	I/O	B	General-purpose input/output ports
	AN16 to AN21			Analog input pins of A/D converter

1. For information about the I/O circuit type, refer to "I/O Circuit Types".

Type	Circuit	Remarks
C	 pull-up control data line pull-down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown	CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx.
D	 pull-up control data line pull-down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown analog input	CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. Analog input

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than (V_{DD5} , V_{DD35} or HV_{DD5} ^[1]) or less than (V_{SS5} or HV_{SS5} ^[1]) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note: 1. HV_{DD5} , HV_{SS5} are available only on devices having Stepper Motor Controller.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2K Ω to 10K Ω) or enable internal pullup or pulldown resistors (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to V_{SS5} or V_{DD5} directly. Unused ALARM input pins can be connected to AV_{SS5} directly.

5.3 Power Supply Pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance. It is also recommended to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between power supply pin and ground pin near this device. This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μ F (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

5.4 Crystal Oscillator Circuit

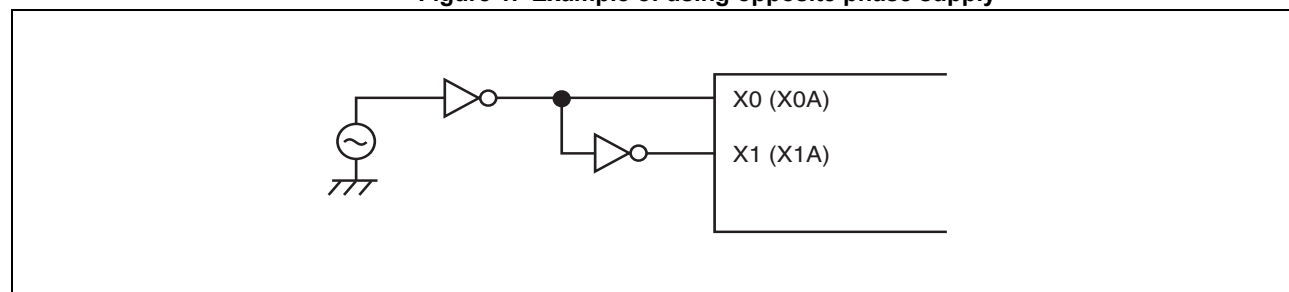
Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Figure 1. Example of using opposite phase supply



5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

■ **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**

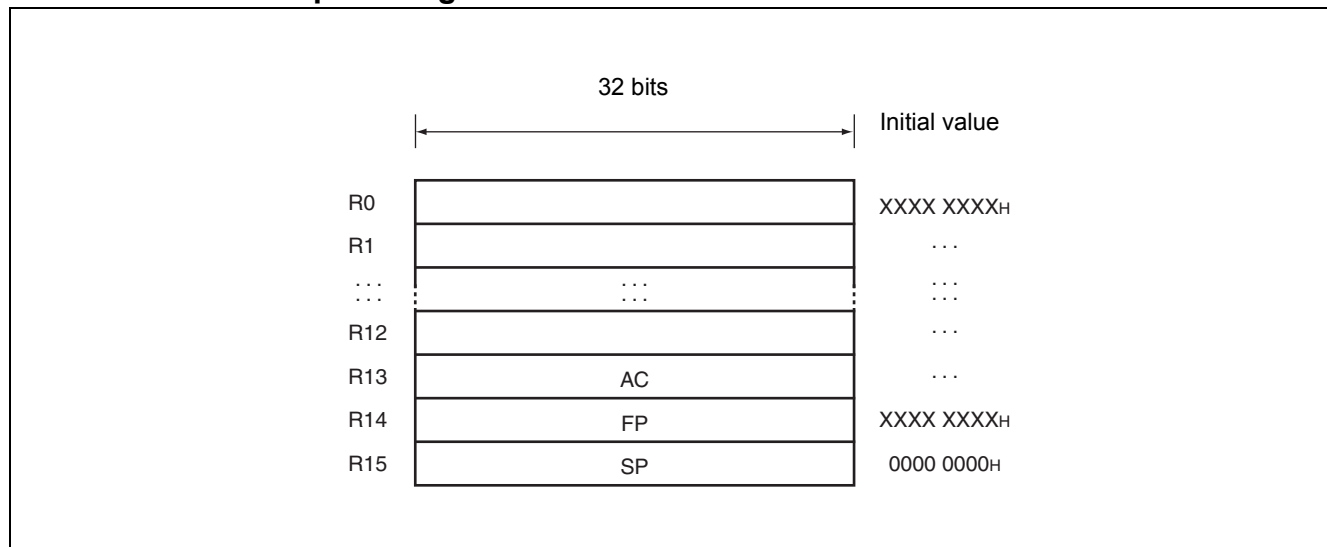
- (a) a user interrupt or NMI is accepted;
- (b) single-step execution is performed;
- (c) execution breaks due to a data event or from the emulator menu.
 - 1. D0 and D1 flags are updated in advance.
 - 2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
 - 3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

■ **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**

- 1. The PS register is updated in advance.
- 2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
- 3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

8.4 Registers

8.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

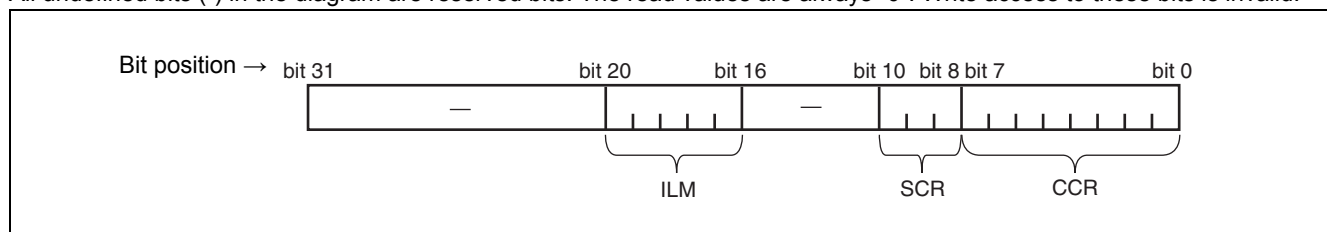
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								
Legend	Memory not available in this area				Memory available in this area				

9.3.2 Flash Access Timing Settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

9.3.2.1 Flash Read Timing Settings (Synchronous Read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F467BA/MB91F466BA

9.3.2.2 Flash Write Timing Settings (Synchronous Write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F467BA/MB91F466BA

Address	Register				Block
	+0	+1	+2	+3	
000300 _H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304 _H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308 _H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
00030C _H to 00031C _H	Reserved				Reserved
000320 _H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] ---- 0000	PPG Control 12 to 15
000324 _H to 00032C _H	Reserved				Reserved
000330 _H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334 _H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338 _H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033C _H	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340 _H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344 _H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348 _H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034C _H	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350 _H to 00038C _H	Reserved				Reserved
000390 _H	ROMS [R] 11111111 00000000 (MB91F467BA/466BA) 11111111 01000011 (MB91F465BB/464BB)		Reserved		ROM Select Register
000394 _H to 0003EC _H	Reserved				Reserved
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H to 00043C _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000640 _H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000 ^[2]		External Bus Unit
000644 _H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648 _H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064C _H	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650 _H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654 _H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658 _H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065C _H	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660 _H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664 _H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668 _H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066C _H	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670 _H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674 _H	Reserved				
000678 _H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C _H	Reserved				
000680 _H	CSEr [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** ^[3]	
000684 _H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688 _H to 0007F8 _H	Reserved				External Bus Unit
0007FC _H	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800 _H to 000CFC _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
00C080 _H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
00C084 _H to 00C08C _H	Reserved		Reserved		
00C090 _H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094 _H to 00C09C _H	Reserved		Reserved		
00C0A0 _H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4 _H to 00C0AC _H	Reserved		Reserved		
00C0B0 _H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4 _H to 00C0FC _H	Reserved		Reserved		
00C100 _H	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
00C104 _H	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
00C108 _H	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
00C10C _H	BRPE1 [R/W] 00000000 00000000		CBSYNC1		
00C110 _H	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
00C114 _H	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
00C118 _H	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
00C11C _H	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
00C120 _H	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
00C124 _H	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
00C128 _H to 00C12C _H	Reserved				
00C130 _H	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
00C134 _H	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
00C138 _H to 00C13C _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C580 _H	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags Note: Not on MB91F465BB/MB91F464 BB
00C584 _H to 00C58C _H	Reserved				
00C590 _H	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
00C594 _H to 00C59C _H	Reserved				
00C5A0 _H	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
00C5A4 _H to 00C5AC _H	Reserved				
00C5B0 _H	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
00C5B4 _H to 00E5FC _H	Reserved				
00F000 _H	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU
00F004 _H	BSTAT [R/W] ----- 000 00000000 10 -- 000000				
00F008 _H	BIAC [R] ----- 00000000 00000000				
00F00C _H	BOAC [R] ----- 00000000 00000000				
00F010 _H	BIRQ [R/W] ----- 00000000 00000000				
00F014 _H to 00F01C _H	Reserved				
00F020 _H	BCR0 [R/W] ----- 00000000 00000000 00000000				
00F024 _H	BCR1 [R/W] ----- 00000000 00000000 00000000				
00F028 _H	BCR2 [R/W] ----- 00000000 00000000 00000000				
00F02C _H	BCR3 [R/W] ----- 00000000 00000000 00000000				
00F030 _H to 00F07C _H	Reserved				Reserved

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current F467BA F466BA	I_{CC}	V_{DD5R}	CLKB: 96 MHz CLKP: 48 MHz CLKT: 48 MHz CLKCAN: 48 MHz	–	120	150	mA	Code fetch from Flash
	I_{CCH}	V_{DD5R}	$T_A = +25\text{ }^{\circ}\text{C}$	–	30	150	μA	At stop mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.4	2.0	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	1.0	5.0	mA	
			$T_A = +25\text{ }^{\circ}\text{C}$	–	100	500	μA	RTC: 4 MHz mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.5	2.4	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	1.1	5.4	mA	
			$T_A = +25\text{ }^{\circ}\text{C}$	–	50	250	μA	RTC: 100 kHz mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.45	2.2	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	1.05	5.2	mA	
	I_{LVE}	V_{DD5}	–	–	70	150	μA	External low voltage detection
	I_{LVI}	V_{DD5R}	–	–	50	100	μA	Internal low voltage detection
Power supply current F465BB F464BB	I_{OSC}	V_{DD5}	–	–	250	500	μA	Main clock (4 MHz)
			–	–	20	40	μA	Sub clock (32 kHz)
	I_{CC}	V_{DD5R}	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	–	110	140	mA	Code fetch from Flash
	I_{CCH}	V_{DD5R}	$T_A = +25\text{ }^{\circ}\text{C}$	–	30	150	μA	At stop mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.3	2.0	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	0.75	5.0	mA	
			$T_A = +25\text{ }^{\circ}\text{C}$	–	100	500	μA	RTC: 4 MHz mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.5	2.4	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	0.85	5.4	mA	
			$T_A = +25\text{ }^{\circ}\text{C}$	–	50	250	μA	RTC: 100 kHz mode [5]
			$T_A = +105\text{ }^{\circ}\text{C}$	–	0.4	2.2	mA	
			$T_A = +125\text{ }^{\circ}\text{C}$	–	0.8	5.2	mA	
	I_{LVE}	V_{DD5}	–	–	70	150	μA	External low voltage detection
	I_{LVI}	V_{DD5R}	–	–	50	100	μA	Internal low voltage detection
	I_{OSC}	V_{DD5}	–	–	250	500	μA	Main clock (4 MHz)
			–	–	20	40	μA	Sub clock (32 kHz)

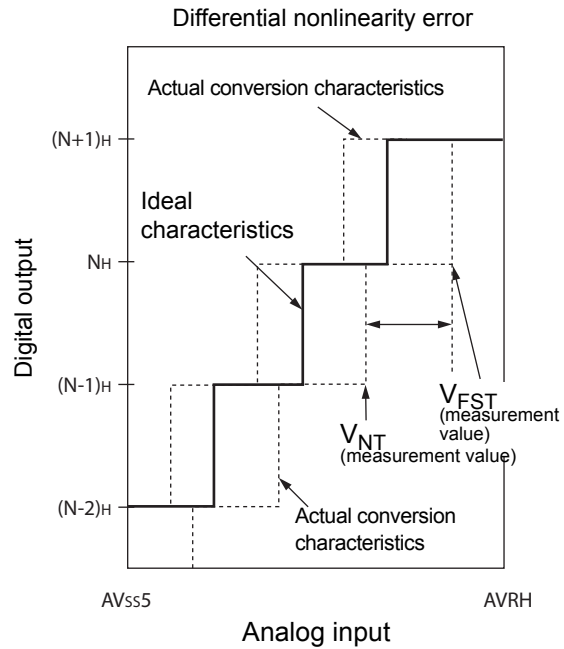
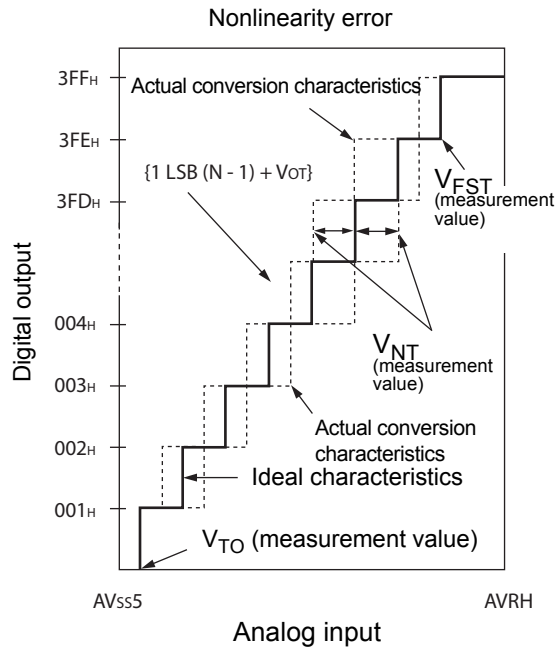
1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

15.4 A/D Converter Characteristics

($V_{DD5} = AV_{CC5} = 3.0 \text{ V to } 5.5 \text{ V}$, $V_{SS5} = AV_{SS5} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	– 3	–	+ 3	LSB	
Nonlinearity error	–	–	– 2.5	–	+ 2.5	LSB	
Differential nonlinearity error	–	–	– 1.9	–	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	–	0.6	–	16,500	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			2.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Sampling time	T_{samp}	–	0.4	–	–	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$, $R_{EXT} < 2 \text{ k}\Omega$
			1.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$, $R_{EXT} < 1 \text{ k}\Omega$
Conversion time	T_{conv}	–	1.0	–	–	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			3.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Input capacitance	C_{IN}	ANn	–	–	11	pF	
Input resistance	R_{IN}	ANn	–	–	2.6	$\text{k}\Omega$	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			–	–	12.1	$\text{k}\Omega$	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Analog input leakage current	I_{AIN}	ANn	– 1	–	+ 1	μA	$T_A = +25 \text{ }^{\circ}\text{C}$
			– 3	–	+ 3	μA	$T_A = +125 \text{ }^{\circ}\text{C}$
Analog input voltage range	V_{AIN}	ANn	AVRL	–	AVRH	V	
Offset between input channels	–	ANn	–	–	4	LSB	

Note: The accuracy gets worse as AVRH - AVRL becomes smaller



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value

V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.

V_{FST} : Voltage at which the digital output changes from 3FE_H to 3FF_H.

15.7.4 I²C AC Timings at V_{DD5} = 3.0 to 5.5 V

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

- -I_{Odrive} = 3 mA
- -V_{DD5} = 3.0 V to 5.5 V, I_{load} = 3 mA
- -V_{SS5} = 0 V
- -T_a = -40 °C to +125 °C
- -C_I = 50 pF
- -VOL = 0.3 × V_{DD5}
- -VOH = 0.7 × V_{DD5}
- -EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × V_{DD5}/0.7 × V_{DD5})

15.7.4.1 Fast mode:

(V_{DD5} = 3.5 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = -40 °C to +125 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f _{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD;STA}	SCLn, SDAn	0.6	–	μs	
LOW period of the SCL clock	t _{LOW}	SCLn	1.3	–	μs	
HIGH period of the SCL clock	t _{HIGH}	SCLn	0.6	–	μs	
Setup time for a repeated START condition	t _{SU;STA}	SCLn, SDAn	0.6	–	μs	
Data hold time for I ² C-bus devices	t _{HD;DAT}	SCLn, SDAn	0	0.9	μs	
Data setup time	t _{SU;DAT}	SCLn, SDAn	100	–	ns	
Rise time of both SDA and SCL signals	t _r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t _f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	t _{SU;STO}	SCLn, SDAn	0.6	–	μs	
Bus free time between a STOP and START condition	t _{BUF}	SCLn, SDAn	1.3	–	μs	
Capacitive load for each bus line	C _b	SCLn, SDAn	–	400	pF	
Pulse width of spike suppressed by input filter	t _{SP}	SCLn, SDAn	0	(1..1.5) × t _{CLKP}	ns	[1]

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I²C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

18. Revision History

Spanion Publication Number: DS07-16609-1E

Version	Date	Remark
2.0	2008-06-19	Initial version
2.1	2008-08-15	Proof reading results from FJ incorporated; Corrected pinout drawings; IO CIRCUIT TYPES: corrected some typos like on the other datasheets; HANDLING DEVICES: updated the section "Notes on PS register" for better understanding; Interrupt Vector Table: corrected the footnotes FLASH: added note about the operation mode switching capability in Boot ROM; corrected flash security vector FSV2 assignments, corrected section about parallel programming, corrected section pin connections in parallel programming mode so that there is only one page added section "Poweron Sequence in parallel programming mode"; ELECTRICAL CHARACTERISTICS: removed the note that analog input/output pins cannot accept +B signal input; splitted I_{LV} into external and internal LV detection current ADC Characteristics: Corrected the items about nonlinearity error; Corrected the company name
3.0	2009-01-09	Page 1: Corrected document name field in top header Block Diagram: Removed SCK0 (LIN-USART0 is asynchronous only) Added Ta=125C characteristics

19. Main Changes in this Edition

Page	Section	Change Results
104	15. Electrical Characteristics 15.4. A/D converter characteristics	Corrected the column "Value" and "Unit" of the parameter "Zero reading voltage" and "Full scale reading voltage". (Value : AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB Unit : LSB → V)

NOTE: Please see "Document History" for later revised information.