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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

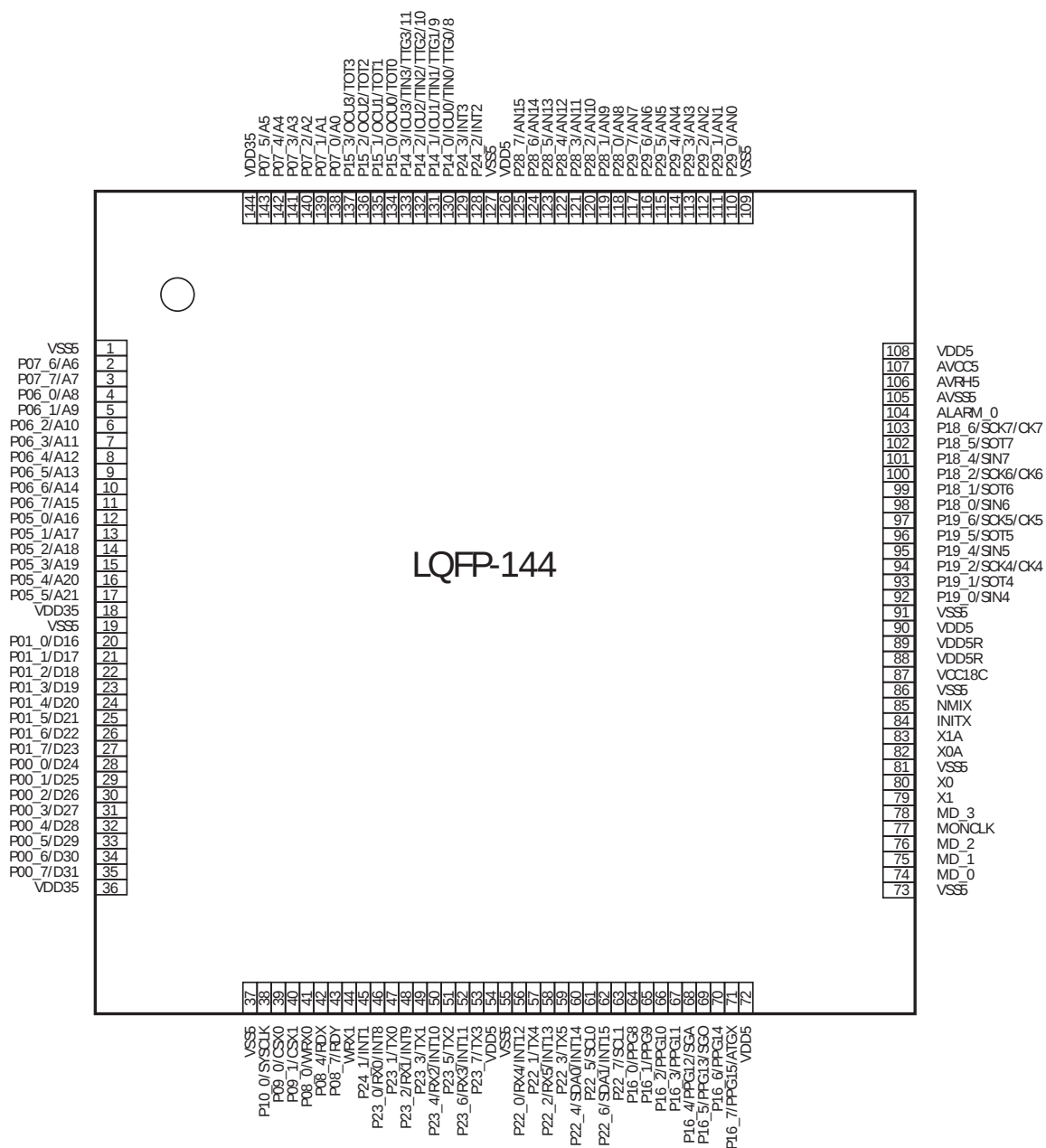
Details

Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	108
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467bapmc-gse2-w021

2. Pin Assignment

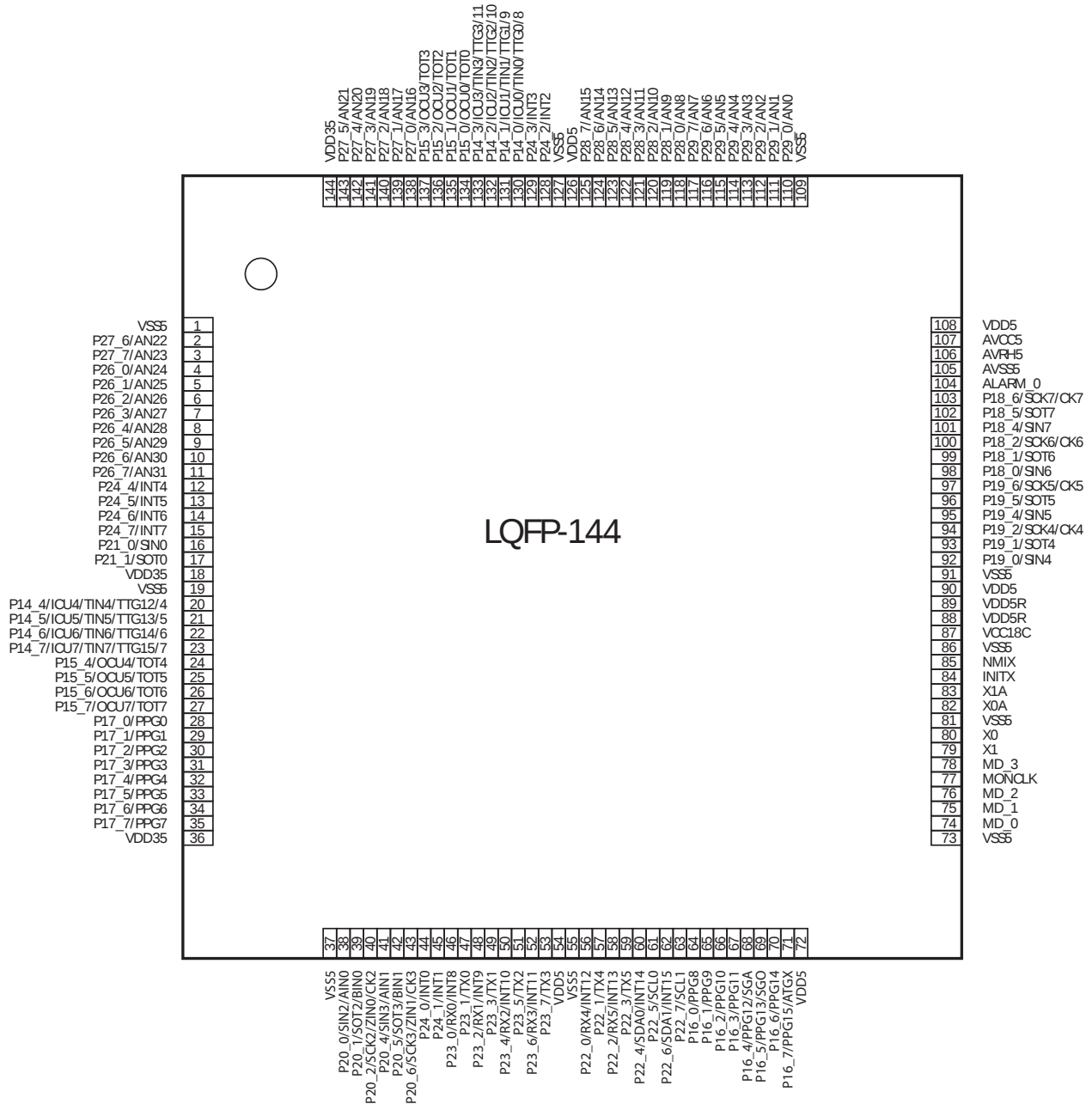
2.1 MB91F467BA/466BA with MD_3=1

(TOP VIEW)



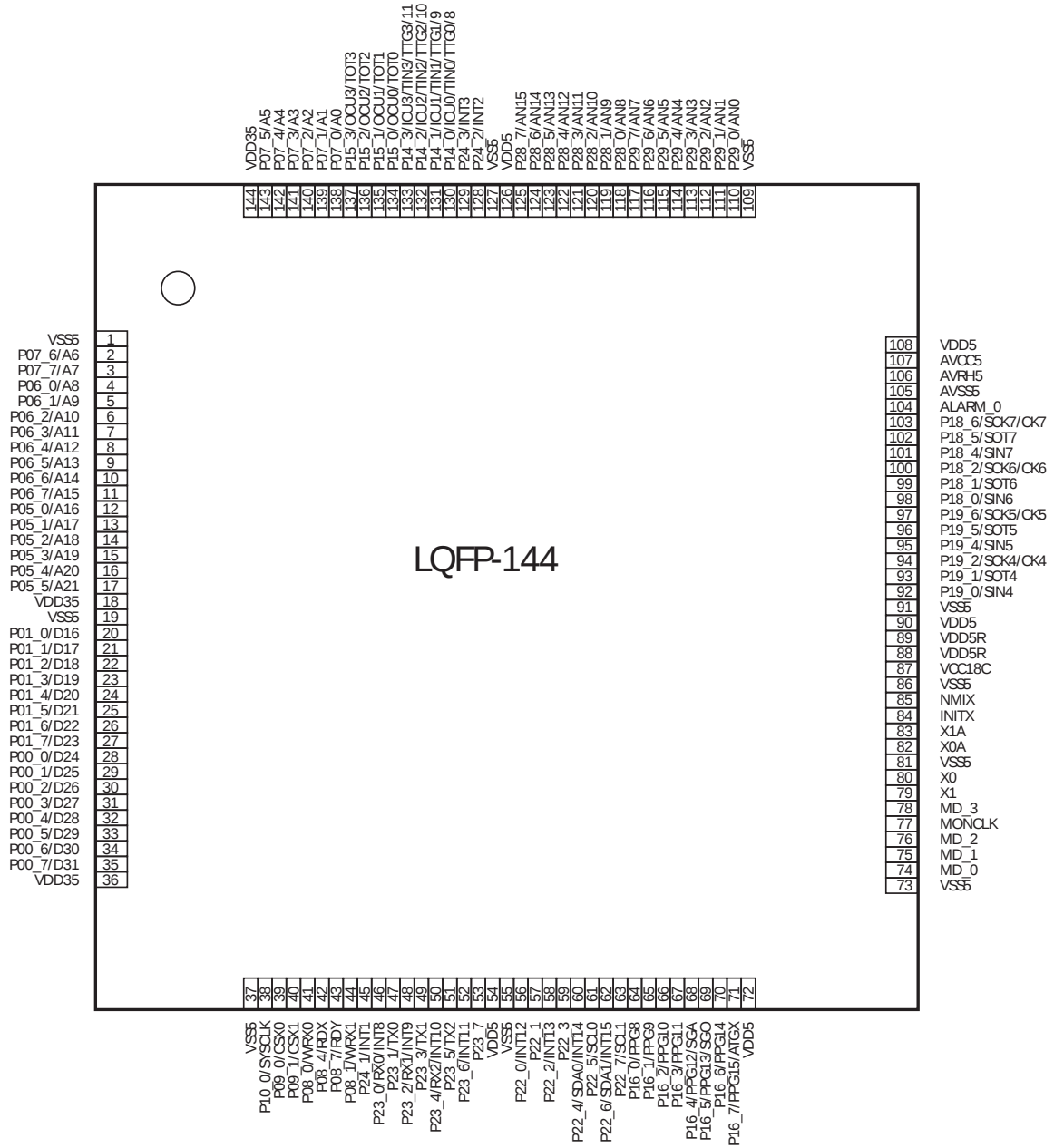
2.2 MB91F467BA/466BA with MD_3=0

(TOP VIEW)



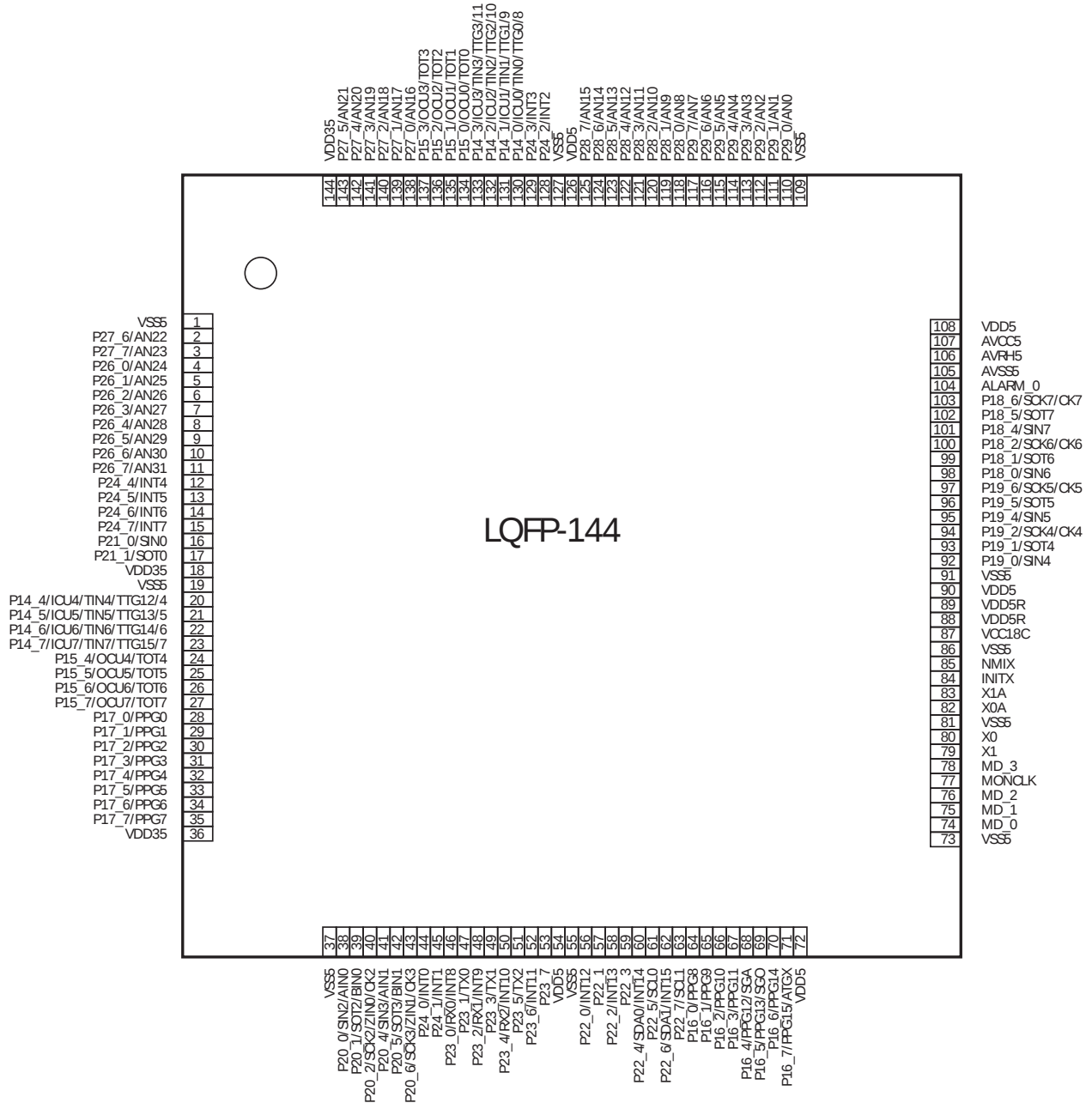
2.3 MB91F465BB/464BB with MD_3=1

(TOP VIEW)



2.4 MB91F465BB/464BB with MD_3=0

(TOP VIEW)



3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

Pin no.	Pin name	I/O	I/O circuit type ^[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466 BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466 BA			External interrupt input, can only be used in general-purpose I/O port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

3.1.1 Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than (V_{DD5} , V_{DD35} or HV_{DD5} ^[1]) or less than (V_{SS5} or HV_{SS5} ^[1]) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note: 1. HV_{DD5} , HV_{SS5} are available only on devices having Stepper Motor Controller.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2K Ω to 10K Ω) or enable internal pullup or pulldown resistors (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to V_{SS5} or V_{DD5} directly. Unused ALARM input pins can be connected to AV_{SS5} directly.

5.3 Power Supply Pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance. It is also recommended to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between power supply pin and ground pin near this device. This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μ F (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

5.4 Crystal Oscillator Circuit

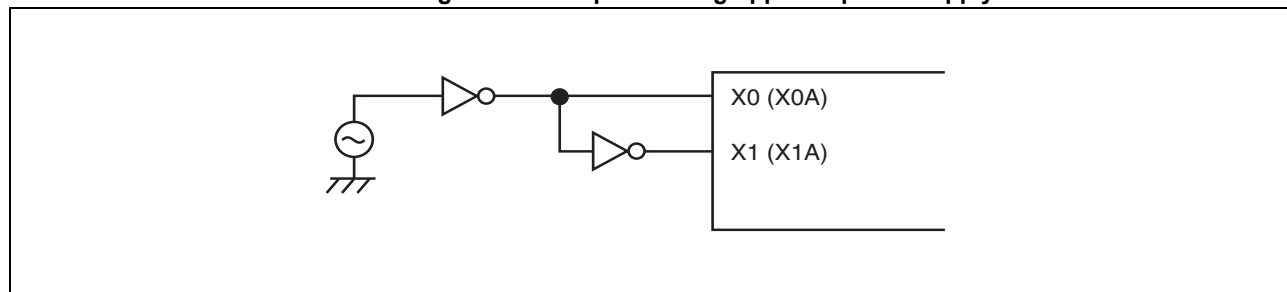
Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

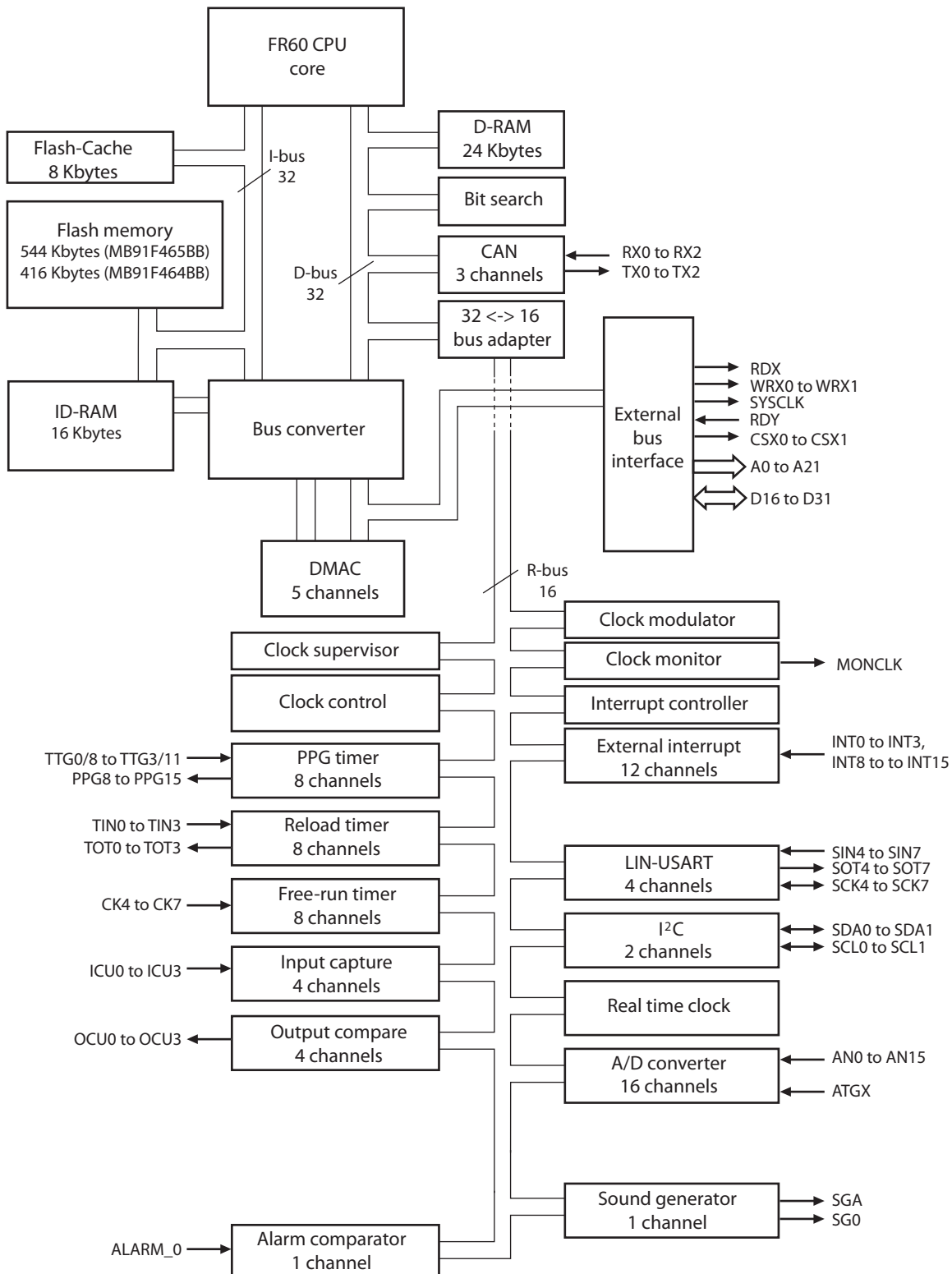
5.5 Notes on using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Figure 1. Example of using opposite phase supply

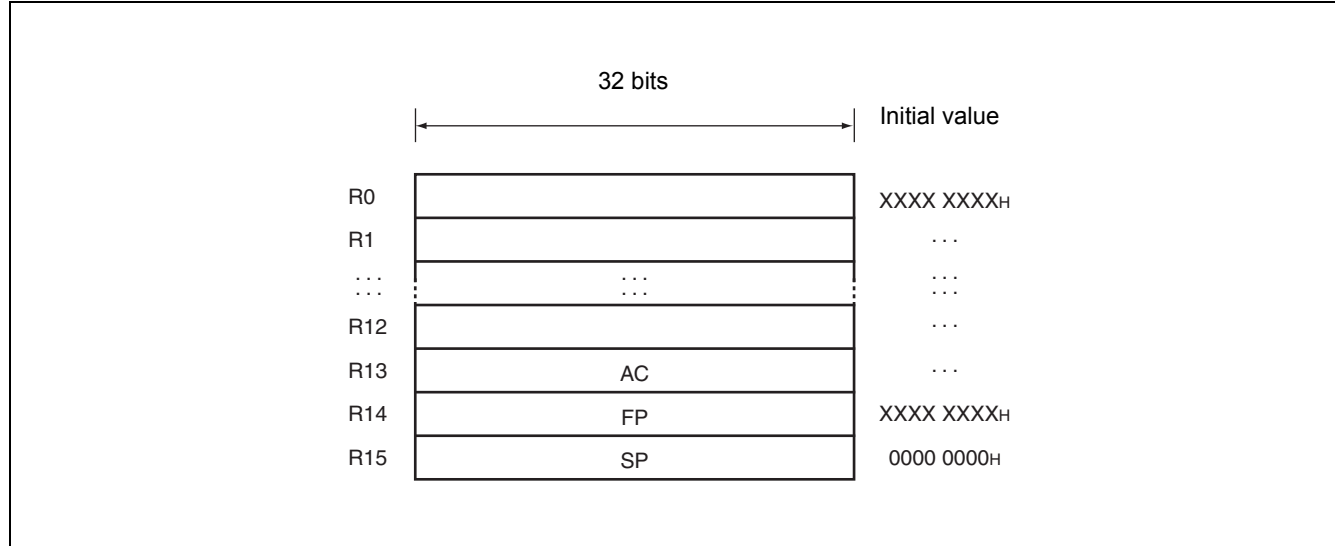


7.3 MB91F465BB/464BB with MD_3=1



8.4 Registers

8.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

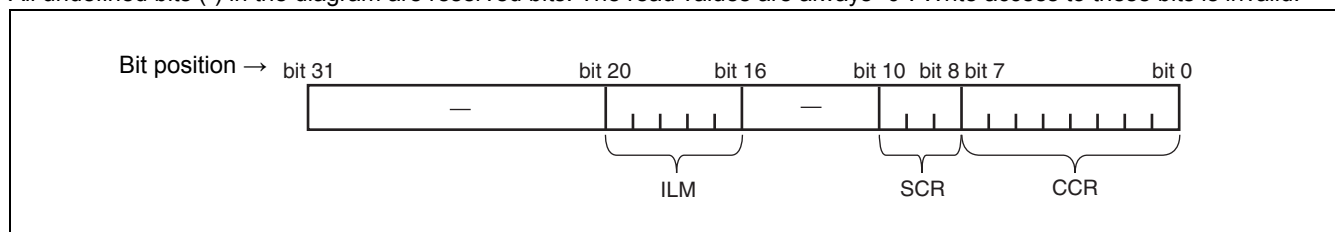
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



9. Embedded Program/Data Memory (Flash)

9.1 Flash features

- MB91F467BA: 1088 Kbytes ($16 \times 64 \text{ Kbytes} + 8 \times 8 \text{ Kbytes} = 8.5 \text{ Mbits}$)
- MB91F466BA: 832 Kbytes ($12 \times 64 \text{ Kbytes} + 8 \times 8 \text{ Kbytes} = 6.5 \text{ Mbits}$)
- MB91F465BB: 544 Kbytes ($8 \times 64 \text{ Kbytes} + 4 \times 8 \text{ Kbytes} = 4.25 \text{ Mbits}$)
- MB91F464BB: 416 Kbytes ($6 \times 64 \text{ Kbytes} + 4 \times 8 \text{ Kbytes} = 3.25 \text{ Mbits}$)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes

9.2.1 64-bit CPU mode (available on MB91F467BA/466BA only) :

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

9.2.2 32-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

9.2.3 16-bit CPU mode:

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in word (16-bit) length units.

9.2.4 Flash Memory Mode (External Access to Flash Memory Enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3.1.2 Flash Memory Map MB91F466BA

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								
Legend	Memory not available in this area				Memory available in this area				

MB91F465BB

FA[20:0]	
001F:FFFFh 001F:0000h	SA19 (64KB)
001E:FFFFh 001E:0000h	SA18 (64KB)
001D:FFFFh 001D:0000h	SA17 (64KB)
001C:FFFFh 001C:0000h	SA16 (64KB)
001B:FFFFh 001B:0000h	SA15 (64KB)
001A:FFFFh 001A:0000h	SA14 (64KB)
0019:FFFFh 0019:0000h	SA13 (64KB)
0018:FFFFh 0018:0000h	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)
	FA[1:0]=00 FA[1:0]=10
16bit write mode	DQ[15:0] DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

Memory available in this area
Memory not available in this area

MB91F464BB

FA[20:0]	
001F:FFFFh 001F:0000h	SA19 (64KB)
001E:FFFFh 001E:0000h	SA18 (64KB)
001D:FFFFh 001D:0000h	SA17 (64KB)
001C:FFFFh 001C:0000h	SA16 (64KB)
001B:FFFFh 001B:0000h	SA15 (64KB)
001A:FFFFh 001A:0000h	SA14 (64KB)
	SA13 (64KB)
	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)
	FA[1:0]=00 FA[1:0]=10
16bit write mode	DQ[15:0] DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

Memory available in this area
Memory not available in this area

9.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TCE xternal pins	FR-CPU mode	MB91F467BA/466BA/F465BB/F464BB External Pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to '1'
-	-	MD1	MD1	75	Set to '1'
-	-	MD0	MD0	74	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to 'H'	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to '0'
-		EQIN	GP18_5	102	Set to '0'
-		TESTX	GP16_5	69	Set to '1'
-		RDYI	GP18_4	101	Set to '0'
A-1	Internal address bus	FA0	GP05_5	17	Set to '0'
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A18		FA17 to FA19	GP05_0 to GP05_2	12 to 14	
A19		FA20	GP05_3	15	See note ^[1]
-		FA21	GP05_4	16	See note ^[2]
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

1. A19 is used as address bit on MB91F467BA/F466BA. For MB91F465BB/F464BB, set this pin to '1'.
2. For MB91F467BA/F466BA, set this pin to '1'. For MB91F465BB/F464BB, this pin can be left open.

9.6.3 Security Vector FSV2 MB91F467BA/466BA

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 5. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to "0"	set to "1"	
FSV2[1]	SA9	set to "0"	set to "1"	
FSV2[2]	SA10	set to "0"	set to "1"	
FSV2[3]	SA11	set to "0"	set to "1"	
FSV2[4]	SA12	set to "0"	set to "1"	
FSV2[5]	SA13	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[12]	SA20 (MB91F467BA)	set to "0"	set to "1"	
FSV2[13]	SA21 (MB91F467BA)	set to "0"	set to "1"	
FSV2[14]	SA22 (MB91F467BA)	set to "0"	set to "1"	
FSV2[15]	SA23 (MB91F467BA)	set to "0"	set to "1"	
FSV2[31:16]	–	set to "0"	set to "1"	not available

Note: See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

9.6.4 Security Vector FSV2 MB91F465BB/464BB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 6. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[3:0]	–	–	–	not available
FSV2[4]	SA12 (MB91F465BB)	set to "0"	set to "1"	
FSV2[5]	SA13 (MB91F465BB)	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[31:12]	–	–	–	not available

Note: See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

Address	Register				Block
	+0	+1	+2	+3	
000640 _H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000 ^[2]		External Bus Unit
000644 _H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648 _H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064C _H	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650 _H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654 _H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658 _H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065C _H	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660 _H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664 _H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668 _H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066C _H	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670 _H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674 _H	Reserved				
000678 _H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C _H	Reserved				
000680 _H	CSEr [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** ^[3]	
000684 _H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688 _H to 0007F8 _H	Reserved				External Bus Unit
0007FC _H	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800 _H to 000CFC _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000E40 _H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
000E44 _H	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48 _H	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - 00	PILR10 [R/W] - - - - - 0	Reserved	
000E4C _H	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
000E50 _H	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - 000	PILR19 [R/W] - 000 - 000	
000E54 _H	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
000E58 _H	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5C _H	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
000E60 _H to 000E7C _H	Reserved				Reserved
000E80 _H	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
000E84 _H	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88 _H	EPILR08 [R/W] 0 - - 0 - - - 0	EPILR09 [R/W] - - - - - 00	EPILR10 [R/W] - - - - - 0	Reserved	
000E8C _H	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
000E90 _H	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - 000	EPILR19 [R/W] - 000 - 000	
000E94 _H	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
000E98 _H	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9C _H	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
000EA0 _H to 000EBC _H	Reserved				Reserved

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000 _H to 1BFFF8 _H	External Bus Area								ROMS8
1C0000 _H to 1FFFF8 _H									ROMS9
200000 _H to 27FFF8 _H									ROMS10
280000 _H to 2FFFF8 _H									ROMS11
300000 _H to 37FFF8 _H									ROMS12
380000 _H to 3FFFF8 _H									ROMS13
400000 _H to 47FFF8 _H									ROMS14
480000 _H to 4FFFF8 _H									ROMS15

Notes: Write operations to address 0FFFF8_H and 0FFFFC_H are not possible. When reading these addresses, the values shown above will be read. On MB91F465BB/F464BB, write access to the flash is only possible in 16-bit mode.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level ^[1]		Interrupt vector ^[2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	3FC _H	000FFFFC _H	—
Mode vector	1	01	—	—	3F8 _H	000FFFF8 _H	—
System reserved	2	02	—	—	3F4 _H	000FFFF4 _H	—
System reserved	3	03	—	—	3F0 _H	000FFFF0 _H	—
System reserved	4	04	—	—	3EC _H	000FFFE _C	—
CPU supervisor mode (INT #5 instruction) ^[5]	5	05	—	—	3E8 _H	000FFFE8 _H	—
Memory Protection exception ^[5]	6	06	—	—	3E4 _H	000FFFE4 _H	—
System reserved	7	07	—	—	3E0 _H	000FFFE0 _H	—
System reserved	8	08	—	—	3DC _H	000FFFD _C	—
System reserved	9	09	—	—	3D8 _H	000FFFD8 _H	—
System reserved	10	0A	—	—	3D4 _H	000FFFD4 _H	—
System reserved	11	0B	—	—	3D0 _H	000FFFD0 _H	—
System reserved	12	0C	—	—	3CC _H	000FFFC _C	—
System reserved	13	0D	—	—	3C8 _H	000FFFC8 _H	—
Undefined instruction exception	14	0E	—	—	3C4 _H	000FFFC4 _H	—
NMI request	15	0F	F _H fixed		3C0 _H	000FFFC0 _H	—
External Interrupt 0	16	10	ICR00	440 _H	3BC _H	000FFFB _C	0, 16
External Interrupt 1	17	11			3B8 _H	000FFFB8 _H	1, 17
External Interrupt 2	18	12	ICR01	441 _H	3B4 _H	000FFFB4 _H	2, 18
External Interrupt 3	19	13			3B0 _H	000FFFB0 _H	3, 19
External Interrupt 4	20	14	ICR02	442 _H	3AC _H	000FFFA _C	20
External Interrupt 5	21	15			3A8 _H	000FFFA8 _H	21
External Interrupt 6	22	16	ICR03	443 _H	3A4 _H	000FFFA4 _H	22
External Interrupt 7	23	17			3A0 _H	000FFFA0 _H	23
External Interrupt 8	24	18	ICR04	444 _H	39C _H	000FFF9 _C	—
External Interrupt 9	25	19			398 _H	000FFF98 _H	—
External Interrupt 10	26	1A	ICR05	445 _H	394 _H	000FFF94 _H	—
External Interrupt 11	27	1B			390 _H	000FFF90 _H	—
External Interrupt 12	28	1C	ICR06	446 _H	38C _H	000FFF8 _C	—
External Interrupt 13	29	1D			388 _H	000FFF88 _H	—
External Interrupt 14	30	1E	ICR07	447 _H	384 _H	000FFF84 _H	—
External Interrupt 15	31	1F			380 _H	000FFF80 _H	—
Reload Timer 0	32	20	ICR08	448 _H	37C _H	000FFF7 _C	4, 32
Reload Timer 1	33	21			378 _H	000FFF78 _H	5, 33
Reload Timer 2	34	22	ICR09	449 _H	374 _H	000FFF74 _H	34
Reload Timer 3	35	23			370 _H	000FFF70 _H	35

15.7.4 I²C AC Timings at V_{DD5} = 3.0 to 5.5 V

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

- -I_{Odrive} = 3 mA
- -V_{DD5} = 3.0 V to 5.5 V, I_{load} = 3 mA
- -V_{SS5} = 0 V
- -T_a = -40 °C to +125 °C
- -C_I = 50 pF
- -VOL = 0.3 × V_{DD5}
- -VOH = 0.7 × V_{DD5}
- -EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × V_{DD5}/0.7 × V_{DD5})

15.7.4.1 Fast mode:

(V_{DD5} = 3.5 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = -40 °C to +125 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f _{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD;STA}	SCLn, SDAn	0.6	–	μs	
LOW period of the SCL clock	t _{LOW}	SCLn	1.3	–	μs	
HIGH period of the SCL clock	t _{HIGH}	SCLn	0.6	–	μs	
Setup time for a repeated START condition	t _{SU;STA}	SCLn, SDAn	0.6	–	μs	
Data hold time for I ² C-bus devices	t _{HD;DAT}	SCLn, SDAn	0	0.9	μs	
Data setup time	t _{SU;DAT}	SCLn, SDAn	100	–	ns	
Rise time of both SDA and SCL signals	t _r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t _f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	t _{SU;STO}	SCLn, SDAn	0.6	–	μs	
Bus free time between a STOP and START condition	t _{BUF}	SCLn, SDAn	1.3	–	μs	
Capacitive load for each bus line	C _b	SCLn, SDAn	–	400	pF	
Pulse width of spike suppressed by input filter	t _{SP}	SCLn, SDAn	0	(1..1.5) × t _{CLKP}	ns	[1]

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I²C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

15.7.7 External Bus AC Timings at $V_{DD35} = 3.0$ to 5.5 V

Note: This chapter is applicable to MB91F467BA/F466BA

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

- $-I_{Odrive} = 5$ mA
- $-V_{DD35} = 4.5$ V to 5.5 V, $I_{load} = 3$ mA
- $-V_{SS5} = 0$ V
- $-T_a = -40$ °C to $+125$ °C
- $-C_I = 50$ pF
- $-VOL = 0.5 \times V_{DD35}$
- $-VOH = 0.5 \times V_{DD35}$
- $-EPILR = 0$, $PILR = 1$ (Automotive Level = worst case)

15.7.7.1 Basic Timing

($V_{DD35} = 3.0$ V to 5.5 V, $V_{ss5} = AV_{ss5} = 0$ V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	$1/2 \times t_{CLKT} - 1$	$1/2 \times t_{CLKT} + 9$	ns
	t_{CHCL}		$1/2 \times t_{CLKT} - 9$	$1/2 \times t_{CLKT} + 1$	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	-	8	ns
	t_{CLCSH}		-	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	-	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.