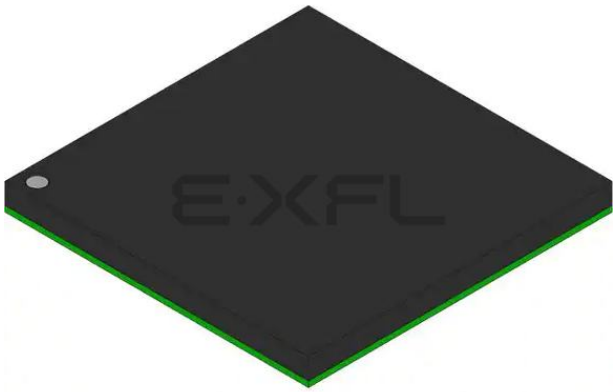

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx21cvk

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK, VM	T_A	0	70	°C
	DVK, DVM	T_A	-30	70	°C
	CVK, CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V

All timing is measured at 30 pF loading with the exception of fast I/O signals as discussed below. Refer to the reference manual's System Control Chapter for details on drive strength settings.

Table 8 provides the maximum loading guidelines that can be tolerated on a memory I/O signal (also known as Fast I/O) to achieve 133 MHz operation. These critical signals include the SDRAM Clock (SDCLK), Data Bus signals (D[31:0]), lower order address signals such as A0-A10, MA10, MA11, and other signals required to meet 133 MHz timing.

The values shown in Table 8 apply over the recommended operating temperature range. Care must be taken to minimize parasitic capacitance of associated printed circuit board traces.

Table 8. Loading Guidelines for Fast IO Signals to Achieve 133 MHz Operation

Drive Strength Setting (DSCR2–DSCR12)	Maximum I/O Loading at 1.8 V	Maximum I/O Loading at 3.0 V
000: 3.5 mA	9 pF	12 pF
001: 4.5 mA	12 pF	16 pF
011: 5.5 mA	15 pF	21 pF
111: 6.5 mA	19 pF	26 pF

Table 9. 32k/26M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak) for both System PLL and MCUPLL	–	5	20	ns
EXTAL32k input jitter (peak to peak) for MCUPLL only	–	5	100	ns
EXTAL32k startup time	800	–	–	ms

Table 10. CLKO Rise/Fall Time (at 30pF Loaded)

	Best Case	Typical	Worst Case	Units
Rise Time	0.80	1.00	1.40	ns
Fall Time	0.74	1.08	1.67	ns

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–

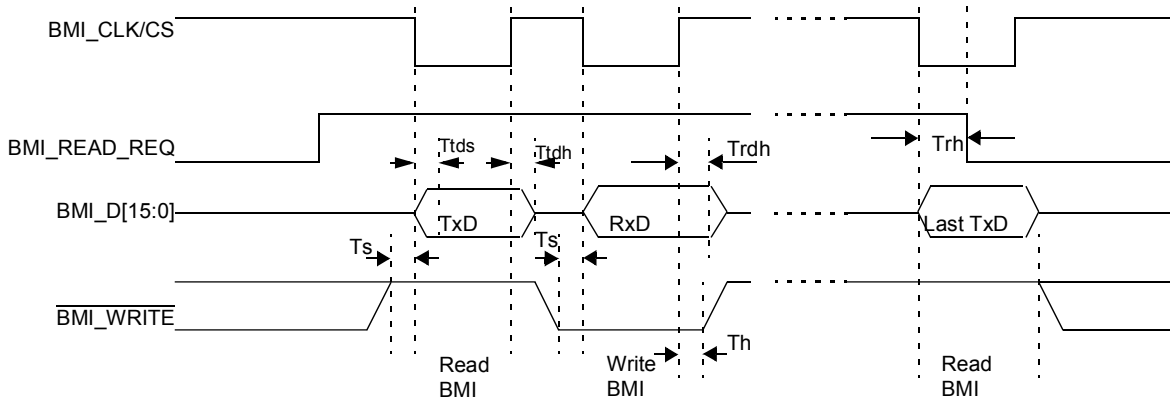

Figure 10. Memory Interface Slave Mode, External Bus Master Read/Write to BMI Timing (MMD_MODE_SEL=0, MASTER_MODE_SEL=0)

Table 18. External Bus Master Read/Write to BMI Timing Table

Item	Symbol	Minimum	Typical	Maximum	Unit
$\overline{\text{Write}}$ setup time	Ts	11	–	–	ns
$\overline{\text{Write}}$ hold time	Th	0	–	–	ns
Receive data hold time	Trdh	3	–	–	ns
Transfer data setup time	Ttds	6	–	14	ns
Transfer data hold time	Ttdh	6	–	14	ns
Read_req hold time	Trh	6	–	24	ns

Note: All the timings are assumed that the hclk is running at 133 MHz.

3.8.3 Connecting BMI to External Bus Slave Devices

In this mode the $\overline{\text{BMI\_WRITE}}$, $\overline{\text{BMI\_READ}}$ and BMI_CLK/CS are output signals driving by the BMI module. The output signal BMI_READ_REQ is still driving active-in on a write cycle, but it can be ignored in this case. Instead, it is used to trigger internal logic to generate the read or write signals. Data write cycles are continuously generated when TxFIFO is not emptied.

To issue a read cycle, the user can write a value of 1 to the READ bit of control register. This bit is cleared automatically when the read operation is completed. A read cycle reads COUNT+1 data from the external bus slave. The user can write a 1 to the READ bit while there is still data in the TxFIFO, but the read cycle will not start until all data in the TxFIFO is emptied. If the read cycle begins, the write operation also cannot begin until this read cycle complete.

In this master mode operation, Int_Clk is derived from HCLK through an integer divider DIV of BMI control register and it is used to control the read/write cycle timing by generate $\overline{\text{WRITE}}$ and CLK/CS signals.

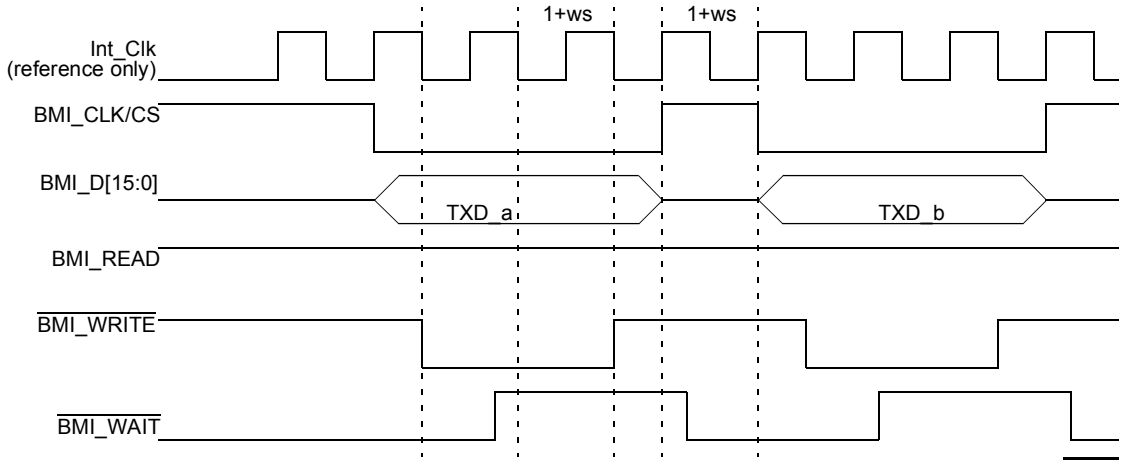

Figure 12. Memory Interface Master Mode, BMI Write to External Slave Device Timing with Wait Signal (MMD_MODE_SEL=0, MASTER_MODE_SEL=1,WAIT=1)

Figure 13 shows the BMI read timing when the WAIT bit is set. As write timing, when the BMI_READ is asserted, the BMI will detect the BMI_WAIT signal on every falling edge of the Int_Clk. When it detected the high level of the BMI_WAIT, the BMI_READ will be negated after 1+WS Int_Clk period. If the BMI_WAIT is always high or already high before BMI_READ is asserted, this timing will same as without WAIT signal. So the BMI_READ will be asserted at least for 1+WS Int_Clk period.

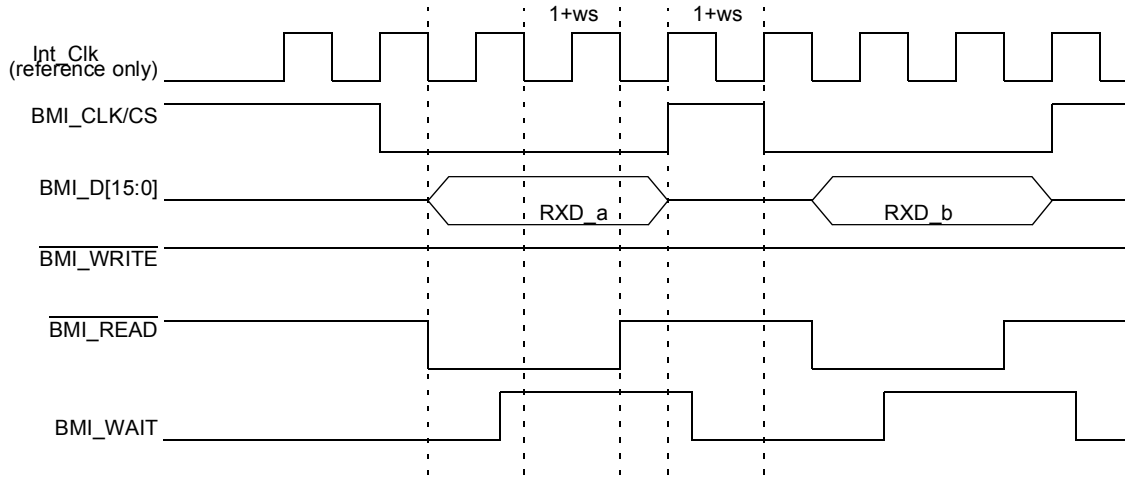

Figure 13. Memory Interface Master Mode, BMI Read to External Slave Device Timing with Wait Signal (MMD_MODE_SEL=0, MASTER_MODE_SEL=1,WAIT=1)

3.9 CSPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the CSPI1 module is configured as a master, two control signals are used for data transfer rate control: the SS signal (output) and the SPI_RDY signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either CSPI1 or CSPI2. When the CSPI1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external CSPI master's timing. In this configuration, SS

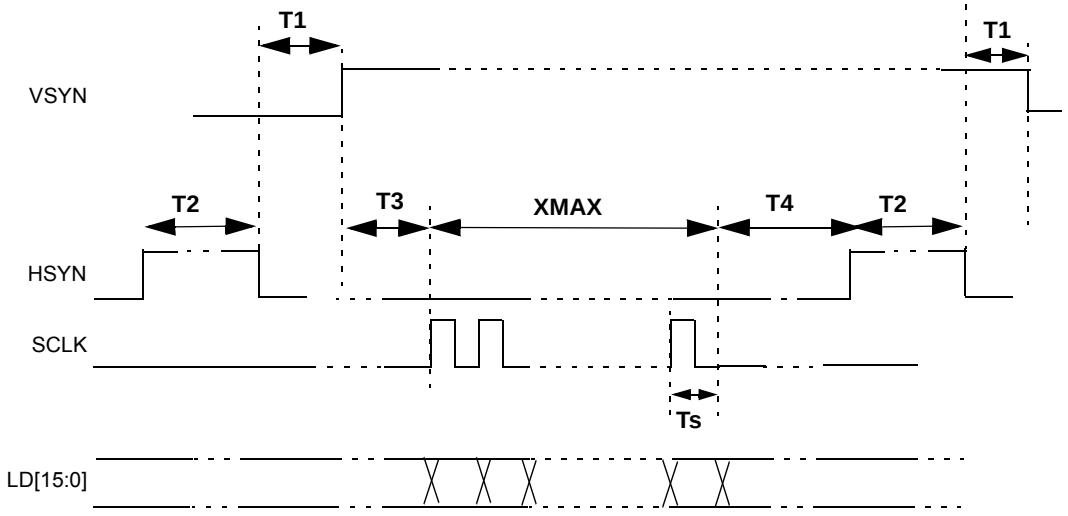

Figure 22. Non-TFT Mode Panel Timing

Table 23. Non-TFT Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	HSYN to VSYN delay	2	HWAIT2+2	Tpix
T2	HSYN pulse width	1	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts$	–
T4	SCLK to HSYN	1	HWAIT1+1	Tpix

Note:
- Ts is the SCLK period while Tpix is the pixel clock period.
- VSYN, HSYN and SCLK can be programmed as active high or active low. In Figure 67, all these 3 signals are active high.
- When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts.
- When it is in monochrome mode with bus width = 2, 4, and 8, T3 = 1, 2 and 4 Tpix respectively.

3.12 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

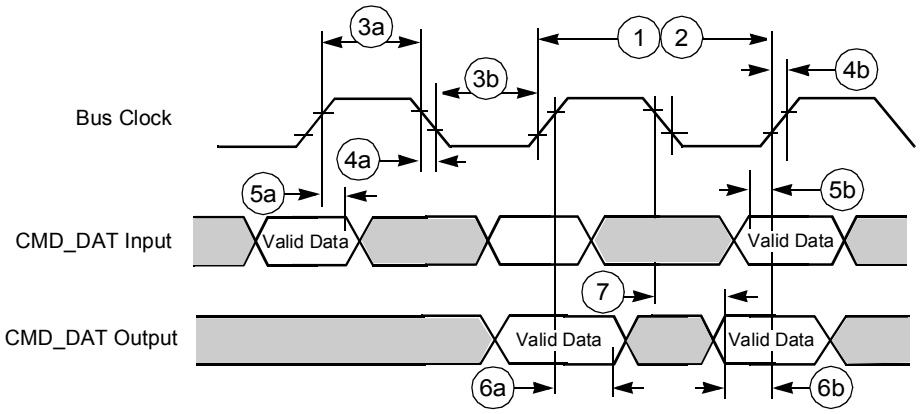

Figure 25. Chip-Select Read Cycle Timing Diagram

Table 26. SDHC Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Min	Max	Min	Max	
1	CLK frequency at Data transfer Mode (PP)[1]—10/30 cards	0	25/5	0	25/5	MHz
2	$\overline{\text{CLK}}$ frequency at Identification Mode[2]	0	400	0	400	kHz
3a	Clock high time[1]—10/30 cards	6/33	–	10/50	–	ns
3b	Clock low time[1]—10/30 cards	15/75	–	10/50	–	ns
4a	Clock fall time[1]—10/30 cards	–	10/50 (5.00)[3]	–	10/50	ns
4b	Clock rise time[1]—10/30 cards	–	14/67 (6.67)[3]	–	10/50	ns
5a	Input hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
5b	Input setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6a	Output hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6b	Output setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
7	Output delay time[3]	0	16	0	14	ns

1. $C_L \leq 100$ pF / 250 pF (10/30 cards)
2. $C_L \leq 250$ pF (21 cards)
3. $C_L \leq 25$ pF (1 card)

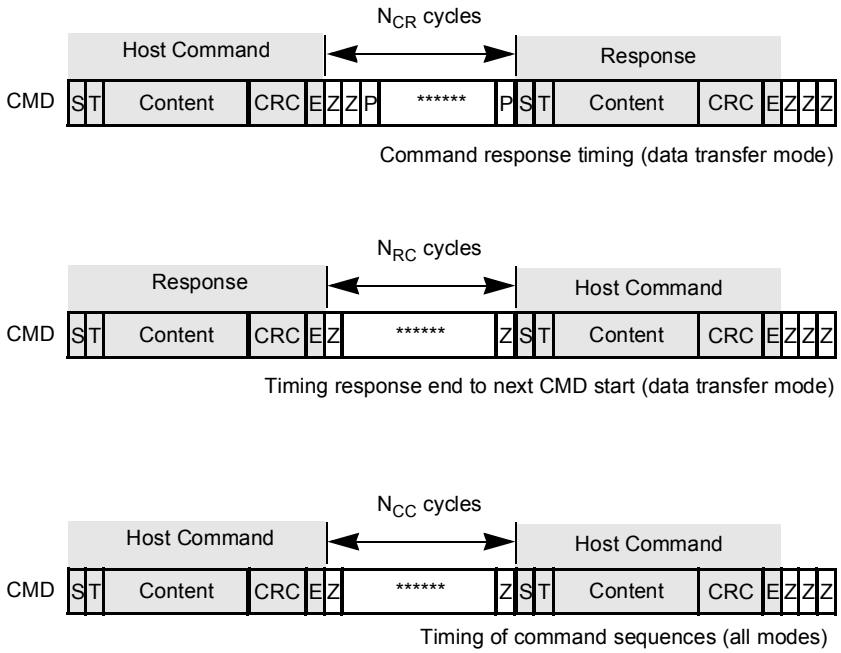

Figure 27. Timing Diagrams at Data Transfer Mode

Figure 28 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC}, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

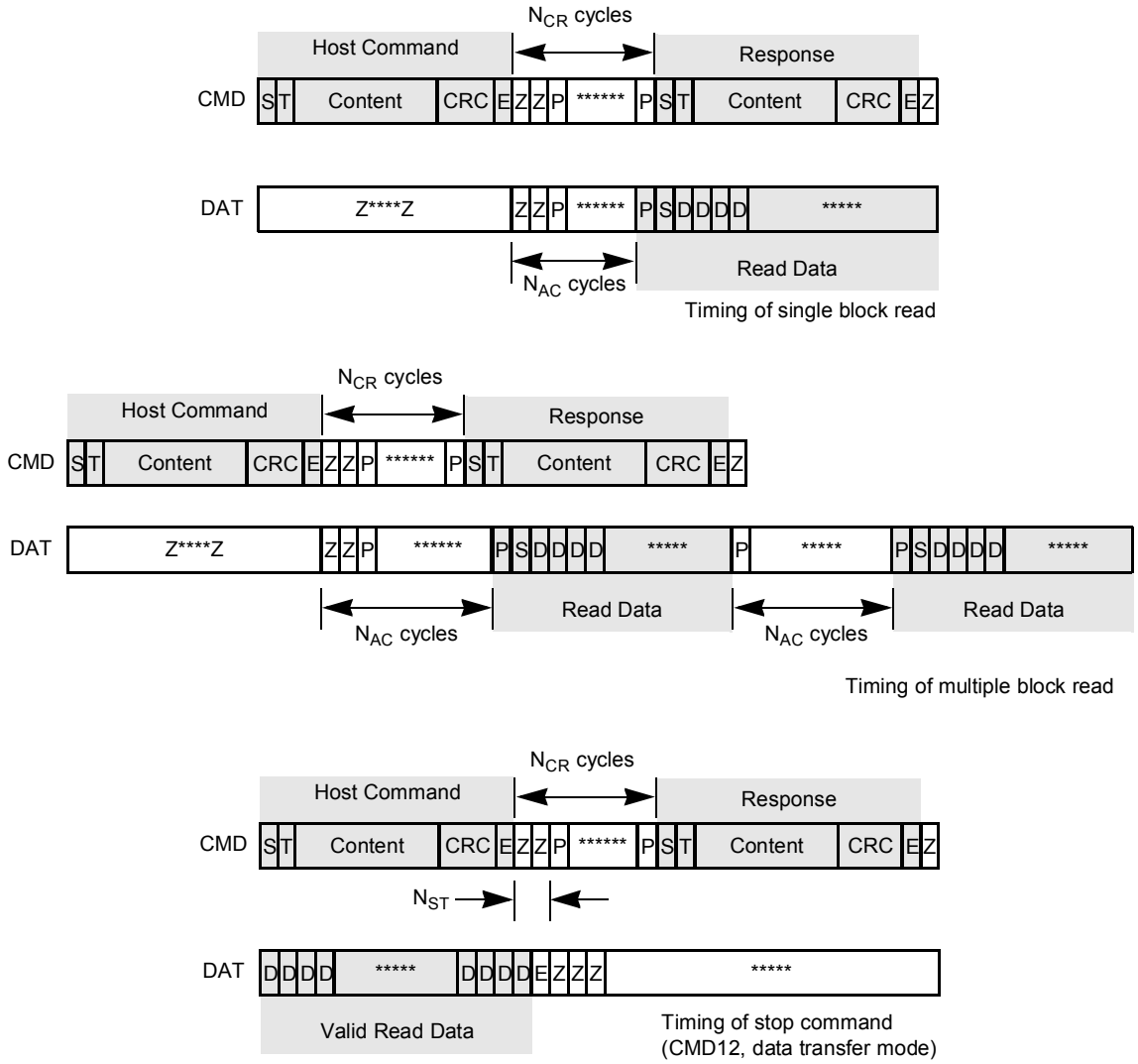

Figure 28. Timing Diagrams at Data Read

Figure 29 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

Table 29. NFC Target Timing Parameters[1],[2]

ID	Parameter	Symbol	Relationship to NFC Clock Period (T)		NFC Clock 22.17 MHz T = 45 ns		NFC Clock 33.25 MHz T = 30 ns		Unit
			Min	Max	Min	Max	Min	Max	
NF1	NFCLE Setup Time	tCLS	T	–	45	–	30	–	ns
NF2	NFCLE Hold Time	tCLH	T	–	45	–	30	–	ns
NF3	$\overline{\text{NFCE}}$ Setup Time	tCS	T	–	45	–	30	–	ns
NF4	$\overline{\text{NFCE}}$ Hold Time	tCH	T	–	45	–	30	–	ns
NF5	$\overline{\text{NF\_WP}}$ Pulse Width	tWP	T	–	45	–	30	–	ns
NF6	NFALE Setup Time	tALS	T	–	45	–	30	–	ns
NF7	NFALE Hold Time	tALH	T	–	45	–	30	–	ns
NF8	Data Setup Time	tDS	T	–	45	–	30	–	ns
NF9	Data Hold Time	tDH	T	–	45	–	30	–	ns
NF10	Write Cycle Time	tWC	2T	–	90	–	60	–	ns
NF11	$\overline{\text{NFWE}}$ Hold Time	tWH	T	–	45	–	30	–	ns
NF12	Ready to $\overline{\text{NFRE}}$ Low	tRR	4T	–	180	–	120	–	ns
NF13	$\overline{\text{NFRE}}$ Pulse Width	tRP	1.5T	–	67.5	–	45	–	ns
NF14	READ Cycle Time	tRC	2T	–	90	–	60	–	ns
NF15	$\overline{\text{NFRE}}$ High Hold Time	tREH	0.5T	–	22.5	–	15	–	ns
NF16	Data Setup on READ	tDSR	15	–	15	–	15	–	ns
NF17	Data Hold on READ	tDHR	0	–	0	–	0	–	ns

1. High is defined as 80% of signal value and low is defined as 20% of signal value. All timings are listed according to this NFC clock frequency (multiples of NFC clock period) except NF16, which is not NFC clock related.
2. The read data is generated by the NAND Flash device and sampled with the internal NFC clock.

Table 37. SSI to SSI3 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	(Tx) CK high to STXD high impedance	9.02	16.46	7.29	14.97	ns
29	SRXD setup time before (Rx) CK low	1.49	–	1.49	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI3 Ports)						
31	SRXD setup before (Tx) CK falling	21.99	–	21.99	–	ns
32	SRXD old fter Txh) Kafalling C	0	–	0	–	ns
Synchronous External Clock Operation (SSI3 Ports)						
33	SRXD setup before (Tx) CK falling	3.80	–	3.80	–	ns
34	SRXD old fter Txh) Kafalling C	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

3.17 1-Wire Interface Timing

3.17.1 Reset Sequence with Reset Pulse Presence Pulse

To begin any communications with the DS2502, it is required that an initialization procedure be issued. A reset pulse must be generated and then a presence pulse must be detected. The minimum reset pulse length is 480 us. The bus master (one-wire) will generate this pulse, then after the DS2502 detects a rising edge on the one-wire bus, it will wait 15-60 us before it will transmit back a presence pulse. The presence pulse will exist for 60-240 us.

The timing diagram for this sequence is shown in Figure 46.

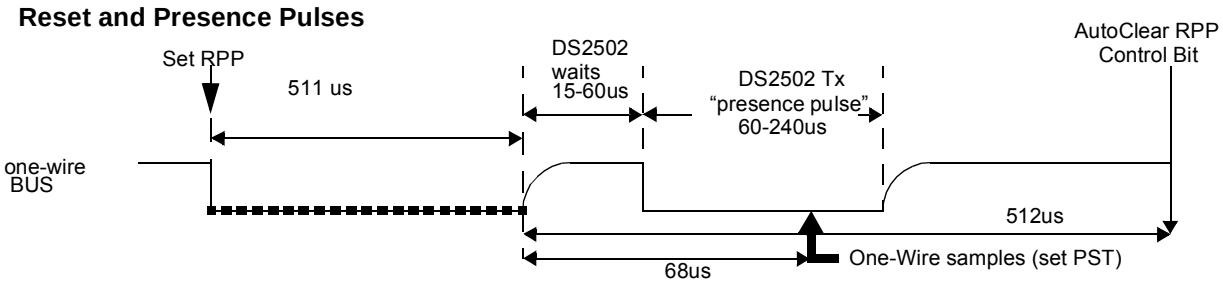

Figure 46. 1-Wire Initialization

The reset pulse begins the initialization sequence and it is initiated when the RPP control register bit is set. When the presence pulse is detected, this bit will be cleared. The presence pulse is used by the bus master to determine if at least one DS2502 is connected. Software will determine if more than one DS2502 exists. The one-wire will sample for the DS2502 presence pulse. The presence pulse is latched in the one-wire

3.18 USB On-The-Go

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, but because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

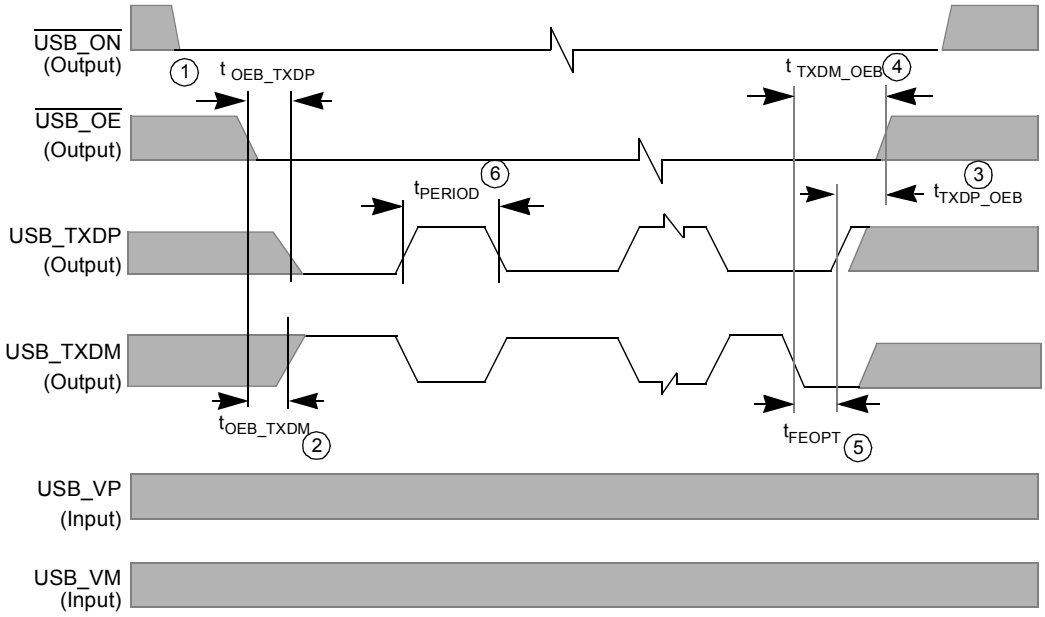

Figure 50. USB Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 40. USB Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{OEB_TXDP}; $\overline{USBD\_OE}$ active to USBD_TXDP low	83.14	83.47	ns
2	t_{OEB_TXDM}; $\overline{USBD\_OE}$ active to USBD_TXDM high	81.55	81.98	ns
3	t_{TXDP_OEB}; USBD_TXDP high to $\overline{USBD\_OE}$ deactivated	83.54	83.8	ns
4	t_{TXDM_OEB}; USBD_TXDM low to $\overline{USBD\_OE}$ deactivated (includes SE0)	248.9	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160	175	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

Table 43. EIM Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V			1.8 V ± 0.1 V	Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	3.97	6.02	9.89	3.83	5.89	9.79	ns
1b	Clock fall to address invalid	3.93	6.00	9.86	3.81	5.86	9.76	ns
2a	Clock fall to chip-select valid	3.47	5.59	8.62	3.30	5.09	8.45	ns
2b	Clock fall to chip-select invalid	3.39	5.09	8.27	3.15	4.85	8.03	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	3.51	5.56	8.79	3.39	5.39	8.51	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	3.59	5.37	9.14	3.36	5.20	8.50	ns
4a	Clock[1] rise to Output Enable Valid	3.62	5.49	8.98	3.46	5.33	9.02	ns
4b	Clock[1] rise to Output Enable Invalid	3.70	5.61	9.26	3.46	5.37	8.81	ns
4c	Clock[1] fall to Output Enable Valid	3.60	5.48	8.77	3.44	5.30	8.88	ns
4d	Clock[1] fall to Output Enable Invalid	3.69	5.62	9.12	3.42	5.36	8.60	ns
5a	Clock[1] rise to Enable Bytes Valid	3.69	5.46	8.71	3.46	5.25	8.54	ns
5b	Clock[1] rise to Enable Bytes Invalid	4.64	5.47	8.70	3.46	5.25	8.54	ns
5c	Clock[1] fall to Enable Bytes Valid	3.52	5.06	8.39	3.41	5.18	8.36	ns
5d	Clock[1] fall to Enable Bytes Invalid	3.50	5.05	8.27	3.41	5.18	8.36	ns
6a	Clock[1] fall to Load Burst Address Valid	3.65	5.28	8.69	3.30	5.23	8.81	ns
6b	Clock[1] fall to Load Burst Address Invalid	3.65	5.67	9.36	3.41	5.43	9.13	ns
6c	Clock[1] rise to Load Burst Address Invalid	3.66	5.69	9.48	3.33	5.47	9.25	ns
7a	Clock[1] rise to Burst Clock rise	3.50	5.22	8.42	3.26	4.99	8.19	ns
7b	Clock[1]rise to Burst Clock fall	3.49	5.19	8.30	3.31	5.03	8.17	ns
7c	Clock[1] fall to Burst Clock rise	3.50	5.22	8.39	3.26	4.98	8.15	ns
7d	Clock[1] fall to Burst Clock fall	3.49	5.19	8.29	3.31	5.02	8.12	ns
8a	Read Data setup time	4.54	–	–	4.54	–	–	ns
8b	Read Data hold time	0.5	–	–	0.5	–	–	ns
9a	Clock[1] rise to Write Data Valid	4.13	5.86	9.16	3.95	6.36	10.31	ns
9b	Clock[1] fall to Write Data Invalid	4.10	5.79	9.15	4.04	6.27	9.16	ns
9c	Clock[1] rise to Write Data Invalid	4.02	5.81	9.37	4.22	5.29	9.24	ns
10a	DTACK setup time	2.65	4.63	8.40	2.64	4.61	8.41	ns
11	Burst Clock (BCLK) cycle time	15	–	–	15	–	–	ns

1. Clock refers to the system clock signal, HCLK, generated from the System DPLL

Note: Signals listed with lower case letters are internal to the device.

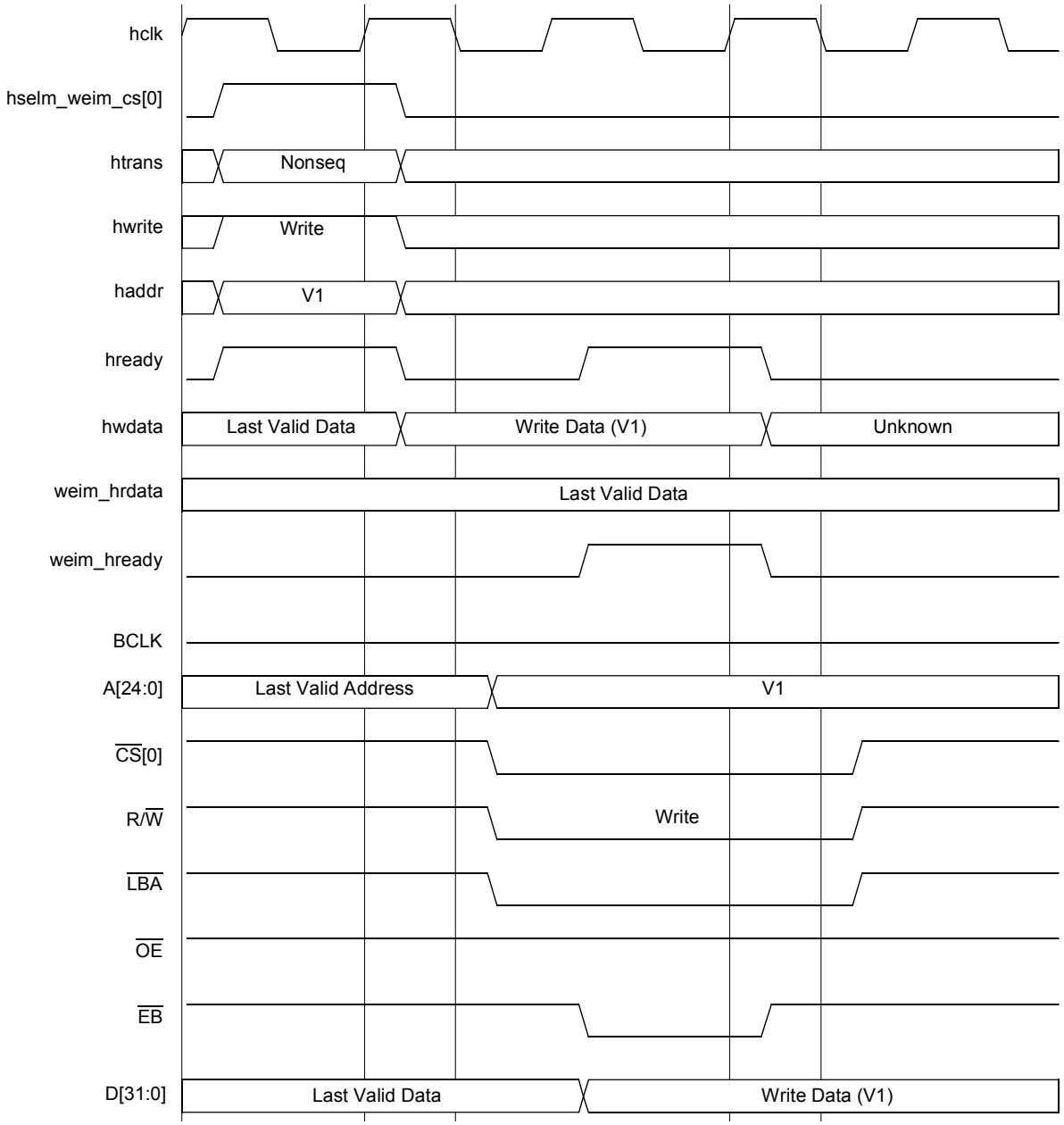

Figure 55. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

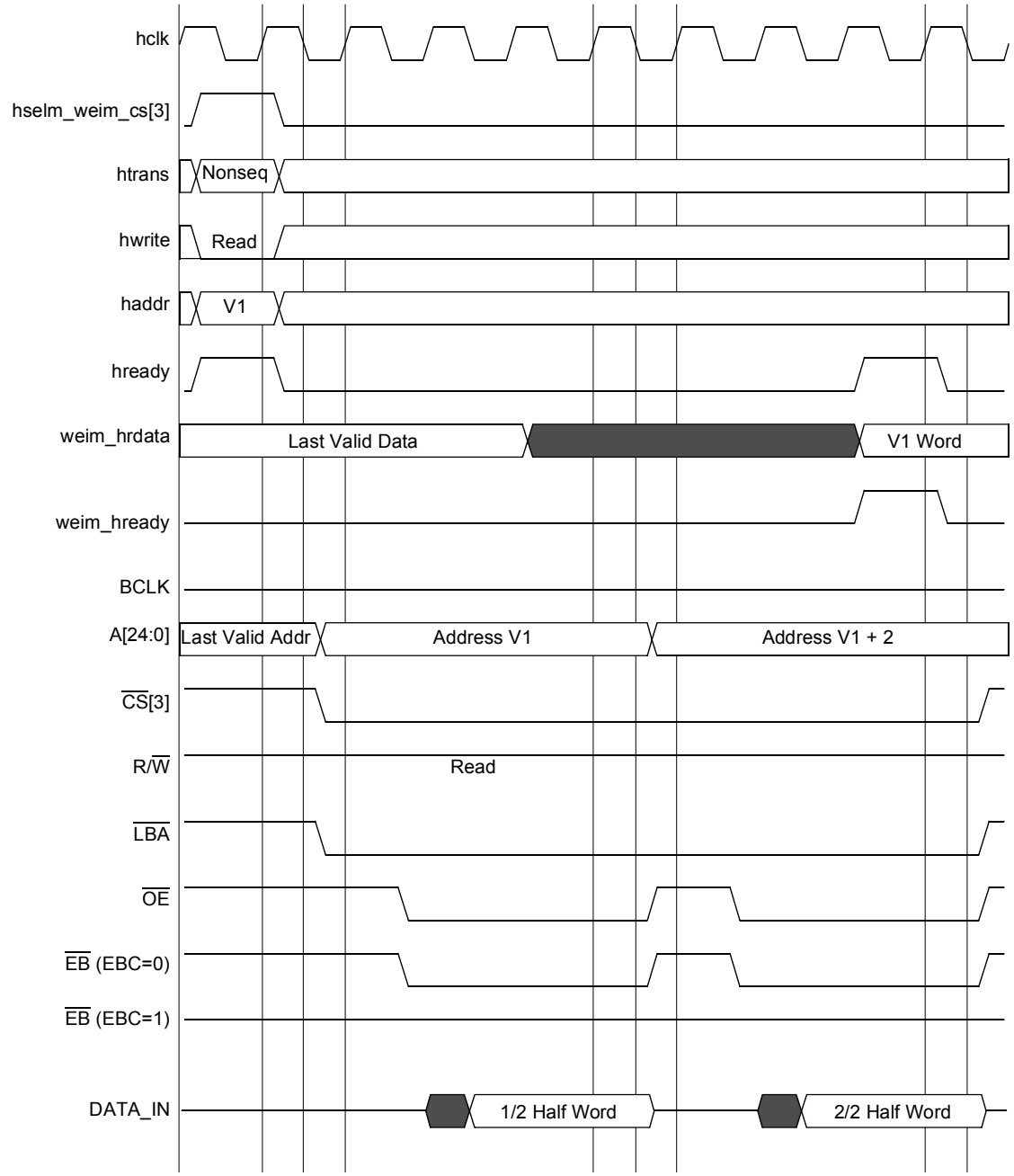

Figure 58. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

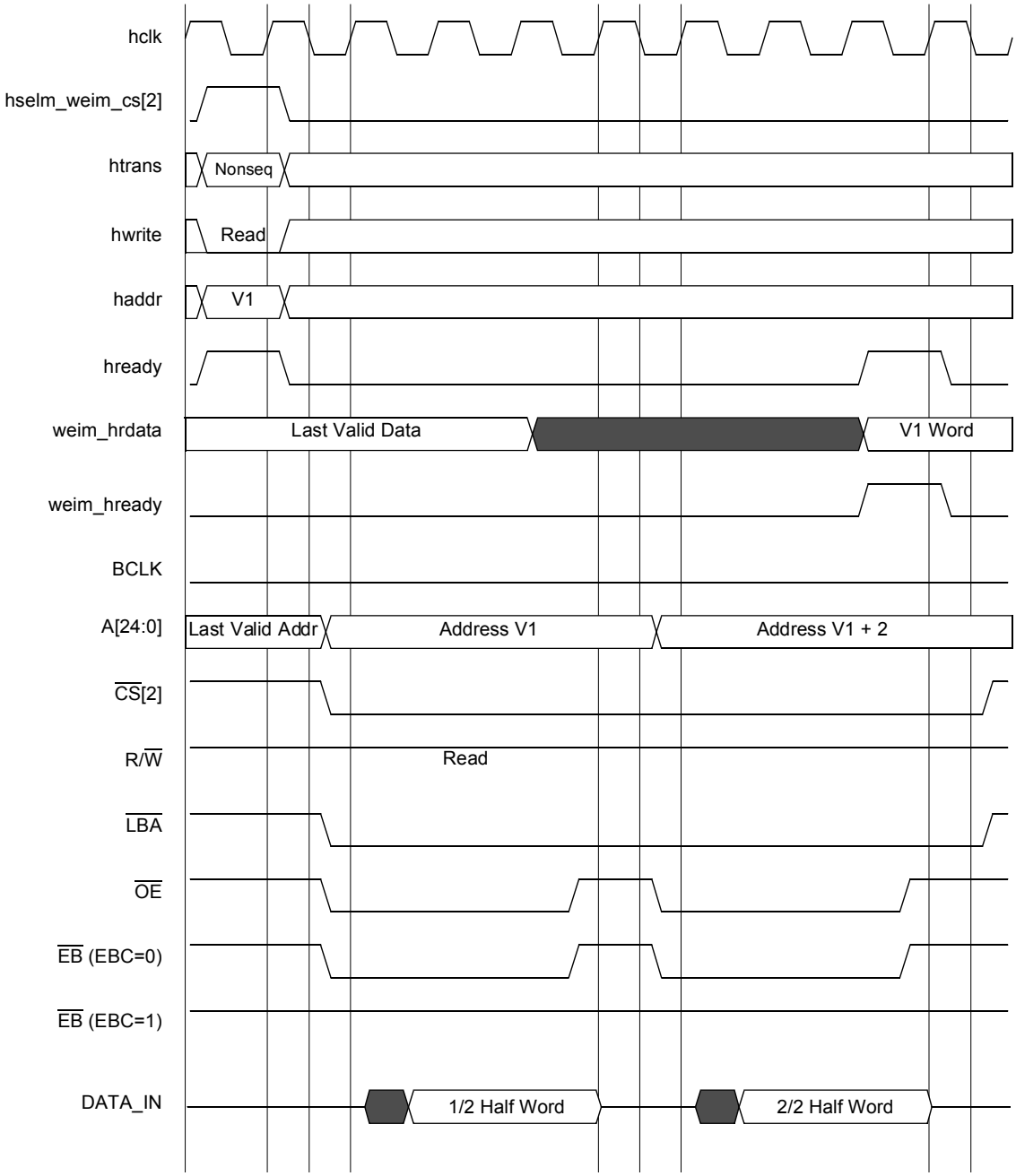

Figure 62. WSC = 3, OEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

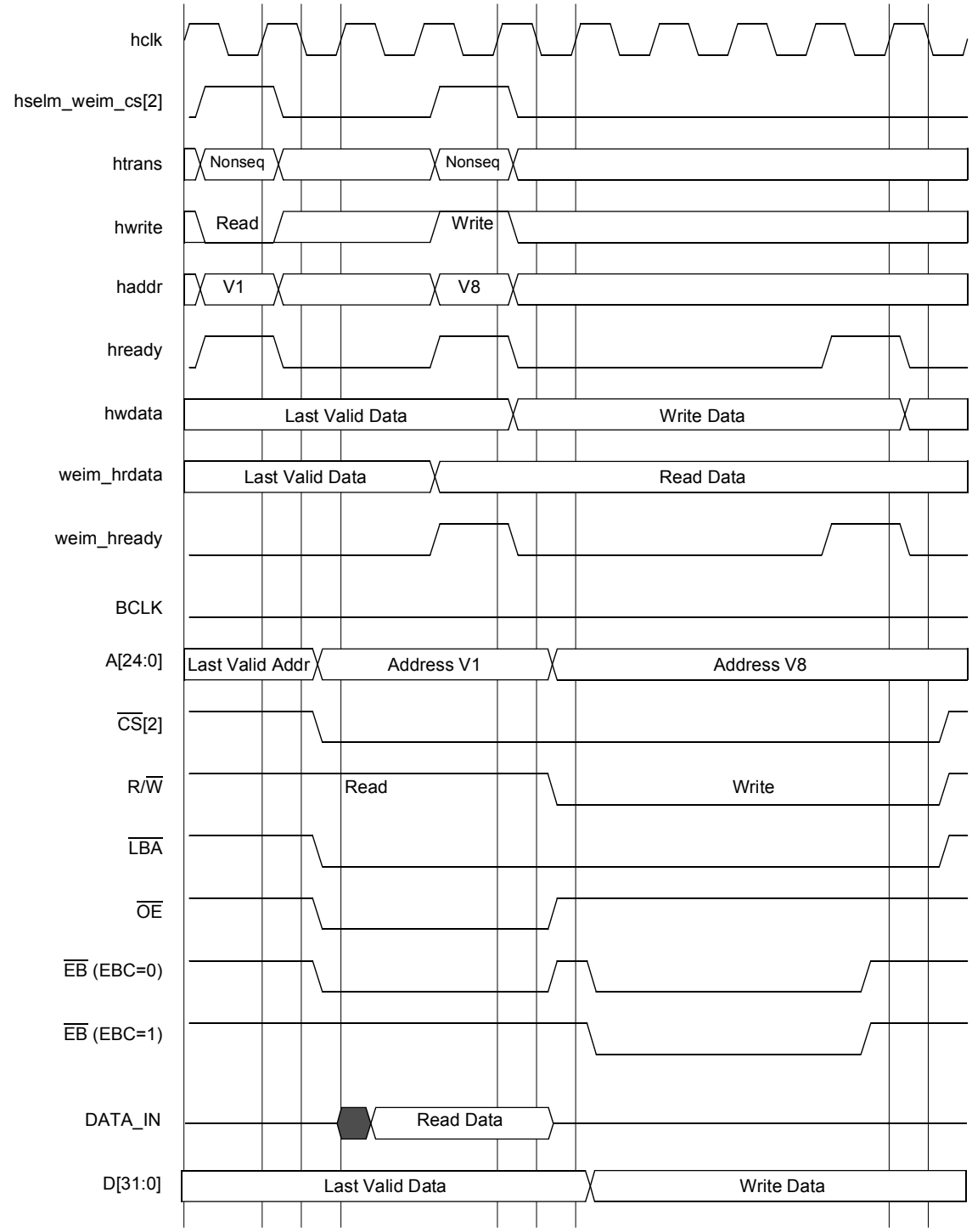

Figure 66. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

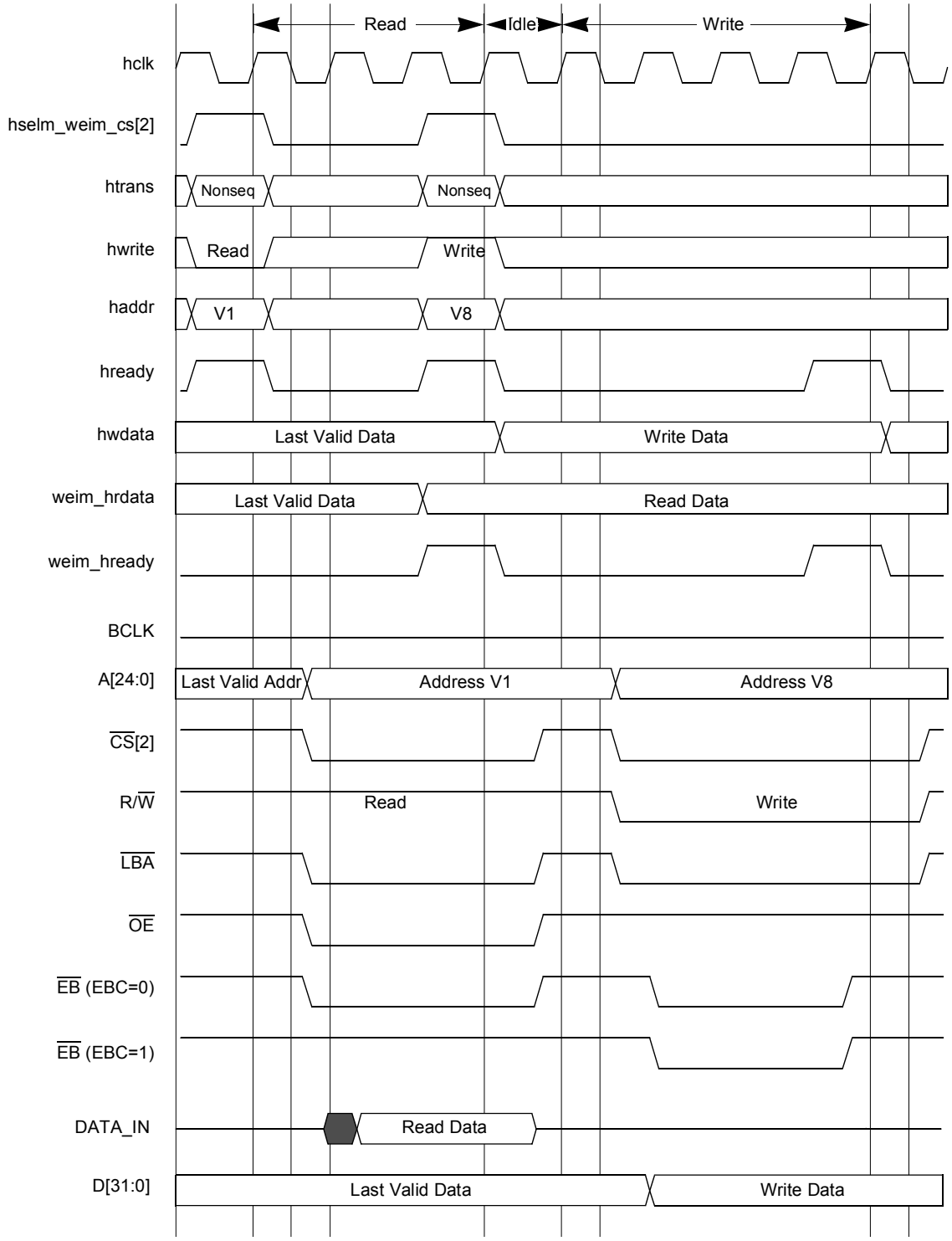

Figure 67. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

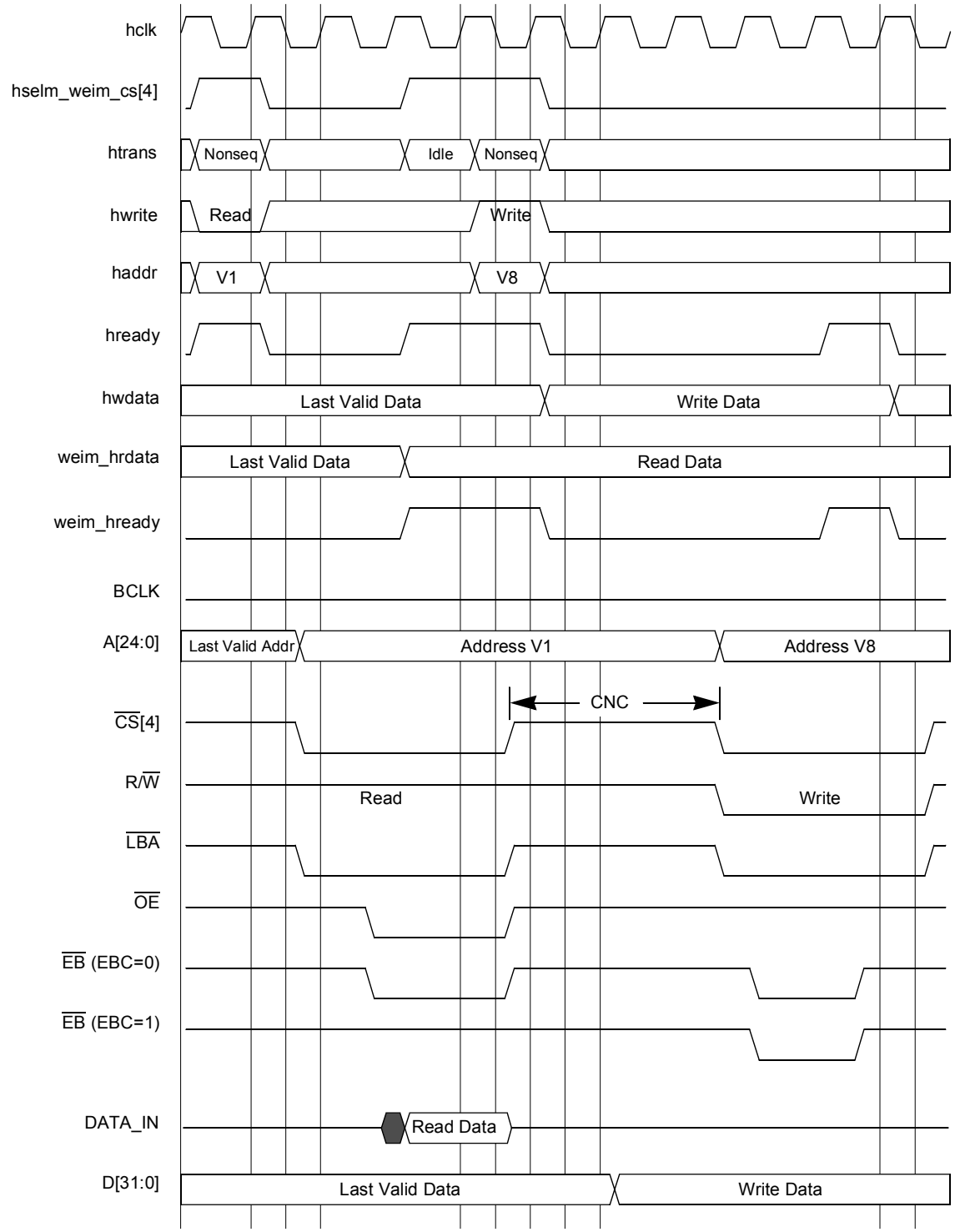

Figure 71. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

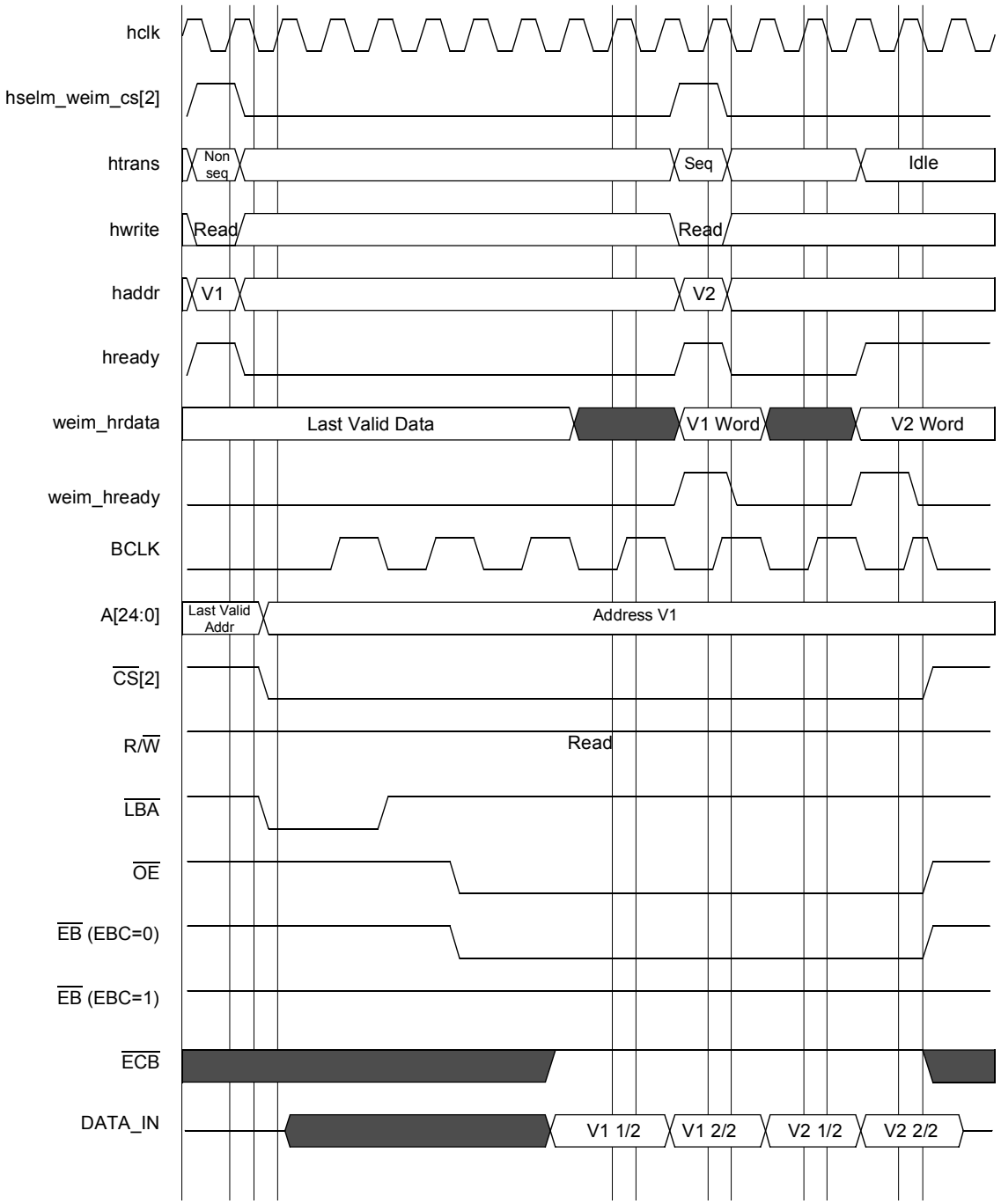

Figure 75. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF

3.20 DTACK Mode Memory Access Timing Diagrams

When enabled, the DTACK input signal is used to externally terminate a data transfer. For DTACK enabled operations, a bus time-out monitor generates a bus error when an external bus cycle is not terminated by the DTACK input signal after 1024 HCLK clock cycles have elapsed, where HCLK is the internal system clock driven from the PLL module. For a 133 MHz HCLK setting, this time equates to 7.7 µs. Refer to the Section 3.5, "DPLL Timing Specifications" for more information on how to generate different HCLK frequencies.

There are two modes of operation for the DTACK input signal: rising edge detection or level sensitive detection with a programmable insensitivity time. DTACK is only used during external asynchronous data transfers, thus the SYNC bit in the chip select control registers must be cleared.

During edge detection mode, the EIM will terminate an external data transfer following the detection of the DTACK signal's rising edge, so long as it occurs within the 1024 HCLK cycle time. Edge detection mode is used for devices that follow the PCMCIA standard. Note that DTACK rising edge detection mode can only be used for $\overline{CS}$[5] operations. To configure $\overline{CS}$[5] for DTACK rising edge detection, the following bits must be programmed in the Chip Select 5 Control Register and EIM Configuration Register:

- WSC bit field set to 0x3F and CSA (or CSN) set to 1 or greater in the Chip Select 5 Control Register
- AGE bit set in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device. The requirement of setting CSA or CSN is required to allow the EIM to wait for the rising edge of DTACK during back-to-back external transfers, such as during DMA transfers or an internal 32-bit access through an external 16-bit data port.

During level sensitive detection, the EIM will first hold off sampling the DTACK signal for at least 2 HCLK cycles, and up to 5 HCLK cycles as programmed by the DCT bits in the Chip Select Control Register. After this insensitivity time, the EIM will sample DTACK and if it detects that DTACK is logic high, it will continue the data transfer at the programmed number of wait states. However, if the EIM detects that DTACK is logic low, it will wait until DTACK goes to logic high to continue the access, so long as this occurs within the 1024 HCLK cycle time. If at anytime during an external data transfer DTACK goes to logic low, the EIM will wait until DTACK returns to logic high to resume the data transfer. Level detection is often used for asynchronous devices such graphic controller chips. Level detection may be used with any chip select except CS[4] as it is multiplexed with the DTACK signal. To configure a chip select for DTACK level sensitive detection, the following bits must be programmed in the Chip Select Control Register and EIM Configuration Register:

- EW bit set, WSC set to > 1, and CSN set to < 3 in the Chip Select Control Register
- BCD/DCT set to desired "insensitivity time" in the Chip Select Control Register. The "insensitivity time" is dictated by the external device's timing requirements.
- AGE bit cleared in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device.

The waveforms in the following section provide examples of the DTACK signal operation.