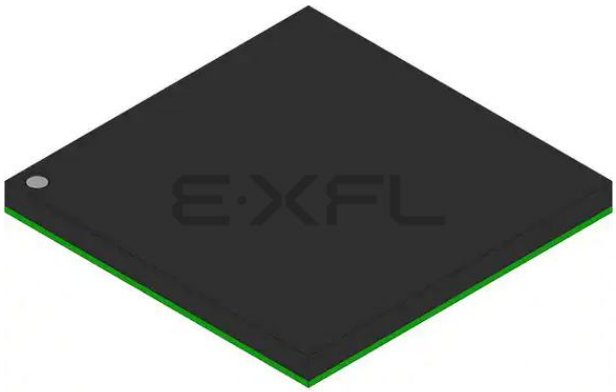

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx21dvk

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [17:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0] from SLCDC1 and BMI_D[15:0]. LD[17] signal is multiplexed with BMI_WRITE of BMI. LD[16] is multiplexed with BMI_READ_REQ of BMI and EXT_DMAGRANT.
FLM_VSYNC (or simply referred to as VSYNC)	Frame Sync or Vsync—This signal also serves as the clock signal output for gate driver (dedicated signal SPS for Sharp panel HR-TFT). This signal is multiplexed with BMI_RXF_FULL and BMI_WAIT of the BMI.
LP_HSYNC (or simply referred to as HSYNC)	Line Pulse or HSync
LSCLK	Shift Clock. This signal is multiplexed with the BMI_CLK_CS from BMI.
OE_ACD	Alternate Crystal Direction/Output Enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control. This signal is multiplexed with the BMI_READ from BMI.
SPL_SPR	Sampling start signal for left and right scanning. This signal is multiplexed with the SLCDC1_CLK.
PS	Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS.
CLS	Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS.
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0.
Smart LCD Controller	
SLCDC1_CLK	SLCDC Clock output signal. This signal is multiplexed and available at 2 alternate locations. These are SPL_SPR and SD2_CLK signals of LCDC and SD2, respectively.
SLCDC1_CS	SLCDC Chip Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are PS and SD2_CMD signals of LCDC and SD2, respectively.
SLCDC1_RS	SLCDC Register Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are CLS and SD2_D3 signals of LCDC and SD2, respectively.
SLCDC1_D0	SLCDC serial data output signal. This signal is multiplexed and available at 2 alternate signal locations. These are and REV and SD2_D2 signals of LCDC and SD2, respectively. This signal is inactive when a parallel data interface is used.
SLCDC1_DAT[15:0]	SLCDC Data output signals for connection to a parallel SLCD panel interface. These signals are multiplexed with LD[15:0] while an alternate 8-bit SLCD muxing is available on LD[15:8]. Further alternate muxing of these signals are available on some of the USB OTG and USBH1 signals.
SLCDC2_CLK	SLCDC Clock input signal for pass through to SLCD device. This signal is multiplexed with SSI3_CLK signal from SSI3.
SLCDC2_CS	SLCDC Chip Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_TXD signal from SSI3.
SLCDC2_RS	SLCDC Register Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_RXD signal from SSI3.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH2_FS	USB Host2 Full Speed output signal. This signal is multiplexed with CSPI2_SS[0] of CSPI2.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added. This signal is multiplexed with CSPI3_MOSI.
SD1_CLK	SD Output Clock. This signal is multiplexed with CSPI3_SCLK.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART2_RXD	Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP.
UART2_TXD	Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP.
$\overline{\text{UART2\_RTS}}$	Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP.
$\overline{\text{UART2\_CTS}}$	Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP.
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave

Table 5. DC Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
Input leakage current (no pull-up or pull-down)	I_{in}	V_{in} = 0 or NVDD	–	–	±1	µA
I/O leakage current	I_{OZ}	$V_{I/O}$ = NVDD or 0 I/O = High impedance state	–	–	±5	µA

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

Table 6. Input/Output Capacitance

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance	C_i	_	_	5	pF
Output capacitance	C_o	_	_	5	pF

Table 7 shows the power consumption for the device.

Table 7. Power Consumption

ID	Parameter	Conditions	Symbol	Typ	Max	Units
1	Run Current	QVDD = QVDDX = 1.65 V, NVDD1 = 1.8 V. NVDD2 through NVDD6 = VDDA = 3.1V. Core = 266 MHz, System = 133 MHz. MPEG4 Playback (QVGA) from MMC/SD card, 30fps, 44.1kHz audio.	I_{QVDD} + I_{QVDDX}	120	–	mA
			I_{NVDD1}	8	–	mA
			I_{NVDD2} through I_{NVDD6} + I_{VDDA}	6.6	–	mA
2	Sleep Current	Standby current with Well Biasing System enabled. Well Bias Control Register (WBCR) must be set as follows: WBCR: CRM_WBS bits = 01 CRM_WBFA bit = 1 CRM_WBM bits = 001 CRM_SPA_SEL bit = 1 FMCR bit = 1 For WBCR definition refer to System Control Chapter in the reference manual.	**I_{STBY}**			
			QVDD = QVDDX = 1.65V, TA[1]	–	3.0	mA
			QVDD = QVDDX = 1.65V, 25°	–	700	µA
			QVDD = QVDDX = 1.55V, 25°	320	–	µA

1. TA = 70°C for suffixes VK, VM, DVK, DVM, and SVK. TA = 85°C for suffixes CVK, CVM, and SCVK.

3.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency (HCLK) from 0 MHz to 133 MHz (core operating frequency 266 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H.

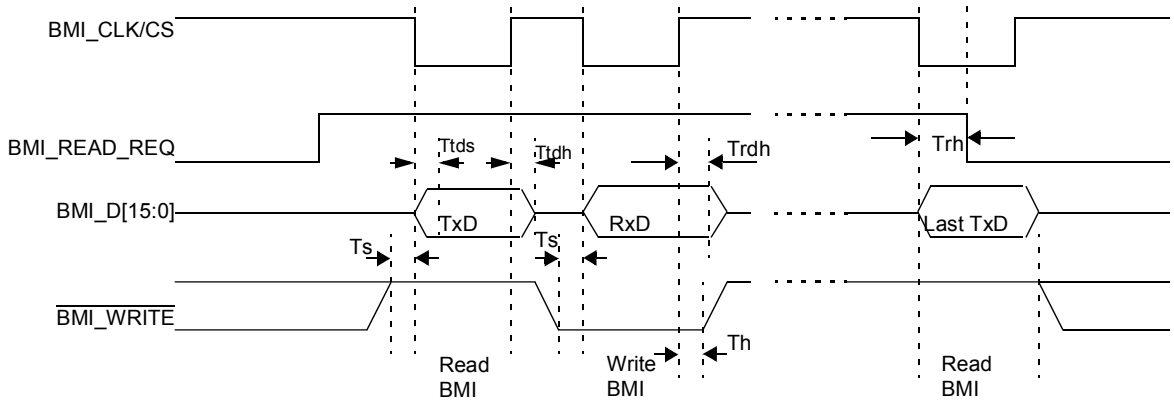

Figure 10. Memory Interface Slave Mode, External Bus Master Read/Write to BMI Timing (MMD_MODE_SEL=0, MASTER_MODE_SEL=0)

Table 18. External Bus Master Read/Write to BMI Timing Table

Item	Symbol	Minimum	Typical	Maximum	Unit
$\overline{\text{Write}}$ setup time	Ts	11	–	–	ns
$\overline{\text{Write}}$ hold time	Th	0	–	–	ns
Receive data hold time	Trdh	3	–	–	ns
Transfer data setup time	Ttds	6	–	14	ns
Transfer data hold time	Ttdh	6	–	14	ns
Read_req hold time	Trh	6	–	24	ns

Note: All the timings are assumed that the hclk is running at 133 MHz.

3.8.3 Connecting BMI to External Bus Slave Devices

In this mode the $\overline{\text{BMI\_WRITE}}$, $\overline{\text{BMI\_READ}}$ and BMI_CLK/CS are output signals driving by the BMI module. The output signal BMI_READ_REQ is still driving active-in on a write cycle, but it can be ignored in this case. Instead, it is used to trigger internal logic to generate the read or write signals. Data write cycles are continuously generated when TxFIFO is not emptied.

To issue a read cycle, the user can write a value of 1 to the READ bit of control register. This bit is cleared automatically when the read operation is completed. A read cycle reads COUNT+1 data from the external bus slave. The user can write a 1 to the READ bit while there is still data in the TxFIFO, but the read cycle will not start until all data in the TxFIFO is emptied. If the read cycle begins, the write operation also cannot begin until this read cycle complete.

In this master mode operation, Int_Clk is derived from HCLK through an integer divider DIV of BMI control register and it is used to control the read/write cycle timing by generate $\overline{\text{WRITE}}$ and CLK/CS signals.

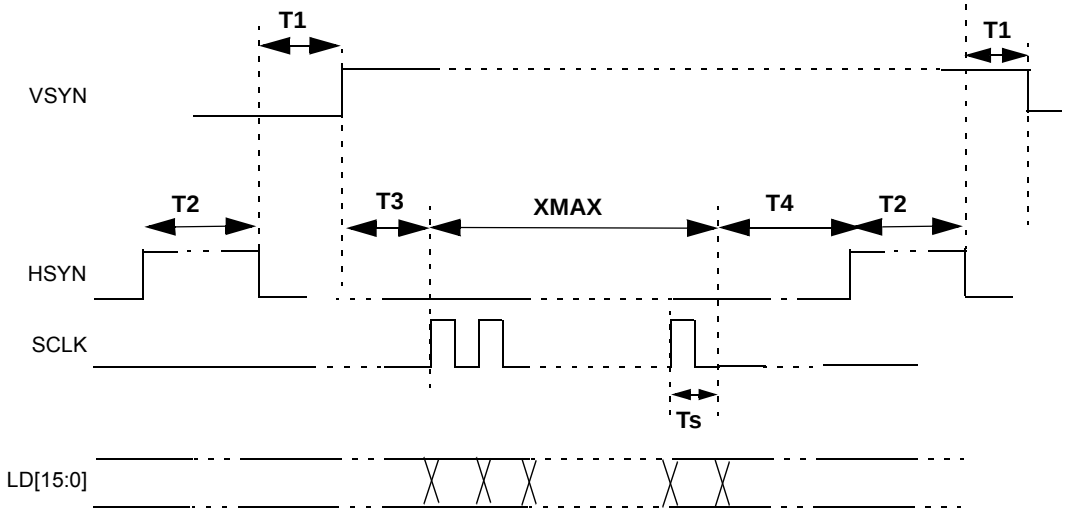

Figure 22. Non-TFT Mode Panel Timing

Table 23. Non-TFT Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	HSYN to VSYN delay	2	HWAIT2+2	Tpix
T2	HSYN pulse width	1	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts$	–
T4	SCLK to HSYN	1	HWAIT1+1	Tpix

Note:
- Ts is the SCLK period while Tpix is the pixel clock period.
- VSYN, HSYN and SCLK can be programmed as active high or active low. In Figure 67, all these 3 signals are active high.
- When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts.
- When it is in monochrome mode with bus width = 2, 4, and 8, T3 = 1, 2 and 4 Tpix respectively.

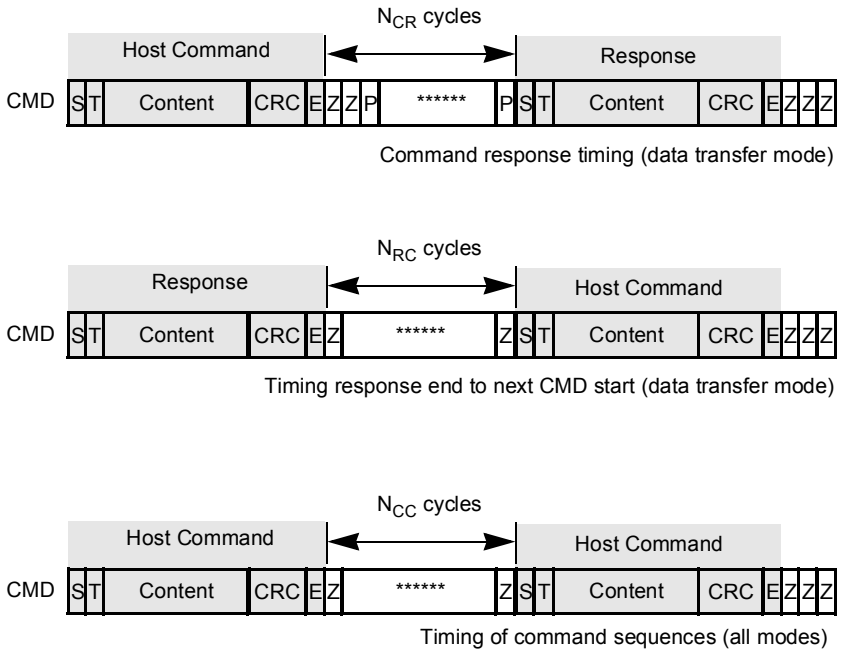

Figure 27. Timing Diagrams at Data Transfer Mode

Figure 28 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC}, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

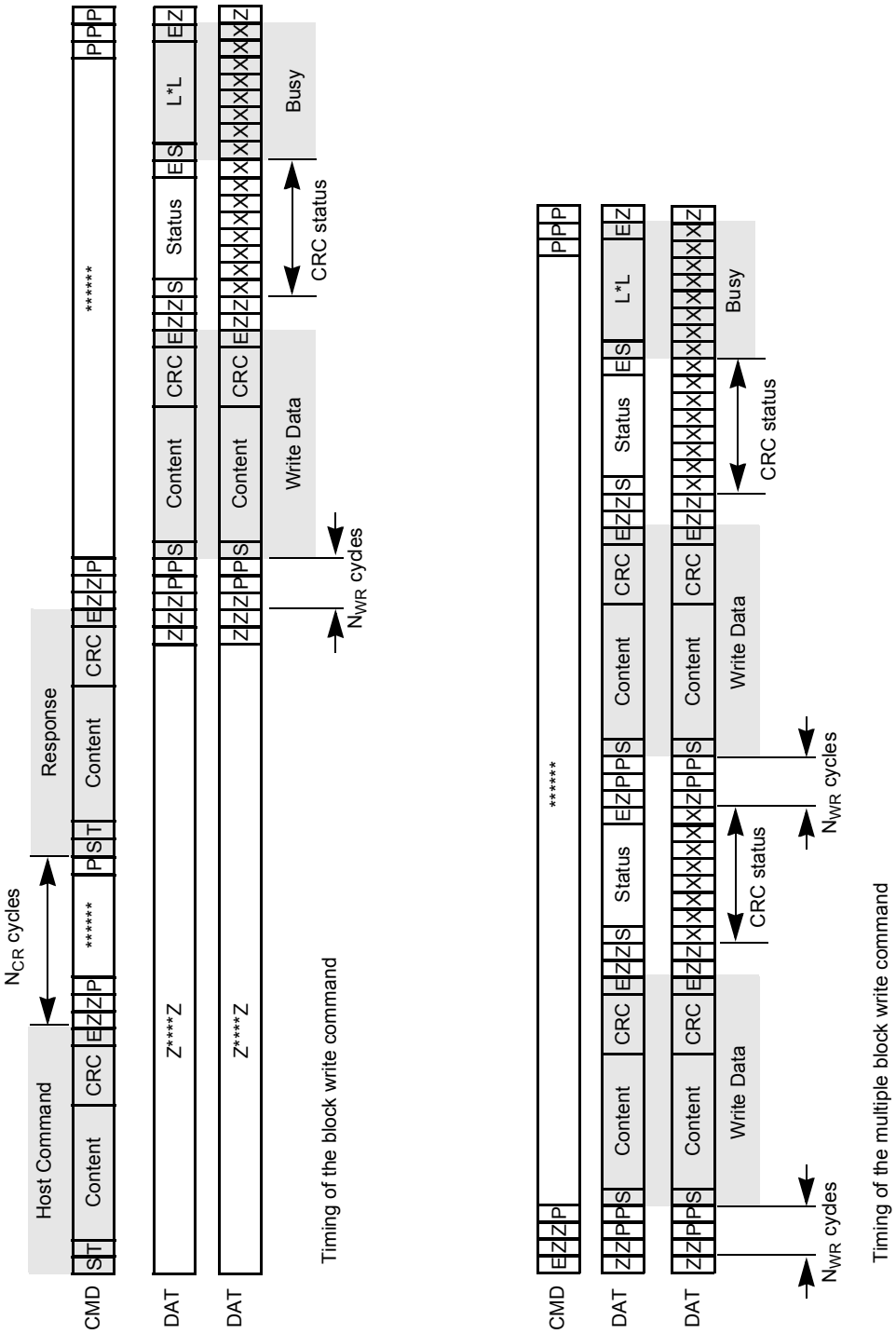

Figure 29. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 30 shows the different scenarios on the bus.

Table 28. Timing Values for Figure 26 through Figure 30 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]				

3.12.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the *Interrupt Period* during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

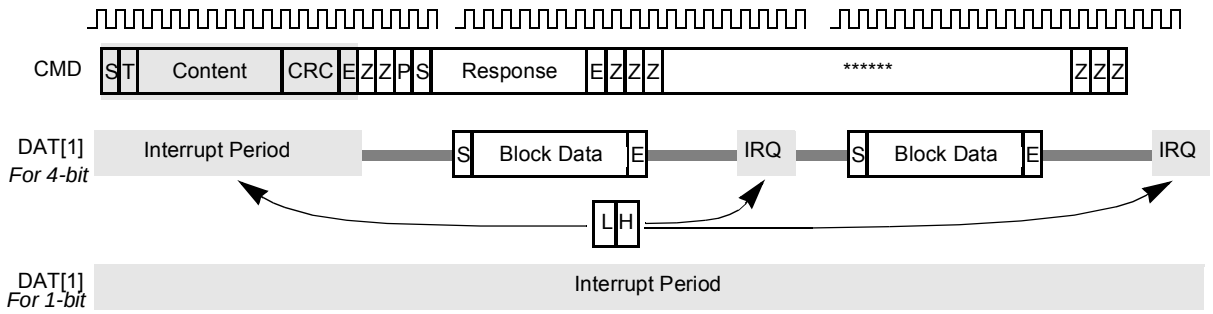

Figure 31. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

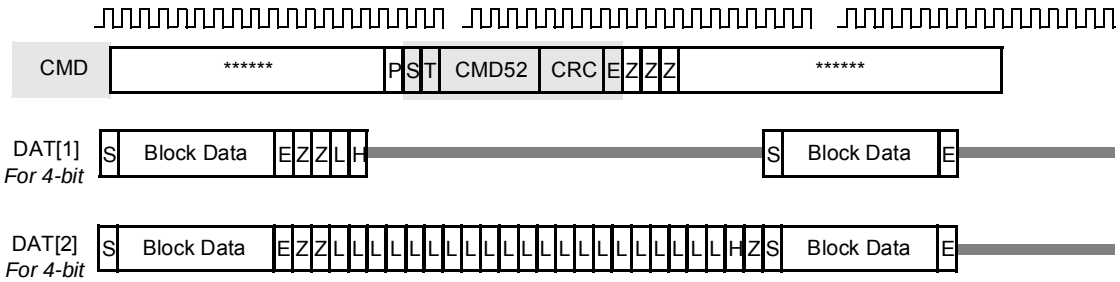

Figure 32. SDIO ReadWait Timing Diagram

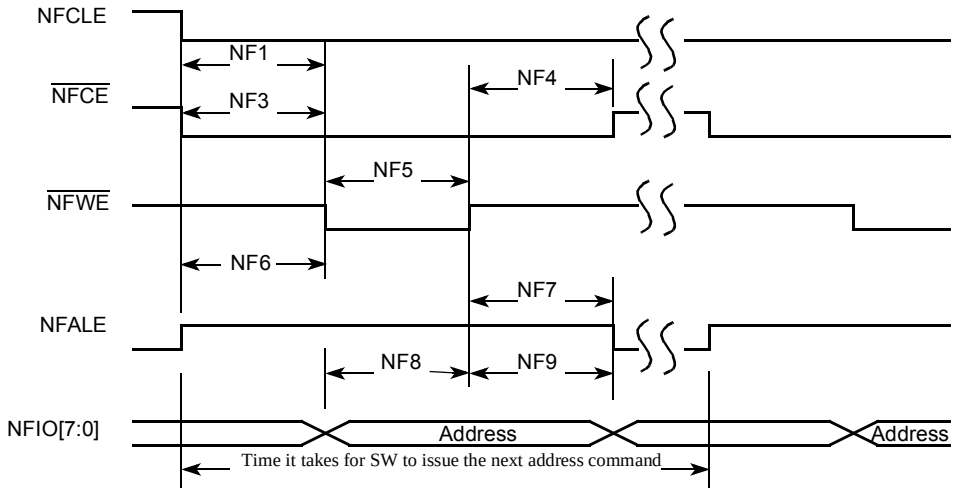

Figure 34. Address Latch Cycle Timing Diagram

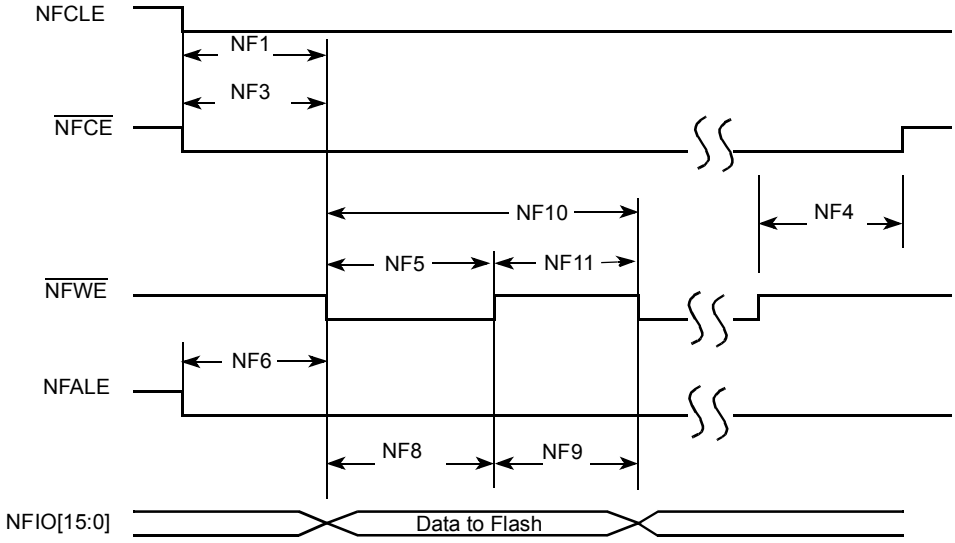

Figure 35. Write Data Latch Timing Diagram

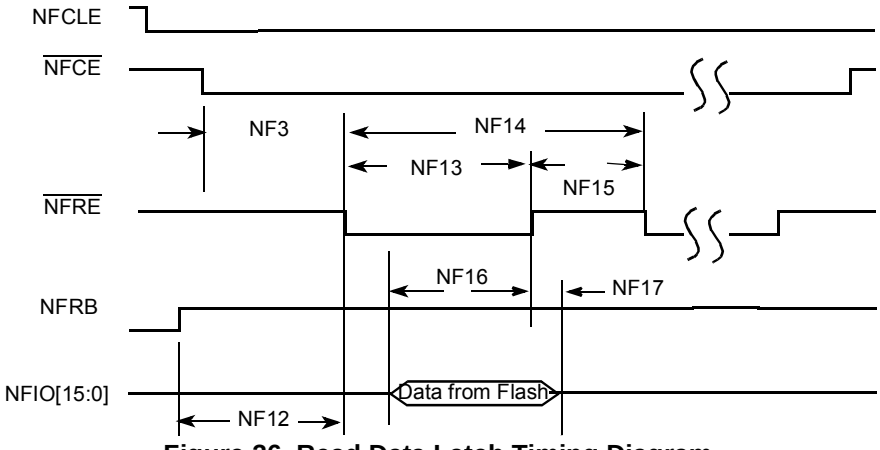

Figure 36. Read Data Latch Timing Diagram

Table 33. SDRAM Refresh Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	$\overline{\text{SDRAM clock low-level width}}$	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
4	Address setup time	3.67	–	2	–	ns
5	Address hold time	2.95	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP}[1]	–	ns
7	Auto precharge command period	t_{RC}[1]	–	t_{RC}[1]	–	ns

1. t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

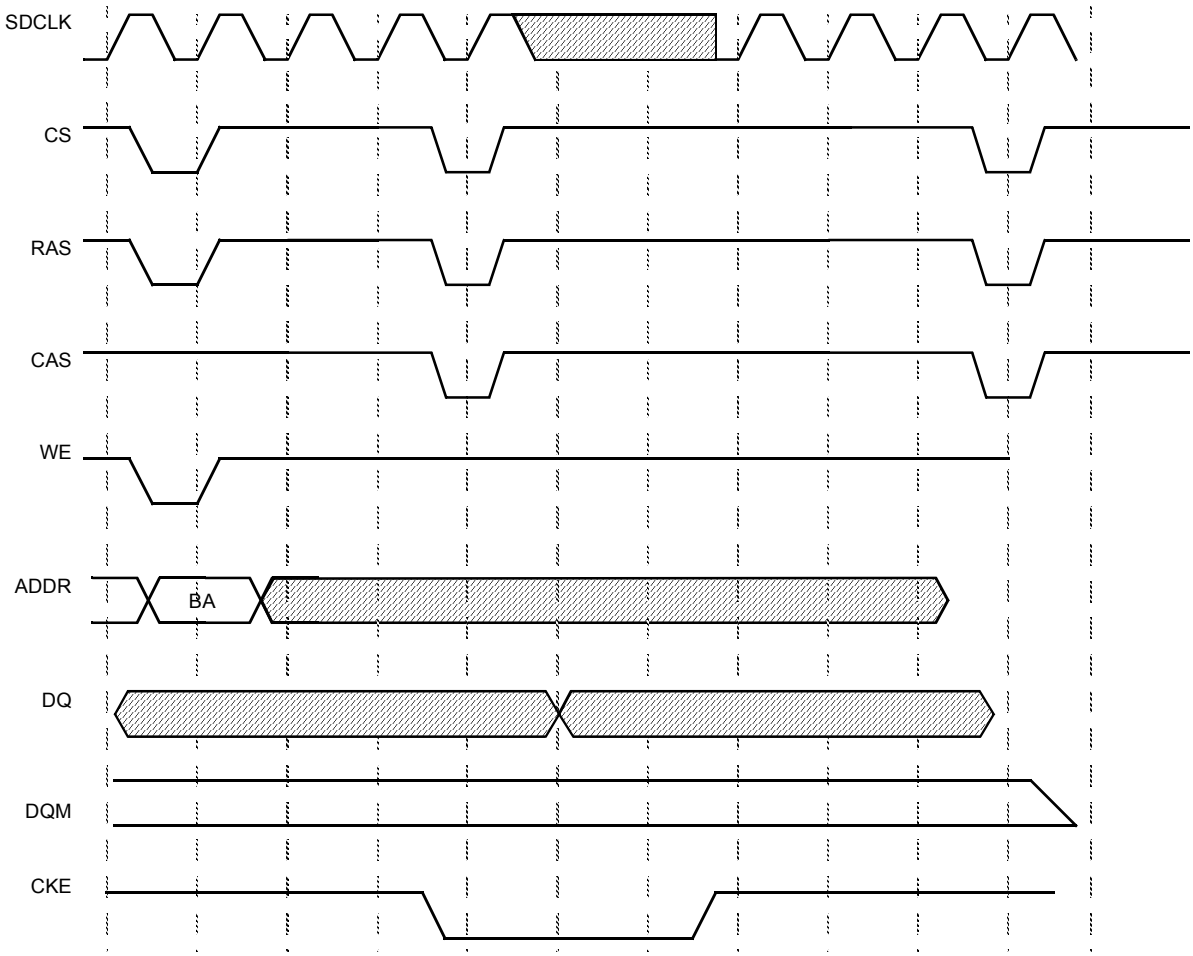

Figure 41. SDRAM Self-Refresh Cycle Timing Diagram

Table 34. SSI to SAP Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Synchronous Internal Clock Operation (SAP Ports)						
31	SRXD setup before (Tx) CK falling	23.00	–	21.41	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SAP Ports)						
33	SRXD setup before (Tx) CK falling	1.20	–	0.88	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 35. SSI to SSI1 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI1 Ports)						
1	(Tx/Rx) CK clock period[1] 9	0.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-0.68	-0.15	-0.68	-0.15	ns
3	(Rx) CK high to FS (bl) high	-0.96	-0.27	-0.96	-0.27	ns
4	(Tx) CK high to FS (bl) low	-0.68	-0.15	-0.68	-0.15	ns
5	(Rx) CK high to FS (bl) low	-0.96	-0.27	-0.96	-0.27	ns
6	(Tx) CK high to FS (wl) high	-0.68	-0.15	-0.68	-0.15	ns
7	(Rx) CK high to FS (wl) high	-0.96	-0.27	-0.96	-0.27	ns
8	(Tx) CK high to FS (wl) low	-0.68	-0.15	-0.68	-0.15	ns
9	(Rx) CK high to FS (wl) low	-0.96	-0.27	-0.96	-0.27	ns
10	(Tx) CK high to STXD valid from high impedance	-1.68	-0.36	-1.68	-0.36	ns
11a	(Tx) CK high to STXD high	-1.68	-0.36	-1.68	-0.36	ns
11b	(Tx) CK high to STXD low	-1.68	-0.36	-1.68	-0.36	ns
12	(Tx) CK high to STXD high impedance	-1.58	-0.31	-1.58	-0.31	ns
13	SRXD setup time before (Rx) CK low	20.41	–	20.41	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI1 Ports)						
15	(Tx/Rx) CK clock period[1] 9	0.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.22	17.63	8.82	16.24	ns
19	(Rx) CK high to FS (bl) high	10.79	19.67	9.39	18.28	ns

Table 37. SSI to SSI3 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	(Tx) CK high to STXD high impedance	9.02	16.46	7.29	14.97	ns
29	SRXD setup time before (Rx) CK low	1.49	–	1.49	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI3 Ports)						
31	SRXD setup before (Tx) CK falling	21.99	–	21.99	–	ns
32	SRXD old fter Txh) Kafalling C	0	–	0	–	ns
Synchronous External Clock Operation (SSI3 Ports)						
33	SRXD setup before (Tx) CK falling	3.80	–	3.80	–	ns
34	SRXD old fter Txh) Kafalling C	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

3.17 1-Wire Interface Timing

3.17.1 Reset Sequence with Reset Pulse Presence Pulse

To begin any communications with the DS2502, it is required that an initialization procedure be issued. A reset pulse must be generated and then a presence pulse must be detected. The minimum reset pulse length is 480 us. The bus master (one-wire) will generate this pulse, then after the DS2502 detects a rising edge on the one-wire bus, it will wait 15-60 us before it will transmit back a presence pulse. The presence pulse will exist for 60-240 us.

The timing diagram for this sequence is shown in Figure 46.

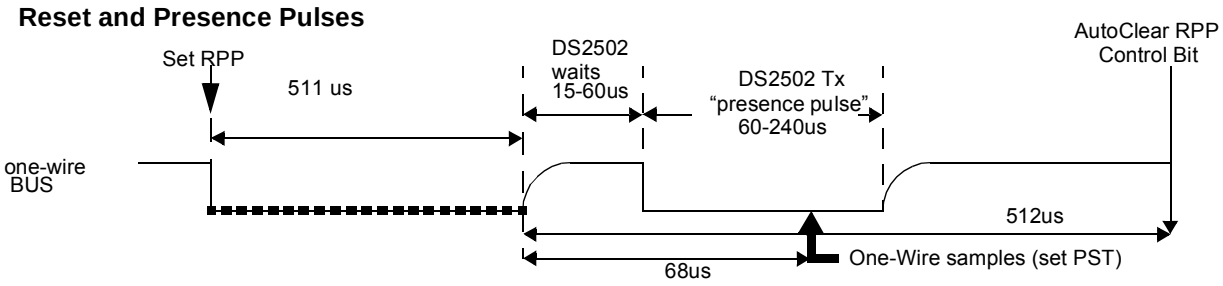

Figure 46. 1-Wire Initialization

The reset pulse begins the initialization sequence and it is initiated when the RPP control register bit is set. When the presence pulse is detected, this bit will be cleared. The presence pulse is used by the bus master to determine if at least one DS2502 is connected. Software will determine if more than one DS2502 exists. The one-wire will sample for the DS2502 presence pulse. The presence pulse is latched in the one-wire

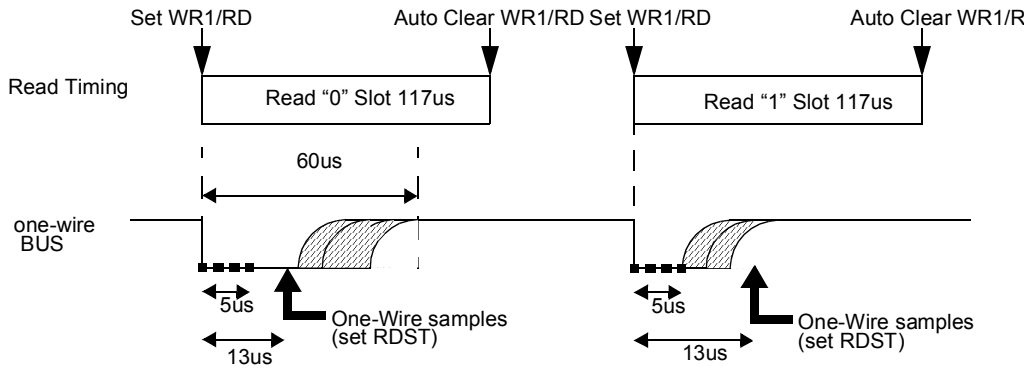

Figure 49. Read Timing

The precision of the generated clock is very important to get a proper behavior of the one-wire module. This module is based on a state machine which undertakes actions at defined times.

Table 38. System Timing Requirements

Times	Values (Microsec)	Minimum (Microsec)	Maximum (microsec)	Absolute Precision	Relative Precision
RSTL	511	480	–	31	0.0645
PST	68	60	75	7	0.1
RSTH	512	480	–	32	0.0645
LOW0	100	60	120	20	0.2
LOWR	5	1	15	4	0.8
READ_sample	13	–	15	2	0.15

The most stringent constraint is 0.0645 as a relative time imprecision.

The time relative precision is directly derived from the frequency of the derivative clock (f):

Time relative precision = 1/f -1 = divider/clock (MHz) - 1

The Figure 39 gathers relative time precision for different main clock frequencies.

Table 39. System Clock Requirements

Main Clock Frequency (MHz)	13	16.8	19.44
Clock divide ratio	13	17	19
Generated frequency (MHz)	1	0.9882	1.023
Relative time imprecision	0	0.0117	0.023

This shows that the user should take care of the main clock frequency when using the one-wire module. If the main clock is an exact integer multiple of 1 MHz, then the generated frequency will be exactly 1 MHz.

NOTE

A main clock frequency below 10 MHz might cause a misbehavior of the module.

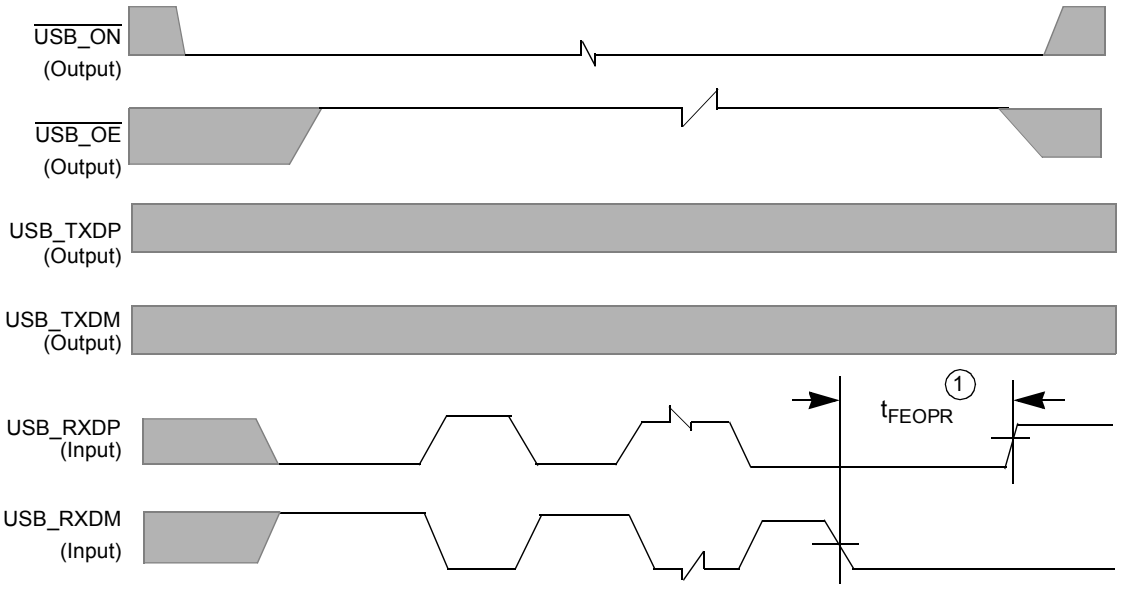

Figure 51. USB Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 41. USB Timing Parameters for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	–	ns

The USBOTG I^2C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

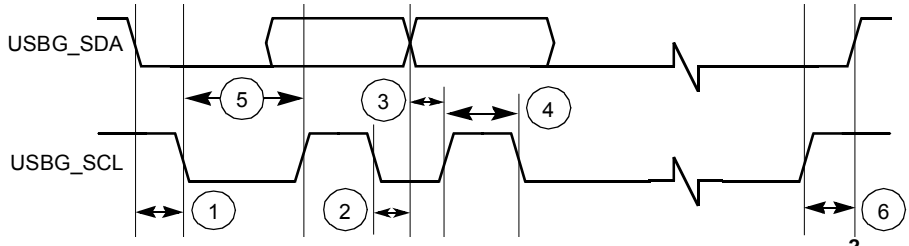

Figure 52. USB Timing Diagram for Data Transfer from USB Transceiver (I^2C)

Table 42. USB Timing Parameters for Data Transfer from USB Transceiver (I^2C)

Ref No.	Parameter	1.8 V ± 0.1 V		Unit
		Minimum	Maximum	
1	Hold time (repeated) START condition	188	–	ns
2	Data hold time	0	188	ns
3	Data setup time	88	–	ns
4	HIGH period of the SCL clock	500	–	ns
5	LOW period of the SCL clock	500	–	ns
6	Setup time for STOP condition	185	–	ns

3.19 External Interface Module (EIM)

The External Interface Module (EIM) handles the interface to devices external to the i.MX21, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 53, and Table 43 defines the parameters of signals.

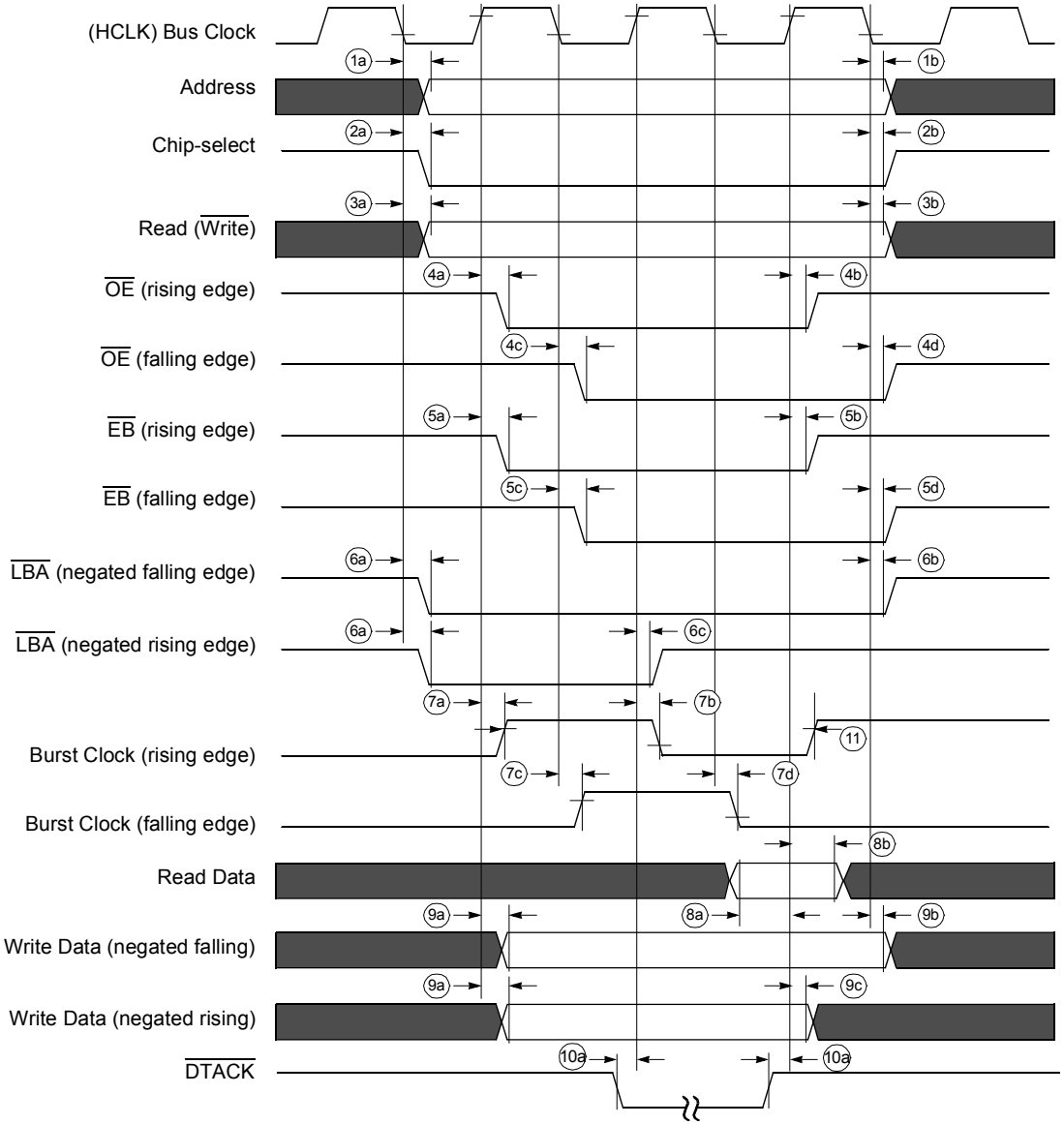

Figure 53. EIM Bus Timing Diagram

Note: Signals listed with lower case letters are internal to the device.

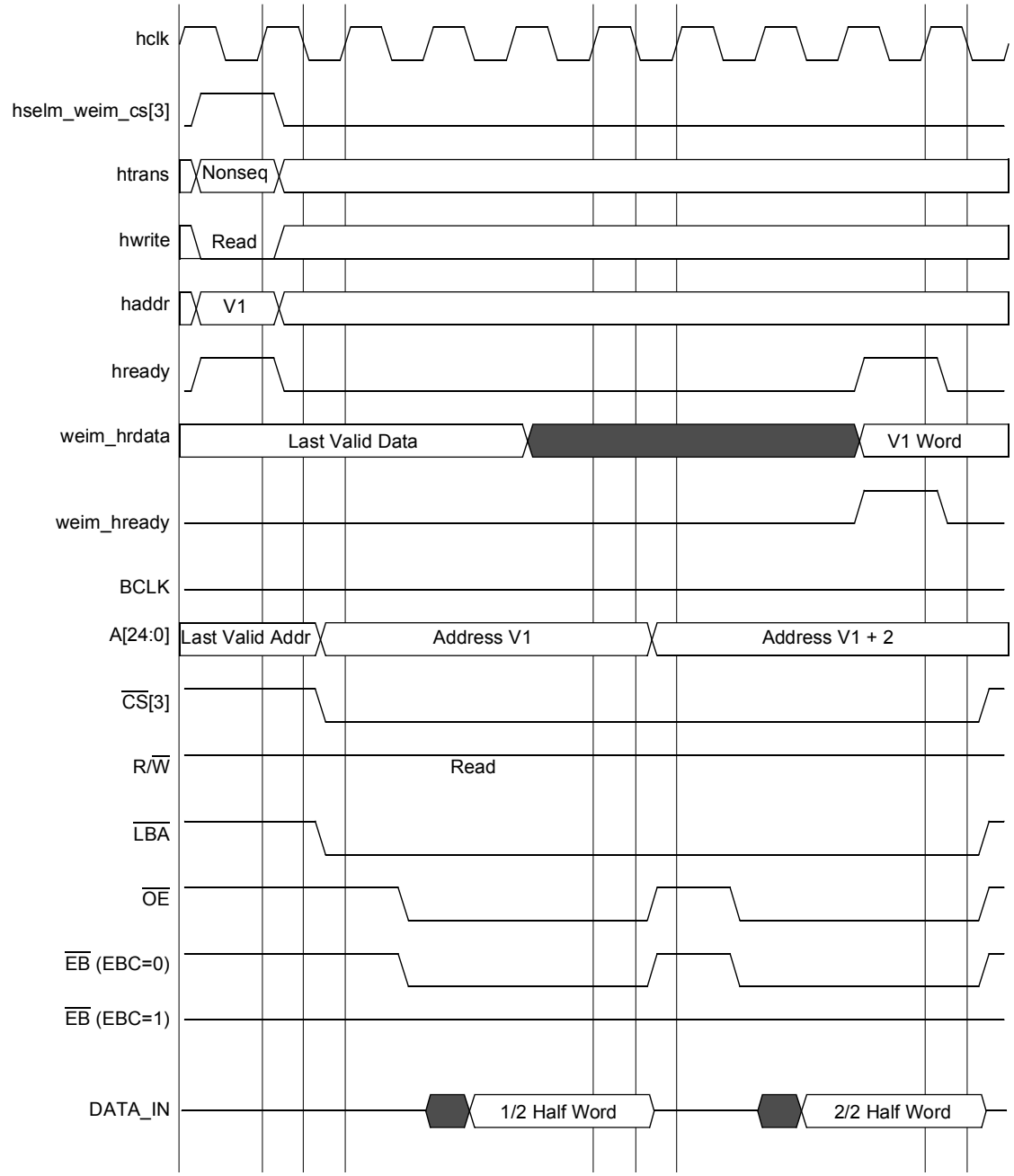

Figure 58. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

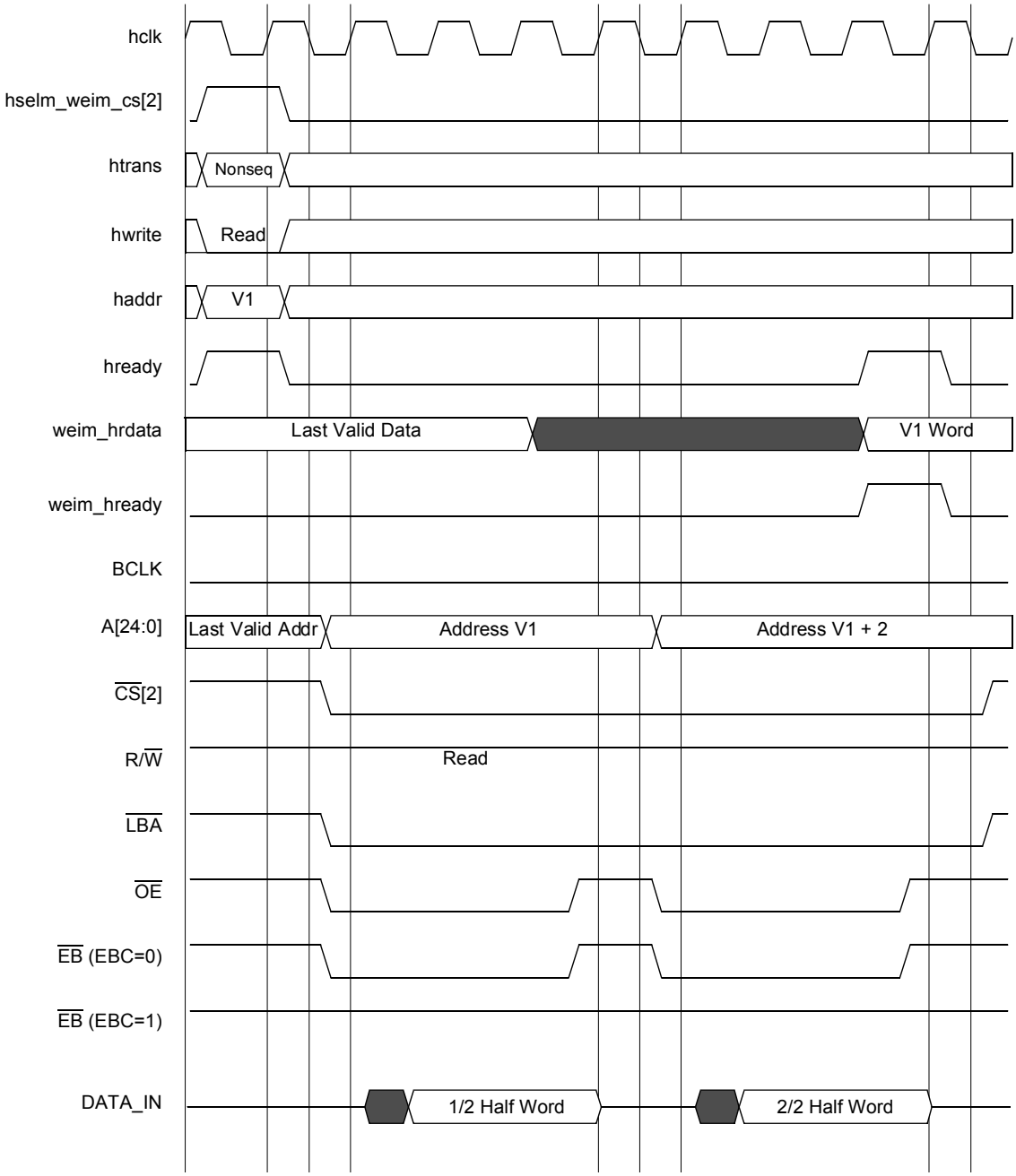

Figure 62. WSC = 3, OEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

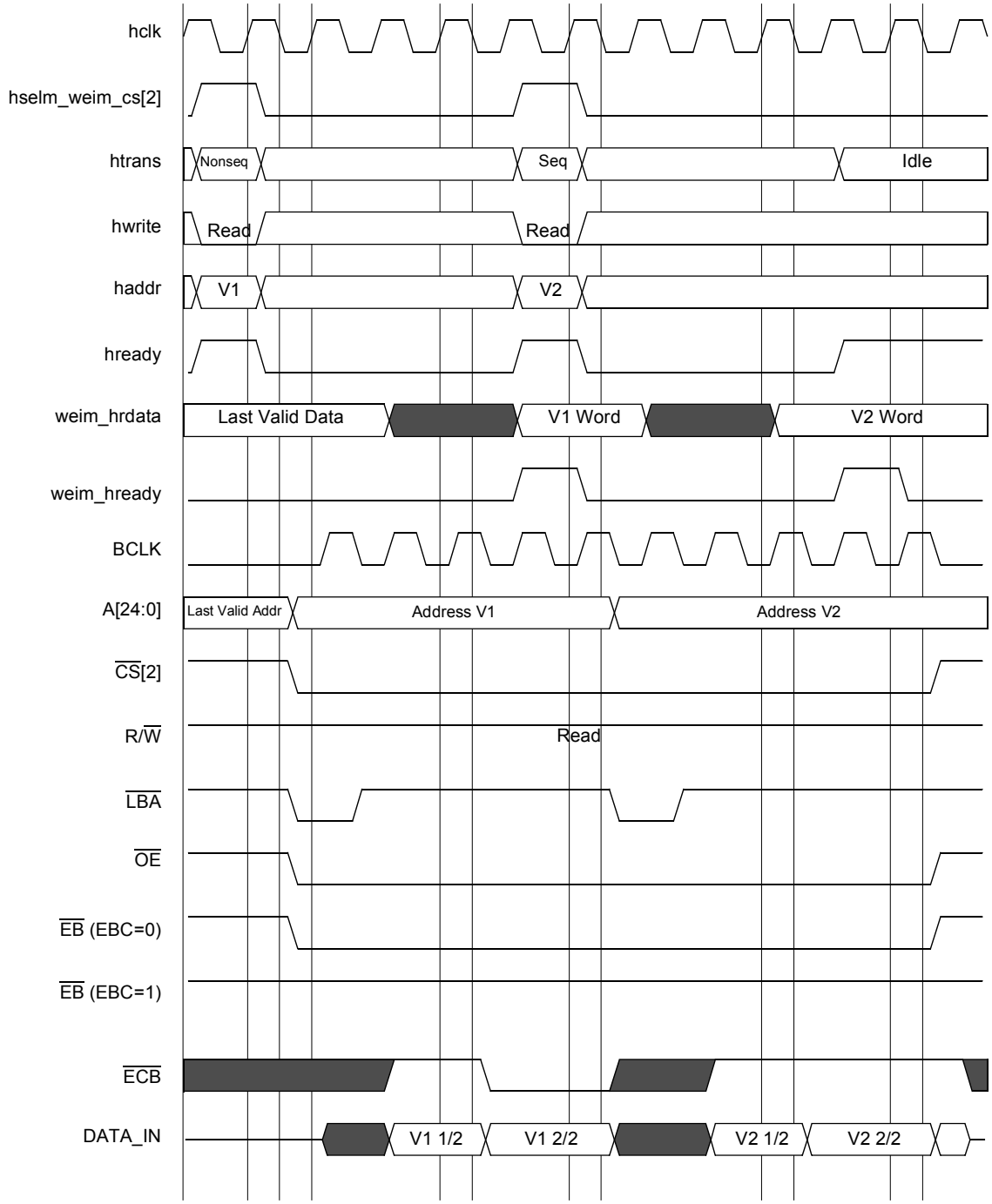

Figure 74. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

3.20.1 DTACK Example Waveforms: Internal ARM AHB Word Accesses to Word-Width (32-bit) Memory

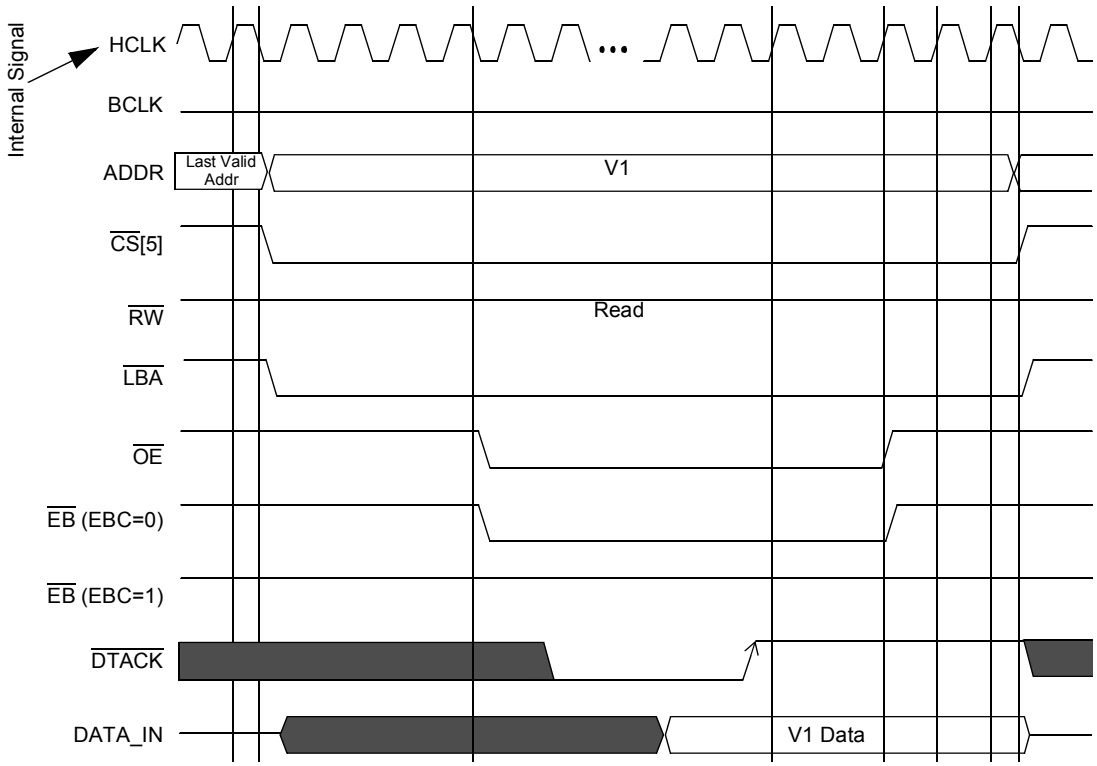

Figure 77. DTACK Edge Triggered Read Access, WSC=3F, OEA=8, OEN=5, AGE=1.

3.21 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

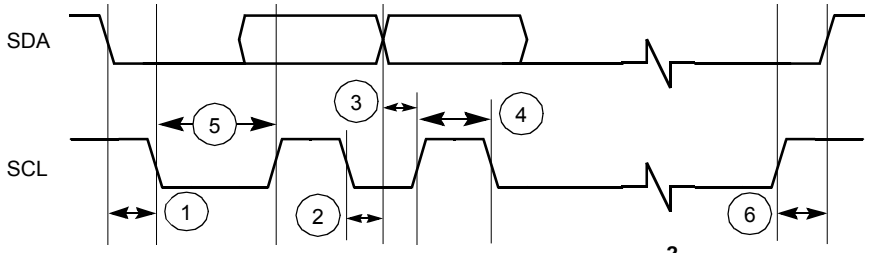

Figure 80. Definition of Bus Timing for I²C

Table 44. I²C Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
	SCL Clock Frequency	0	100	0	100	kHz
1	Hold time (repeated) START condition	114.8	–	111.1	–	ns
2	Data hold time	0	69.7	0	72.3	ns
3	Data setup time	3.1	–	1.76	–	ns
4	HIGH period of the SCL clock	69.7	–	68.3	–	ns
5	LOW period of the SCL clock	336.4	–	335.1	–	ns
6	Setup time for STOP condition	110.5	–	111.1	–	ns

3.22 CMOS Sensor Interface

The CSI module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32 × 32 image data receive FIFO, and a 16 × 32 statistic data FIFO.

3.22.1 Gated Clock Mode

Figure 81 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 82 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 45. The formula for calculating the pixel clock rise and fall time is located in Section 3.22.3, “Calculation of Pixel Clock Rise/ Fall Time.”