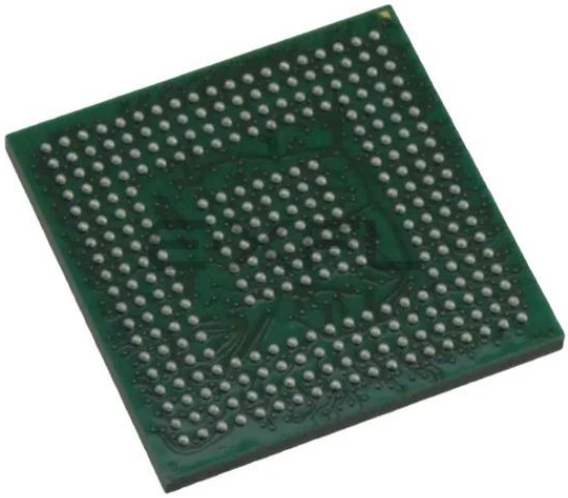

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21dvkr2

- Memory Interface
  - External Interface Module (EIM)
  - SDRAM Controller (SDRAMC)
  - NAND Flash Controller (NFC)
  - PCMCIA/CF Interface
- Standard System Resources
  - Clock Generation Module (CGM) and Power Control Module
  - Three General-Purpose 32-Bit Counters/Timers
  - Watchdog Timer
  - Real-Time Clock/Sampling Timer (RTC)
  - Pulse-Width Modulator (PWM) Module
  - Direct Memory Access Controller (DMAC)
  - General-Purpose I/O (GPIO) Ports
  - Debug Capability

2 Signal Descriptions

Table 2 identifies and describes the i.MX21 signals. Pin assignment is provided in Section 4, "Pin Assignment and Package Information" and in the "Signal Multiplexing Scheme" table within the reference manual.

The connections of the pins in Table 2 depends solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX21 processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_48M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- TEST_WB[2:0]: These signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not utilizing these signals for GPIO functionality or for their other multiplexed function, then configure as GPIO input with pull up enabled, and leave as a no connect.
- TEST_WB[4:3]: To ensure proper operation, leave these signals as no connects.

Table 2. i.MX21 Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip Select (EIM)	
A [25:0]	Address bus signals
D [31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24], shared with SDRAM DQM0.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
SLCDC2_D0	SLCD Data input signal for pass through to SLCD device. This signal is multiplexed with SSI3_FS signal from SSI3.
Bus Master Interface (BMI)	
BMI_D[15:0]	BMI bidirectional data bus. Bus width is programmable between 8-bit or 16-bit.These signals are multiplexed with LD[15:0] and SLCDC_DAT[15:0].
BMI_CLK_CS	BMI bidirectional clock or chip select signal.This signal is multiplexed with LSCLK of LCDC.
$\overline{\text{BMI\_WRITE}}$	BMI bidirectional signal to indicate read or write access. This is an input signal when the BMI is a slave and an output signal when BMI is the master of the interface. $\overline{\text{BMI\_WRITE}}$ is asserted for write and negated for read.This signal is muxed with LD[17] of LCDC.
$\overline{\text{BMI\_READ}}$	BMI output signal to enable data read from external slave device. This signal is not used and driven high when BMI is slave.This signal is multiplexed with CONTRAST signal of LCDC.
BMI_READ_REQ	BMI Read request output signal to external bus master. This signal is active when the data in the TXFIFO is larger or equal to the data transfer size of a single external BMI access.This signal is muxed with LD[16] of LCDC.
BMI_RXF_FULL	BMI Receive FIFO full active high output signal to reflect if the RxFIFO reaches water mark value.This signal is muxed with VSYNC of the LCDC.
$\overline{\text{BMI\_WAIT}}$	BMI Wait—Active low signal to wait for data ready (read cycle) or accepted (write_cycle). Also multiplexed with VSYNC.
External DMA	
$\overline{\text{EXT\_DMAREQ}}$	External DMA Request input signal. This signal is multiplexed with CSPI1_$\overline{\text{RDY}}$.
$\overline{\text{EXT\_DMAGRANT}}$	External DMA Grant output signal. This signal is multiplexed with LD[16] of LCDC and CSPI1_SS1 of CSPI1.
NAND Flash Controller	
NF_CLE	NAND Flash Command Latch Enable output signal. Multiplexed with PC_POE of PCMCIA.
$\overline{\text{NF\_CE}}$	NAND Flash Chip Enable output signal. This signal is multiplexed with PC_CE1 of PCMCIA.
$\overline{\text{NF\_WP}}$	NAND Flash Write Protect output signal. This signal is multiplexed with PC_CE2 of PCMCIA.
NF_ALE	NAND Flash Address Latch Enable output signal. This signal is multiplexed with $\overline{\text{PC\_OE}}$ of PCMCIA.
$\overline{\text{NF\_RE}}$	NAND Flash Read Enable output signal. This signal is multiplexed with $\overline{\text{PC\_RW}}$ of PCMCIA.
$\overline{\text{NF\_WE}}$	NAND Flash Write Enable output signal. This signal is multiplexed with and PC_BVD2 of PCMCIA.
NF_RB	NAND Flash Ready Busy input signal. This signal is multiplexed with PC_RST of PCMCIA.
NF_IO[15:0]	NAND Flash Data input and output signals. NF_IO[15:7] signals are multiplexed with A[25:21] and A[15:13]. NF_IO[7:0] signals are multiplexed with several PCMCIA signals.
PCMCIA Controller	
PC_A[25:0]	PCMCIA Address signals. These signals are multiplexed with A[25:0].
PC_D[15:0]	PCMCIA Data input and output signals. These signals are multiplexed with D[15:0].
$\overline{\text{PC\_CD1}}$	PCMCIA Card Detect1 input signal. This signal is multiplexed with NFIO[7] signal of NF.
$\overline{\text{PC\_CD2}}$	PCMCIA Card Detect2 input signal. This signal is multiplexed with NFIO[6] signal of NF.
$\overline{\text{PC\_WAIT}}$	PCMCIA Wait input signal to extend current access. This signal is multiplexed with NFIO[5] signal of NF.
PC_READY	PCMCIA Ready input signal indicates card is ready for access. Multiplexed with NFIO[4] signal of NF.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH2_FS	USB Host2 Full Speed output signal. This signal is multiplexed with CSPI2_SS[0] of CSPI2.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added. This signal is multiplexed with CSPI3_MOSI.
SD1_CLK	SD Output Clock. This signal is multiplexed with CSPI3_SCLK.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART2_RXD	Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP.
UART2_TXD	Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP.
$\overline{\text{UART2\_RTS}}$	Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP.
$\overline{\text{UART2\_CTS}}$	Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP.
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.
KP_ROW[7:0]	Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2\_RTS}}$ and $\overline{\text{UART2\_RXD}}$ signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available.
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6.
NVSS	Noisy Ground for the I/O pins

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK, VM	T_A	0	70	°C
	DVK, DVM	T_A	-30	70	°C
	CVK, CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V

Table 11. DPLL Specifications (Continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Frequency lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	350	400	450	T_{ref}
Frequency lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	280	330	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	480	530	580	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	360	410	460	T_{ref}
Frequency jitter (p-p)	–	–	0.02	0.03	$2 \cdot T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.7V	–	1.0	1.5	ns
Power dissipation	FOL mode, integer MF, f_{dck} = 560 MHz, Vcc = 1.5V	–	1.5	–	mW (Avg)

3.6 Reset Module

The timing relationships of the Reset module with the $\overline{\text{POR}}$ and $\overline{\text{RESET\_IN}}$ are shown in Figure 2 and Figure 3. Be aware that NVDD must ramp up to at least 1.7V for NVDD1 and 2.7V for NVDD2-6 before QVDD is powered up to prevent forward biasing.

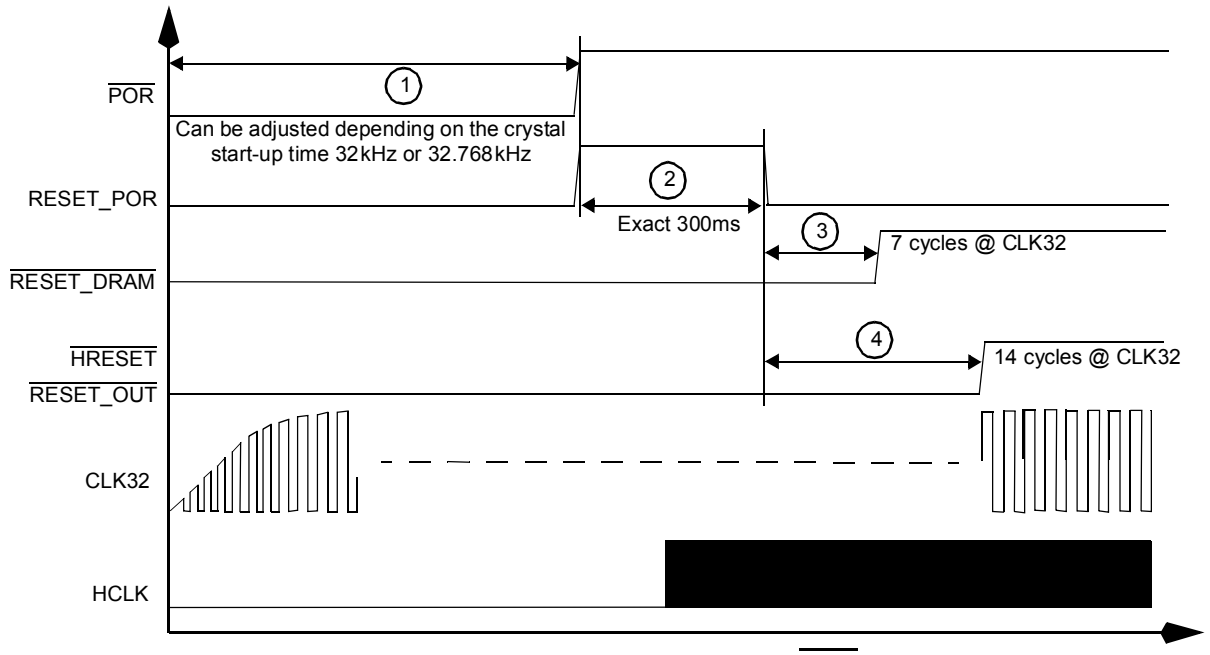

Figure 2. Timing Relationship with $\overline{\text{POR}}$

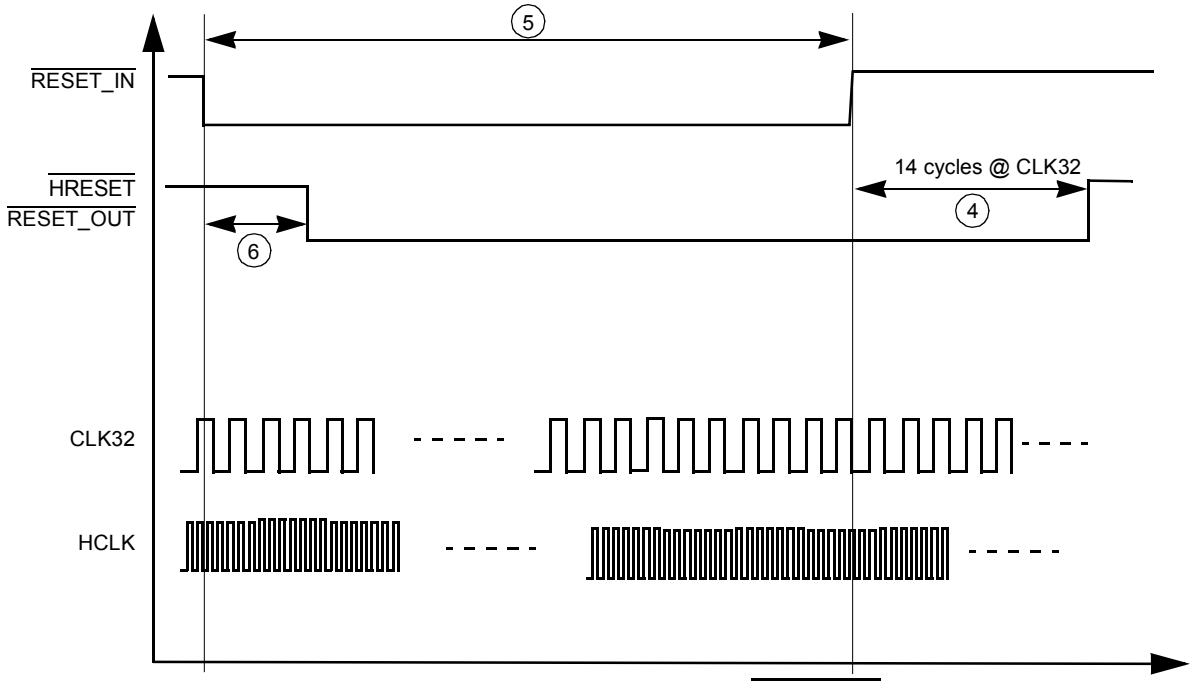

Figure 3. Timing Relationship with $\overline{\text{RESET\_IN}}$

Table 12. Reset Module Timing Parameters

Ref No.	Parameter	1.8 V ± 0.10 V		3.0 V ± 0.30 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	800	–	800	–	ms
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7k to 32k-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14k to 32k-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4k to 32k-cycle qualifier	4	4	4	4	Cycles of CLK32

3.7 External DMA Request and Grant

The External DMA request is an active low signal to be used by devices external to i.MX21 processor to request the DMAC for data transfer.

After assertion of External DMA request the DMA burst will start when the channel on which the External request is the source (as per the RSSR settings) becomes the current highest priority channel. The external device using the External DMA request should keep its request asserted until it is serviced by the DMAC. One External DMA request will initiate one DMA burst.

Table 13. DMA External Request and Grant Timing Parameters

Parameter	Description	3.0 V		1.8 V		Unit
		WCS	BCS	WCS	BCS	
t_{min_assert}	Minimum assertion time of External Grant signal	8 hclk + 8.6	8 hclk + 2.74	8 hclk + 7.17	8 hclk + 3.25	ns
$t_{max\_req\_assert}$	Maximum External request assertion time after assertion of Grant signal	9 hclk - 20.66	9 hclk - 6.7	9 hclk - 17.96	9 hclk - 8.16	ns
t_{max_read}	Maximum External request assertion time after first read completion	8 hclk - 6.21	8 hclk - 0.77	8 hclk - 5.84	8 hclk - 0.66	ns
t_{max_write}	Maximum External request assertion time after completion of first write	3 hclk - 15.87	3 hclk - 8.83	3 hclk - 15.9	3 hclk - 9.12	ns

3.8 BMI Interface Timing Diagram

3.8.1 Connecting BMI to ATI MMD Devices

3.8.1.1 ATI MMD Devices Drive the BMI_CLK/CS

In this mode MMD_MODE_SEL bit is set and MMD_CLKOUT bit is cleared. $\overline{\text{BMI\_WRITE}}$ and BMI_CLK/CS are input signals to BMI driving by ATI MMD chip set. Output signal BMI_READ_REQ can be used as interrupt signal to inform MMD that data is ready in BMI TxFIFO for read access. MMD can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

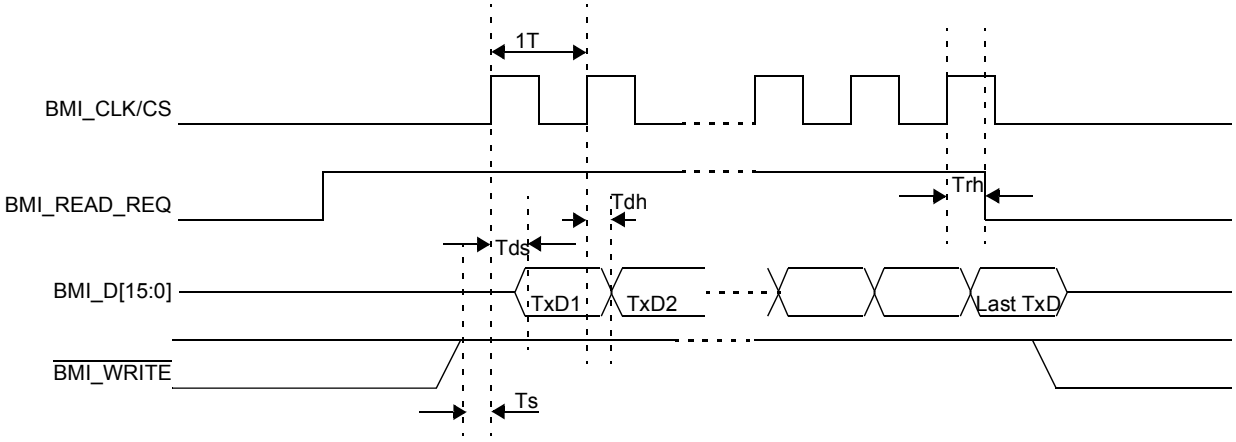

Figure 6. MMD (ATI) Drives Clock, MMD Read BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0,MMD_CLKOUT=0)

Table 14. MMD Read BMI Timing Table when MMD Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Clock period	1T	33.3	–	–	ns
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
read_req hold time	Trh	6	–	24	ns
transfer data setup time	Tds	6	–	14	ns
transfer data hold time	Tdh	6	-	14	ns

Note: All the timings assume that the hclk is running at 133 MHz.

Note: The MIN period of the 1T is assumed that MMD latch data at falling edge.

Note: If the MMD latch data at next rising edge, the ideally max clock can be as much as double, but because the BMI data pads are slow pads and it max frequency can only up to 18MHz, the max clock frequency can only up to 36 MHz.

3.8.1.1.2 MMD Write BMI Timing

Figure 7 shows the MMD write BMI timing when MMD drives clock. On each falling edge of BMI_CLK/$\overline{\text{CS}}$ BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a write cycle. If the $\overline{\text{BMI\_WRITE}}$ is logic low, it latches data into the RxFIFO on each falling edge of BMI_CLK/CS signal.

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

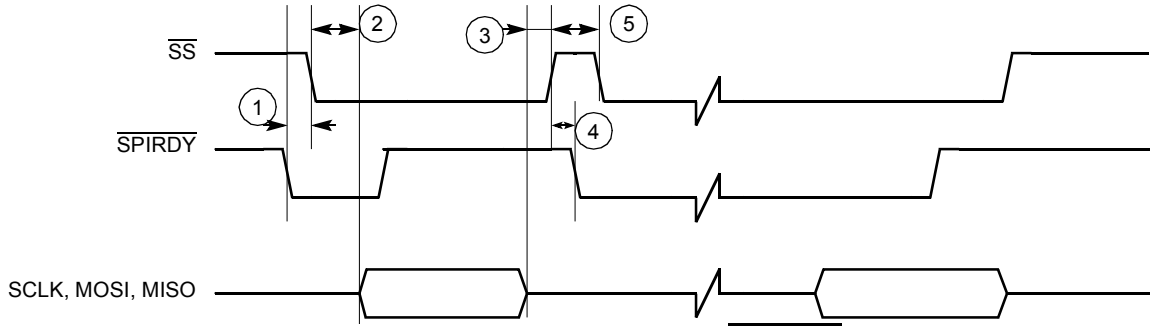

Figure 14. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger

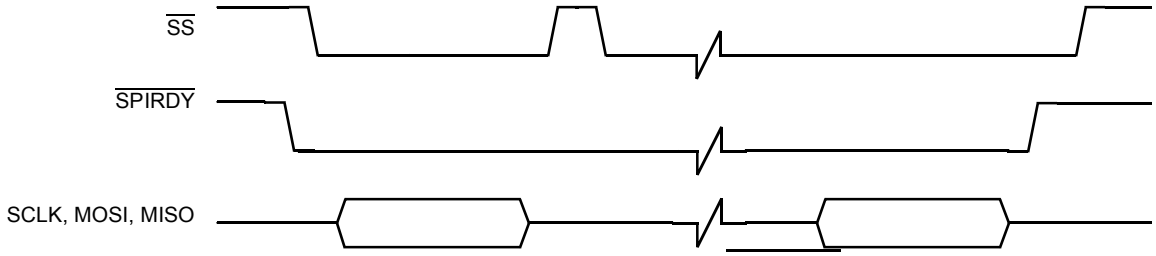

Figure 15. Master CSPI Timing Diagram Using SPI_RDY Level Trigger

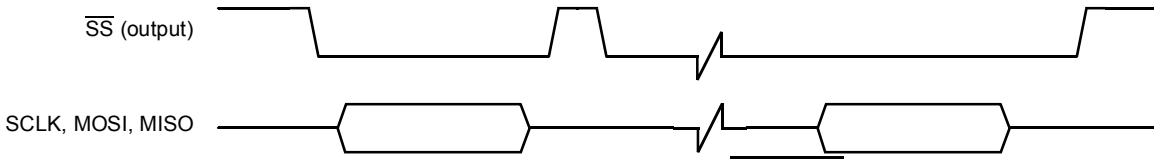

Figure 16. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger

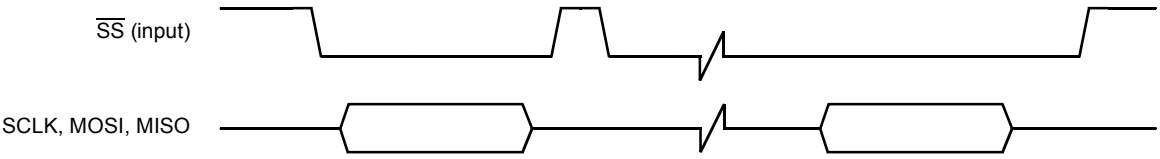

Figure 17. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT

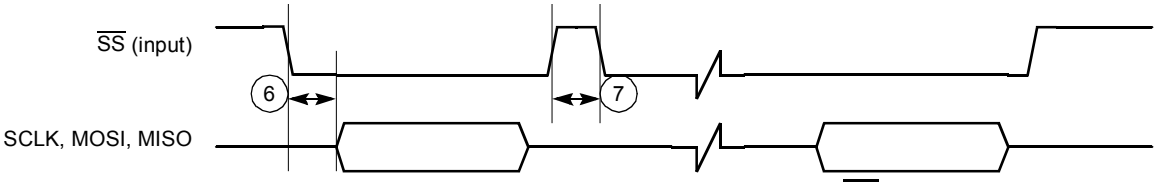

Figure 18. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge

Table 19. Timing Parameters for Figure 14 through Figure 18

Ref No.	Parameter	Minimum	Maximum	Unit
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T [1]	–	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3·Tsclk [2]	–	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2·Tsclk	–	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	–	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	–	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	–	ns
7	$\overline{\text{SS}}$ input pulse width	T	–	ns

1. T = CSPI system clock period (PERCLK2).
2. Tsclk = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

3.10 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *i.MX21 Reference Manual*.

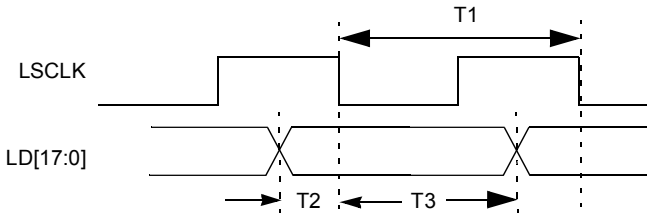

Figure 19. SCLK to LD Timing Diagram

Table 20. LCDC SCLK Timing Parameters

Symbol	Parameter	3.0 ± 0.3V		Unit
		Minimum	Maximum	
T1	SCLK period	23	2000	ns
T2	Pixel data setup time	11	–	ns
T3	Pixel data up time	11	–	ns
The pixel clock is equal to LCDC_CLK / (PCD + 1). When it is in CSTN, TFT or monochrome mode with bus width = 1, SCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, SCLK is equal to the pixel clock divided by bus width. The polarity of SCLK and LD can also be programmed. Maximum frequency of SCLK is HCLK / 3 for TFT and CSTN, otherwise LD output will be incorrect.				

Table 29. NFC Target Timing Parameters[1],[2]

ID	Parameter	Symbol	Relationship to NFC Clock Period (T)		NFC Clock 22.17 MHz T = 45 ns		NFC Clock 33.25 MHz T = 30 ns		Unit
			Min	Max	Min	Max	Min	Max	
NF1	NFCLE Setup Time	tCLS	T	–	45	–	30	–	ns
NF2	NFCLE Hold Time	tCLH	T	–	45	–	30	–	ns
NF3	$\overline{\text{NFCE}}$ Setup Time	tCS	T	–	45	–	30	–	ns
NF4	$\overline{\text{NFCE}}$ Hold Time	tCH	T	–	45	–	30	–	ns
NF5	$\overline{\text{NF\_WP}}$ Pulse Width	tWP	T	–	45	–	30	–	ns
NF6	NFALE Setup Time	tALS	T	–	45	–	30	–	ns
NF7	NFALE Hold Time	tALH	T	–	45	–	30	–	ns
NF8	Data Setup Time	tDS	T	–	45	–	30	–	ns
NF9	Data Hold Time	tDH	T	–	45	–	30	–	ns
NF10	Write Cycle Time	tWC	2T	–	90	–	60	–	ns
NF11	$\overline{\text{NFWE}}$ Hold Time	tWH	T	–	45	–	30	–	ns
NF12	Ready to $\overline{\text{NFRE}}$ Low	tRR	4T	–	180	–	120	–	ns
NF13	$\overline{\text{NFRE}}$ Pulse Width	tRP	1.5T	–	67.5	–	45	–	ns
NF14	READ Cycle Time	tRC	2T	–	90	–	60	–	ns
NF15	$\overline{\text{NFRE}}$ High Hold Time	tREH	0.5T	–	22.5	–	15	–	ns
NF16	Data Setup on READ	tDSR	15	–	15	–	15	–	ns
NF17	Data Hold on READ	tDHR	0	–	0	–	0	–	ns

1. High is defined as 80% of signal value and low is defined as 20% of signal value. All timings are listed according to this NFC clock frequency (multiples of NFC clock period) except NF16, which is not NFC clock related.
2. The read data is generated by the NAND Flash device and sampled with the internal NFC clock.

Table 31. SDRAM Read Cycle Timing Parameter (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
4S	Address setup time	3.67	–	2	–	ns
4H	Address hold time	2.95	–	2	–	ns
5	SDRAM access time (CL = 3)	–	5.4	–	5.4	ns
5	SDRAM access time (CL = 2)	–	6.0	–	6.0	ns
5	SDRAM access time (CL = 1)	–	–	–	–	ns
6	Data out hold time	2	–	2	–	ns
7	Data out high-impedance time (CL = 3)	–	t_{HZ}[1]	–	t_{HZ}[1]	ns
7	Data out high-impedance time (CL = 2)	–	t_{HZ}[1]	–	t_{HZ}[1]	ns
7	Data out high-impedance time (CL = 1)	–	–	–	–	ns
8	Active to read/write command period (RC = 1)	t_{RCD}[2]	–	t_{RCD}[2]	–	ns

1. t_{HZ} = SDRAM data out high-impedance time, external SDRAM memory device dependent parameter.
2. t_{RCD} = SDRAM clock cycle time. The t_{RCD} setting can be found in the i.MX21 reference manual.

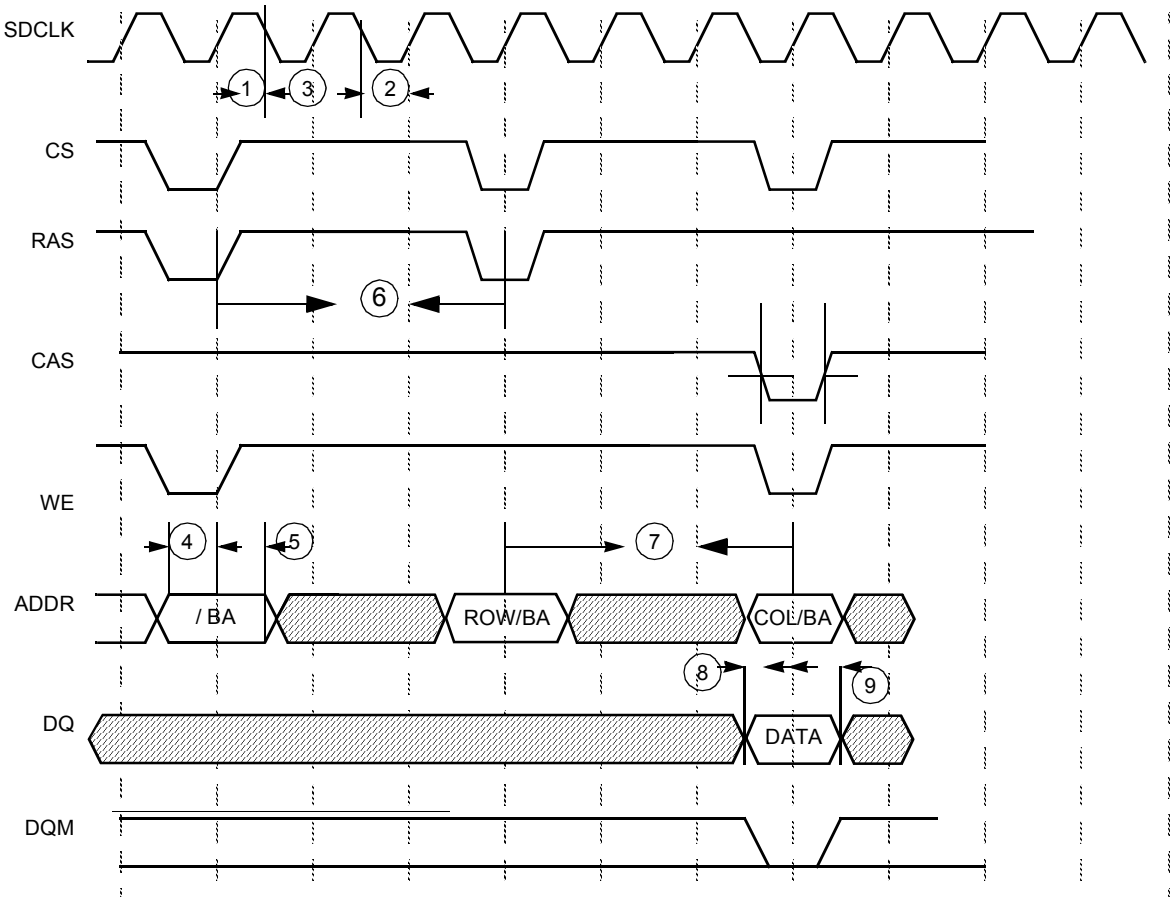

Figure 39. SDRAM Write Cycle Timing Diagram

Table 35. SSI to SSI1 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
20	(Tx) CK high to FS (bl) low	10.22	17.63	8.82	16.24	ns
21	(Rx) CK high to FS (bl) low	10.79	19.67	9.39	18.28	ns
22	(Tx) CK high to FS (wl) high	10.22	17.63	8.82	16.24	ns
23	(Rx) CK high to FS (wl) high	10.79	19.67	9.39	18.28	ns
24	(Tx) CK high to FS (wl) low	10.22	17.63	8.82	16.24	ns
25	(Rx) CK high to FS (wl) low	10.79	19.67	9.39	18.28	ns
26	(Tx) CK high to STXD valid from high impedance	10.05	15.75	8.66	14.36	ns
27a	(Tx) CK high to STXD high	10.00	15.63	8.61	14.24	ns
27b	(Tx) CK high to STXD low	10.00	15.63	8.61	14.24	ns
28	(Tx) CK high to STXD high impedance	10.05	15.75	8.66	14.36	ns
29	SRXD setup time before (Rx) CK low	0.78	–	0.47	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI1 Ports)						
31	SRXD setup before (Tx) CK falling	19.90	–	19.90	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI1 Ports)						
33	SRXD setup before (Tx) CK falling	2.59	–	2.28	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 36. SSI to SSI2 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI2 Ports)						
1	(Tx/Rx) CK clock period[1] 90	.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	0.01	0.15	0.01	0.15	ns
3	(Rx) CK high to FS (bl) high	-0.21	0.05	-0.21	0.05	ns
4	(Tx) CK high to FS (bl) low	0.01	0.15	0.01	0.15	ns
5	(Rx) CK high to FS (bl) low	-0.21	0.05	-0.21	0.05	ns
6	(Tx) CK high to FS (wl) high	0.01	0.15	0.01	0.15	ns
7	(Rx) CK high to FS (wl) high	-0.21	0.05	-0.21	0.05	ns
8	(Tx) CK high to FS (wl) low	0.01	0.15	0.01	0.15	ns
9	(Rx) CK high to FS (wl) low	-0.21	0.05	-0.21	0.05	ns
10	(Tx) CK high to STXD valid from high impedance	0.34	0.72	0.34	0.72	ns

Table 36. SSI to SSI2 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
11a	(Tx) CK high to STXD high	0.34	0.72	0.34	0.72	ns
11b	(Tx) CK high to STXD low	0.34	0.72	0.34	0.72	ns
12	(Tx) CK high to STXD high impedance	0.34	0.48	0.34	0.48	ns
13	SRXD setup time before (Rx) CK low	21.50	–	21.50	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI2 Ports)						
15	(Tx/Rx) CK clock period[1] 90	.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.40	17.37	8.67	15.88	ns
19	(Rx) CK high to FS (bl) high	11.00	19.70	9.28	18.21	ns
20	(Tx) CK high to FS (bl) low	10.40	17.37	8.67	15.88	ns
21	(Rx) CK high to FS (bl) low	11.00	19.70	9.28	18.21	ns
22	(Tx) CK high to FS (wl) high	10.40	17.37	8.67	15.88	ns
23	(Rx) CK high to FS (wl) high	11.00	19.70	9.28	18.21	ns
24	(Tx) CK high to FS (wl) low	10.40	17.37	8.67	15.88	ns
25	(Rx) CK high to FS (wl) low	11.00	19.70	9.28	18.21	ns
26	(Tx) CK high to STXD valid from high impedance	9.59	17.08	7.86	15.59	ns
27a	(Tx) CK high to STXD high	9.59	17.08	7.86	15.59	ns
27b	(Tx) CK high to STXD low	9.59	17.08	7.86	15.59	ns
28	(Tx) CK high to STXD high impedance	9.59	16.84	7.86	15.35	ns
29	SRXD setup time before (Rx) CK low	2.52	–	2.52	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI2 Ports)						
31	SRXD setup before (Tx) CK falling	20.78	–	20.78	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI2 Ports)						
33	SRXD setup before (Tx) CK falling	4.42	–	4.42	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 43. EIM Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V			1.8 V ± 0.1 V	Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	3.97	6.02	9.89	3.83	5.89	9.79	ns
1b	Clock fall to address invalid	3.93	6.00	9.86	3.81	5.86	9.76	ns
2a	Clock fall to chip-select valid	3.47	5.59	8.62	3.30	5.09	8.45	ns
2b	Clock fall to chip-select invalid	3.39	5.09	8.27	3.15	4.85	8.03	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	3.51	5.56	8.79	3.39	5.39	8.51	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	3.59	5.37	9.14	3.36	5.20	8.50	ns
4a	Clock[1] rise to Output Enable Valid	3.62	5.49	8.98	3.46	5.33	9.02	ns
4b	Clock[1] rise to Output Enable Invalid	3.70	5.61	9.26	3.46	5.37	8.81	ns
4c	Clock[1] fall to Output Enable Valid	3.60	5.48	8.77	3.44	5.30	8.88	ns
4d	Clock[1] fall to Output Enable Invalid	3.69	5.62	9.12	3.42	5.36	8.60	ns
5a	Clock[1] rise to Enable Bytes Valid	3.69	5.46	8.71	3.46	5.25	8.54	ns
5b	Clock[1] rise to Enable Bytes Invalid	4.64	5.47	8.70	3.46	5.25	8.54	ns
5c	Clock[1] fall to Enable Bytes Valid	3.52	5.06	8.39	3.41	5.18	8.36	ns
5d	Clock[1] fall to Enable Bytes Invalid	3.50	5.05	8.27	3.41	5.18	8.36	ns
6a	Clock[1] fall to Load Burst Address Valid	3.65	5.28	8.69	3.30	5.23	8.81	ns
6b	Clock[1] fall to Load Burst Address Invalid	3.65	5.67	9.36	3.41	5.43	9.13	ns
6c	Clock[1] rise to Load Burst Address Invalid	3.66	5.69	9.48	3.33	5.47	9.25	ns
7a	Clock[1] rise to Burst Clock rise	3.50	5.22	8.42	3.26	4.99	8.19	ns
7b	Clock[1]rise to Burst Clock fall	3.49	5.19	8.30	3.31	5.03	8.17	ns
7c	Clock[1] fall to Burst Clock rise	3.50	5.22	8.39	3.26	4.98	8.15	ns
7d	Clock[1] fall to Burst Clock fall	3.49	5.19	8.29	3.31	5.02	8.12	ns
8a	Read Data setup time	4.54	–	–	4.54	–	–	ns
8b	Read Data hold time	0.5	–	–	0.5	–	–	ns
9a	Clock[1] rise to Write Data Valid	4.13	5.86	9.16	3.95	6.36	10.31	ns
9b	Clock[1] fall to Write Data Invalid	4.10	5.79	9.15	4.04	6.27	9.16	ns
9c	Clock[1] rise to Write Data Invalid	4.02	5.81	9.37	4.22	5.29	9.24	ns
10a	DTACK setup time	2.65	4.63	8.40	2.64	4.61	8.41	ns
11	Burst Clock (BCLK) cycle time	15	–	–	15	–	–	ns

1. Clock refers to the system clock signal, HCLK, generated from the System DPLL

3.20 DTACK Mode Memory Access Timing Diagrams

When enabled, the DTACK input signal is used to externally terminate a data transfer. For DTACK enabled operations, a bus time-out monitor generates a bus error when an external bus cycle is not terminated by the DTACK input signal after 1024 HCLK clock cycles have elapsed, where HCLK is the internal system clock driven from the PLL module. For a 133 MHz HCLK setting, this time equates to 7.7 µs. Refer to the Section 3.5, "DPLL Timing Specifications" for more information on how to generate different HCLK frequencies.

There are two modes of operation for the DTACK input signal: rising edge detection or level sensitive detection with a programmable insensitivity time. DTACK is only used during external asynchronous data transfers, thus the SYNC bit in the chip select control registers must be cleared.

During edge detection mode, the EIM will terminate an external data transfer following the detection of the DTACK signal's rising edge, so long as it occurs within the 1024 HCLK cycle time. Edge detection mode is used for devices that follow the PCMCIA standard. Note that DTACK rising edge detection mode can only be used for $\overline{CS}$[5] operations. To configure $\overline{CS}$[5] for DTACK rising edge detection, the following bits must be programmed in the Chip Select 5 Control Register and EIM Configuration Register:

- WSC bit field set to 0x3F and CSA (or CSN) set to 1 or greater in the Chip Select 5 Control Register
- AGE bit set in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device. The requirement of setting CSA or CSN is required to allow the EIM to wait for the rising edge of DTACK during back-to-back external transfers, such as during DMA transfers or an internal 32-bit access through an external 16-bit data port.

During level sensitive detection, the EIM will first hold off sampling the DTACK signal for at least 2 HCLK cycles, and up to 5 HCLK cycles as programmed by the DCT bits in the Chip Select Control Register. After this insensitivity time, the EIM will sample DTACK and if it detects that DTACK is logic high, it will continue the data transfer at the programmed number of wait states. However, if the EIM detects that DTACK is logic low, it will wait until DTACK goes to logic high to continue the access, so long as this occurs within the 1024 HCLK cycle time. If at anytime during an external data transfer DTACK goes to logic low, the EIM will wait until DTACK returns to logic high to resume the data transfer. Level detection is often used for asynchronous devices such graphic controller chips. Level detection may be used with any chip select except CS[4] as it is multiplexed with the DTACK signal. To configure a chip select for DTACK level sensitive detection, the following bits must be programmed in the Chip Select Control Register and EIM Configuration Register:

- EW bit set, WSC set to > 1, and CSN set to < 3 in the Chip Select Control Register
- BCD/DCT set to desired "insensitivity time" in the Chip Select Control Register. The "insensitivity time" is dictated by the external device's timing requirements.
- AGE bit cleared in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device.

The waveforms in the following section provide examples of the DTACK signal operation.

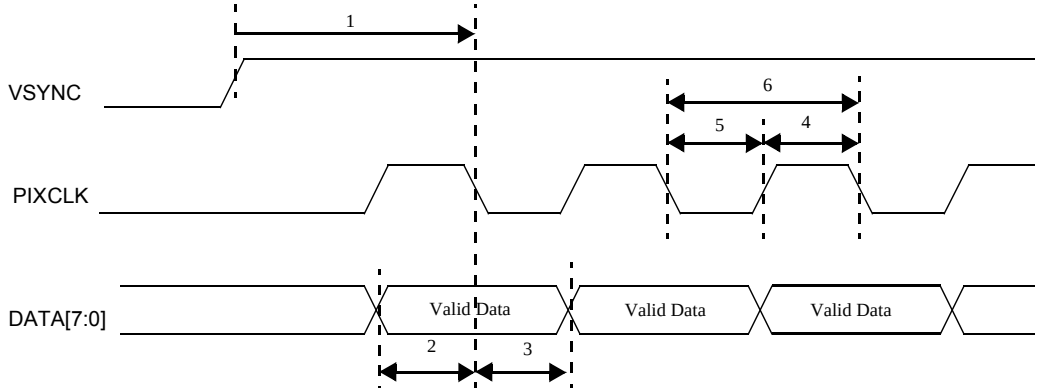

Figure 84. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 46. Non-Gated Clock Mode Parameters[1]

Number	Parameter	Minimum	Maximum	Unit
1	csi_vsync to csi_pixclk	9 * T_{HCLK}	–	ns
2	csi_d setup time	1	–	ns
3	csi_d hold time	1	–	ns
4	csi_pixclk high time	T_{HCLK}	–	ns
5	csi_pixclk low time	T_{HCLK}	–	ns
6	csi_pixclk frequency	0	HCLK / 2	MHz

1. HCLK = AHB System Clock, T_{HCLK} = Period of HCLK

3.22.3 Calculation of Pixel Clock Rise/Fall Time

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data

- max rise time allowed = (positive duty cycle - hold time)
- max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

- max rise time = (period / 2 - hold time)
- max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
≥ max rise time allowed = 5 - 1 = 4ns
negative duty cycle = 10 / 2 = 5ns
≥ max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

- max fall time allowed = (negative duty cycle - hold time)
- max rise time allowed = (positive duty cycle - setup time)

4 Pin Assignment and Package Information

Table 47. i.MX21 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	LD9	LD12	LD14	REV	HSYNC	OE_ ACD	SD2_D2	CSI_ D0	CSI_ PIXCLK	CSI_ VSYNC	USBH1_ FS	USBH1_ OE	USBG_ FS	TOUT	SAP_ TXDAT	SSI1_ CLK	SSI2_ RXDAT	SSI2_TXDAT	SSI3_ FS
B	LD7	LD5	LD11	LD16	PS	CON TRAST	SD2_D0	SD2_ CMD	CSI_ D4	CSI_D6	USB_ PWR	USBG_ SCL	USBG_ TXDM	SAP_ FS	SSI1_ FS	SSI2_ FS	SSI3_ TXDAT	I2C_DATA	CSPI2_ SS2
C	LD1	LD3	LD6	LD10	LD17	VSYNC	SD2_D3	CSI_ D1	CSI_ MCLK	CSI_ HSYNC	USB_ OC	USBH1_ RXDM	USBG_ RXDM	TIN	SSI1_ TXDAT	SSI3_ RXDAT	SSI3_ CLK	I2C_CLK	CSPI2_ SS1
D	LD2	LD0	LD13	CLS	QVDD	QVSS	SD2_D1	SD2_ CLK	CSI_ D2	CSI_D7	USBH1_ TXDM	USBH1_ RXDP	USBG_ ON	USBG_ RXDP	SAP_ RXDAT	SSI1_ RXDAT	SSI2_ CLK	CSPI2_SS0	CSPI2_ SCLK
E	LD8	LD4	LD15	SPL_ SPR												SAP_ CLK	CSPI2_ MISO	CSPI1_SS2	CSPI2_ MOSI
F	A24_ NFIO14	D31	A25_ NFIO15	LSCLK												CSPI1_ SS1	CSPI1_ MISO	KP_ROW0	CSPI1_ SS0
G	A22_ NFIO12	D29	A23_ NFIO13	D30			NVDD6	NVSS6	CSI_D3	USB_ BYP	USBH_ ON	USBG_ SDA	USBG_ TXDP			KP_ ROW1	KP_ ROW3	UART2_CTS	KP_ ROW4
H	A20	D27	A21_ NFIO11	D28			NVDD1	NVSS5	CSI_D5	CSPI1_ SCLK	CSPI1_ RDY	USBH1_ TXDP	USBG_ OE			TEST_ WB4	TEST_ WB2	TEST_WB3	PWMO
J	A19	A18	D25	D26			NVDD1	NVDD5	NVDD4	KP_ ROW5	KP_ ROW2	CSPI1_ MOSI	TEST_ WB0			UART2_ RTS	KP_COL1	KP_COL0	TEST_ WB1
K	A16	A17	D23	D24			NVSS1	NVSS4	QVDDX	UART1_ RXD	TDO	QVDD	QVSS			KP_ COL3	KP_COL5	KP_COL4	KP_ COL2
L	A14_ NFIO9	A15_ NFIO10	D21	D22			NVSS1	NVDD3	QVDD	QVSS	NFIO2	NFWP	UART1_ TXD			UART2_ TXD	UART3_ RTS	UART3_CTS	UART3_ TXD
M	D19	A13_ NFIO8	D20	D18			NVDD2	NVDD3	NVSS3	QVSS	NFIO7	NFRB	EXT_ 48M			UART2_ RXD	UART3_ RXD	UART1_RTS	UART1_ CTS
N	A11	A12	D17	D16			LBA	NVSS3	SDCKE0	NVSS1	NVSS1	NVDD1	NVDD1			SD1_ D0	TCK	SD1_D1	RTCK
P	A9	A10	D15	D14												SD1_ D2	SD1_ CMD	TDI	TMS
R	A7	A8	D13	D12												SD1_ CLK	EXT_ 266M	NVSS2	TRST
T	A5	A6	EB3	D10	CS3	CS1	BCLK	MA11	RAS	CAS	NFIO5	NFIO3	NFWE	RESET_ IN	NFCE	BOOT1	SD1_D3	CLKMODE1	CLK MODE0
U	D11	EB1	EB2	OE	CS4	D6	ECB	D3	MA10	PC_ PWRON	PF16	NFIO4	NFIO1	NFALE	NFCLE	POR	BOOT2	BOOT3	XTAL32K
V	A4	EB0	D9	D8	CS5	D5	CS0	RW	D1	JTAG_ CTRL	SDWE	CLKO	NFIO6	QVSS	RESET_ OUT	BOOT0	OSC26M_ TEST	VDDA	EXTAL 32K
W	A3	A2	D7	A1	CS2	A0	D4	D2	D0	SDCLK	SDCKE1	NFIO0	NFRE	QVDD	QVSS	EXTAL 26M	XTAL26M	QVDD	QVSS

5 Document Revision History

Table 48 provides the document changes for the MC9328MX21 Rev. 3.4.

Table 48. Document Revision History

Location	Description of Change
Table 30 on page 46	Updated the table by removing the table footnote
Table 1 on page 3	Added VM and CVM devices.
Table 7 on page 16	Updated Sleep Current values.
Table 1 on page 4	Added a part number MC9328MX21CJM and a footnote.