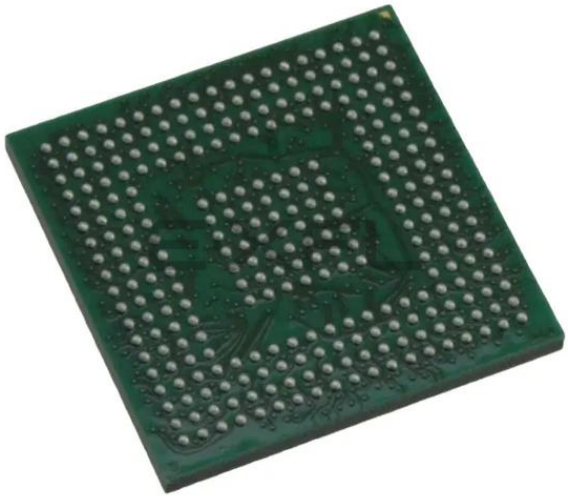

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21dvm

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

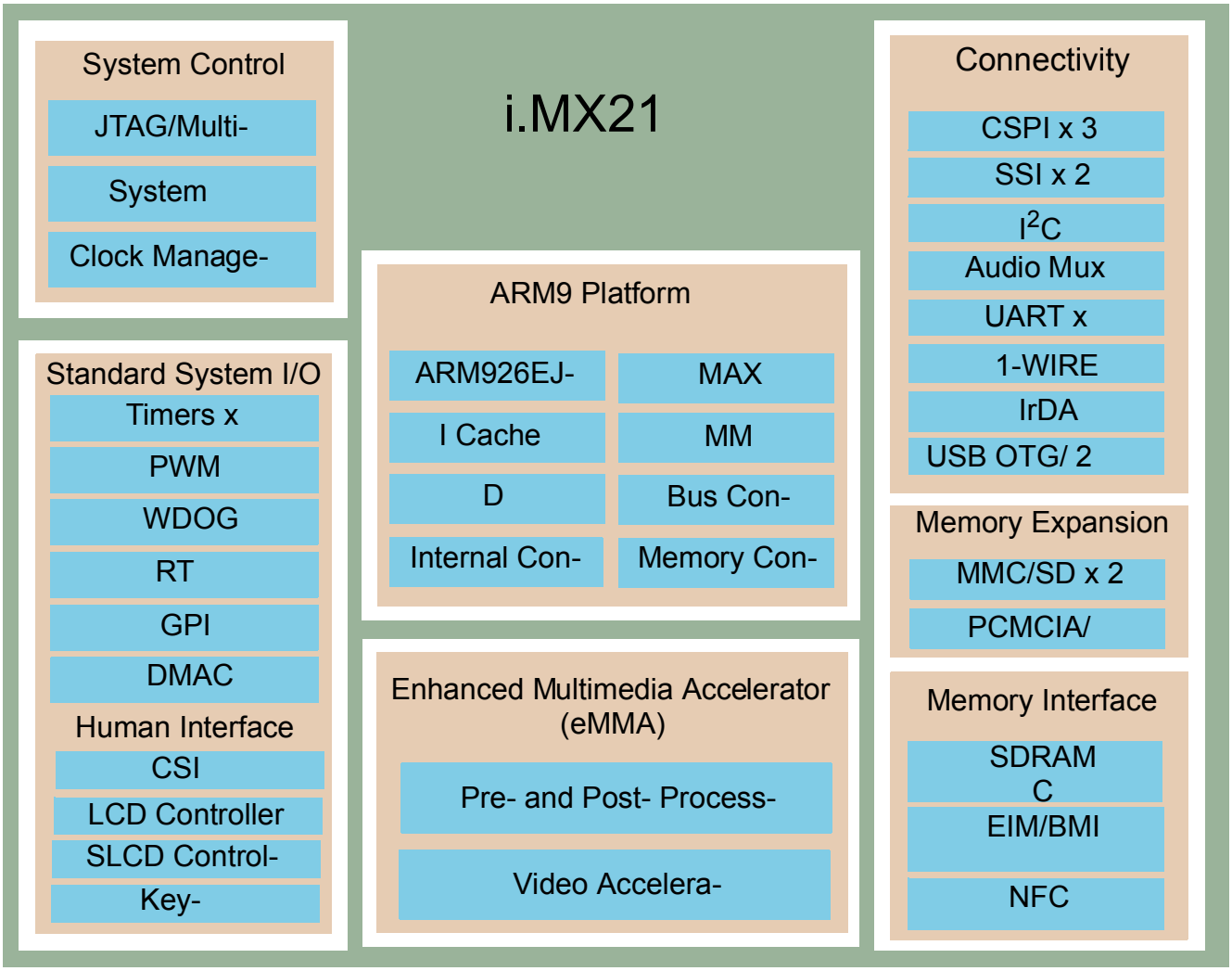


Figure 1. i.MX21 Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.
KP_ROW[7:0]	Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2\_RTS}}$ and $\overline{\text{UART2\_RXD}}$ signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available.
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6.
NVSS	Noisy Ground for the I/O pins

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK, VM	T_A	0	70	°C
	DVK, DVM	T_A	-30	70	°C
	CVK, CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V

The output External Grant signal from the DMAC is an active-low signal.When the following conditions are true, the External DMA Grant signal is asserted with the initiation of the DMA burst.

- The DMA channel for which the DMA burst is ongoing has request source as external DMA Request
  (as per source select register setting).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

After the grant is asserted, the External DMA request will not be sampled until completion of the DMA burst. As the external request is synchronized, the request synchronization will not be done during this period. The priority of the external request becomes low for the next consecutive burst, if another DMA request signal is asserted.

Worst case—that is, the smallest burst (1 byte read/write) timing diagrams are shown in Figure 4 and Figure 5. Minimum and maximum timings for the External request and External grant signals are present in Table 13.

Figure 4 shows the minimum time for which the External Grant signal remains asserted when an External DMA request is de-asserted immediately after sensing grant signal active.

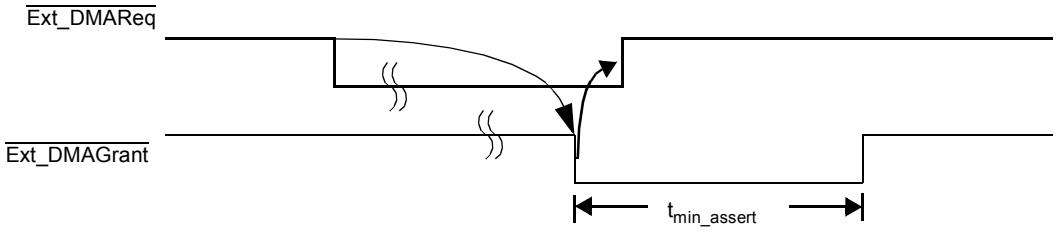
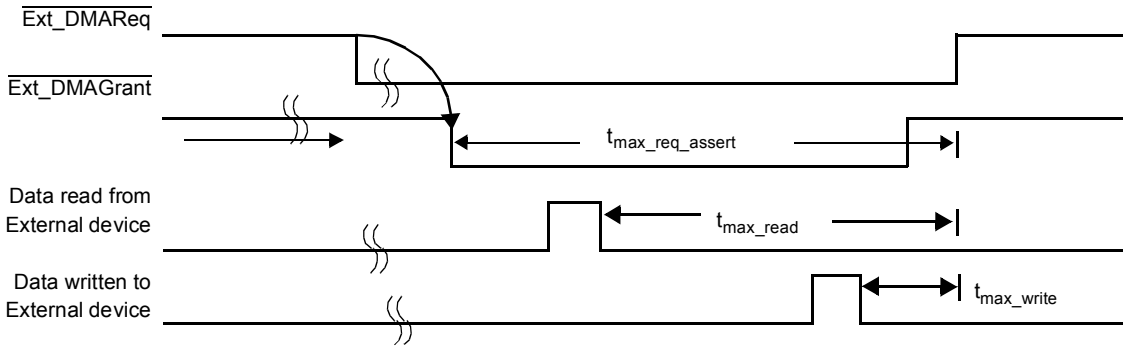


Figure 4. Assertion of DMA External Grant Signal

Figure 5 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.



NOTE: Assuming in worst case the data is read/written from/to External device as per the above waveform.

Figure 5. Safe Maximum Timings for External Request De-Assertion

Table 13. DMA External Request and Grant Timing Parameters

Parameter	Description	3.0 V		1.8 V		Unit
		WCS	BCS	WCS	BCS	
t_{min_assert}	Minimum assertion time of External Grant signal	8 hclk + 8.6	8 hclk + 2.74	8 hclk + 7.17	8 hclk + 3.25	ns
$t_{max\_req\_assert}$	Maximum External request assertion time after assertion of Grant signal	9 hclk - 20.66	9 hclk - 6.7	9 hclk - 17.96	9 hclk - 8.16	ns
t_{max_read}	Maximum External request assertion time after first read completion	8 hclk - 6.21	8 hclk - 0.77	8 hclk - 5.84	8 hclk - 0.66	ns
t_{max_write}	Maximum External request assertion time after completion of first write	3 hclk - 15.87	3 hclk - 8.83	3 hclk - 15.9	3 hclk - 9.12	ns

3.8 BMI Interface Timing Diagram

3.8.1 Connecting BMI to ATI MMD Devices

3.8.1.1 ATI MMD Devices Drive the BMI_CLK/CS

In this mode MMD_MODE_SEL bit is set and MMD_CLKOUT bit is cleared. $\overline{\text{BMI\_WRITE}}$ and BMI_CLK/CS are input signals to BMI driving by ATI MMD chip set. Output signal BMI_READ_REQ can be used as interrupt signal to inform MMD that data is ready in BMI TxFIFO for read access. MMD can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

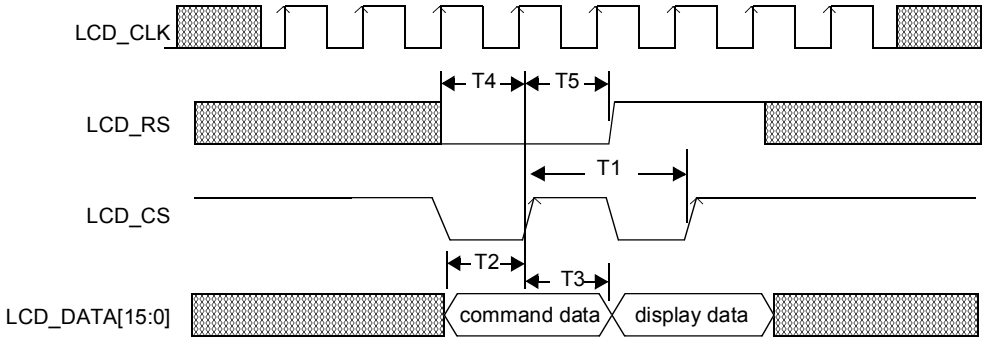
3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

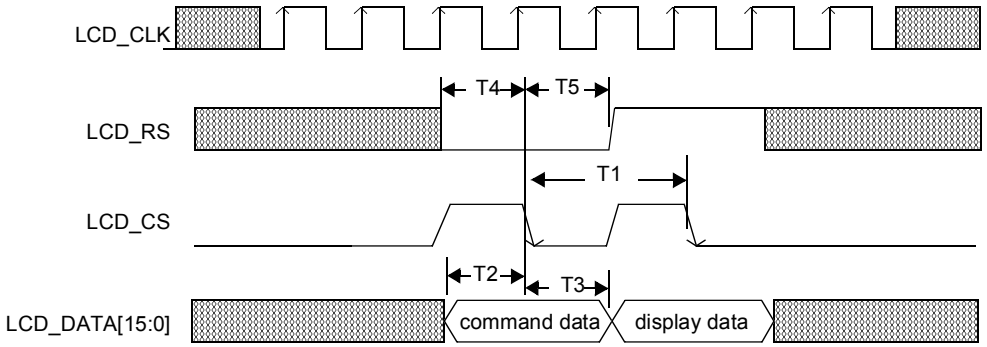
On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

Table 24. SLCDC Serial Transfer Timing

Symbol	Description	Minimum	Maximum	Unit
T1	Pixel clock period	42	962	ns
T2	Chip select setup time	5	–	ns
T3	Chip select hold time	5	–	ns
T4	Data setup time	5	–	ns
T4	Data hold time	5	–	ns
T6	Register select setup time	5	–	ns
T7	Register select hold time	5	–	ns



CSPOL = 0



CSPOL = 1

Figure 24. SLCDC Parallel Transfers Timing

Table 25. SLCDC Parallel Transfers Timing

Symbol	Description	Minimum	Maximum	Unit
T1	Pixel clock period	23	962	ns
T2	Data setup time	5	–	ns
T3	Data hold time	5	–	ns
T4	Register select setup time	5	–	ns
T5	Register select hold time	5	–	ns

3.15 SDRAM Memory Controller

The following figures (Figure 38 through Figure 41) and their associated tables specify the timings related to the SDRAMC module in the i.MX21.

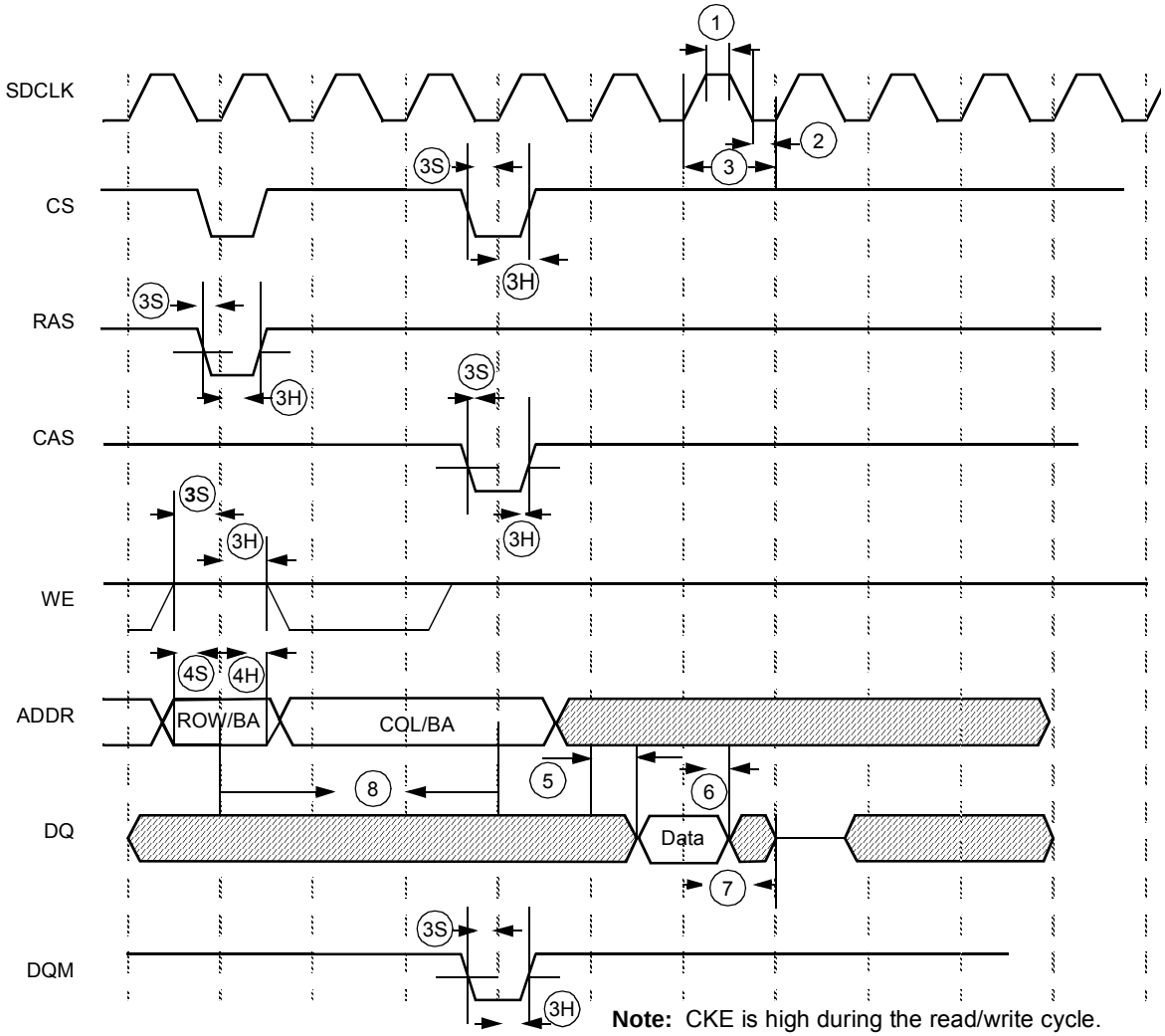


Figure 38. SDRAM Read Cycle Timing Diagram

Table 31. SDRAM Read Cycle Timing Parameter

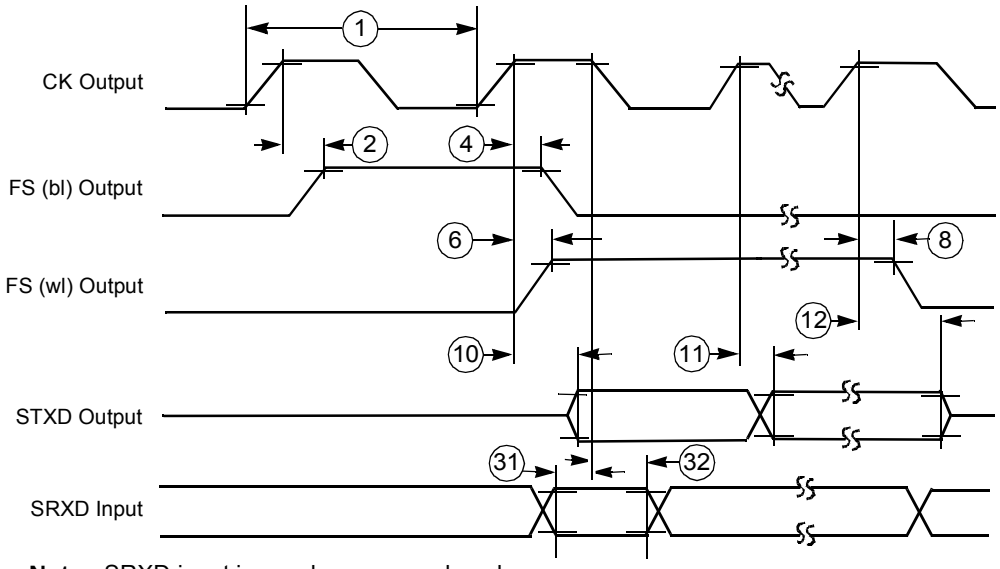
Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	$\overline{\text{SDRAM clock low-level width}}$	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	4.78	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	3.03	–	2	–	ns

3.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 42 through Figure 45.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.

The SSI can be connected to 4 set of ports, SAP, SSI1, SSI2 and SSI3.



Note: SRXD input in synchronous mode only.

Figure 42. SSI Transmitter Internal Clock Timing Diagram

Table 37. SSI to SSI3 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI3 Ports)						
1	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-2.09	-0.66	-2.09	-0.66	ns
3	(Rx) CK high to FS (bl) high	-2.74	-0.84	-2.74	-0.84	ns
4	(Tx) CK high to FS (bl) low	-2.09	-0.66	-2.09	-0.66	ns
5	(Rx) CK high to FS (bl) low	-2.74	-0.84	-2.74	-0.84	ns
6	(Tx) CK high to FS (wl) high	-2.09	-0.66	-2.09	-0.66	ns
7	(Rx) CK high to FS (wl) high	-2.74	-0.84	-2.74	-0.84	ns
8	(Tx) CK high to FS (wl) low	-2.09	-0.66	-2.09	-0.66	ns
9	(Rx) CK high to FS (wl) low	-2.74	-0.84	-2.74	-0.84	ns
10	(Tx) CK high to STXD valid from high impedance	-1.73	-0.26	-1.73	-0.26	ns
11a	(Tx) CK high to STXD high	-2.87	-0.80	-2.87	-0.80	ns
11b	(Tx) CK high to STXD low	-2.87	-0.80	-2.87	-0.80	ns
12	(Tx) CK high to STXD high impedance	-1.73	-0.26	-1.73	-0.26	ns
13	SRXD setup time before (Rx) CK low	22.77	–	22.77	–	ns
14	SRXD old ime after r Rx) CK low (	0	–	0	–	ns
External Clock Operation (SSI3 Ports)						
15	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	9.62	17.10	7.90	15.61	ns
19	(Rx) CK high to FS (bl) high	10.30	19.54	8.58	18.05	ns
20	(Tx) CK high to FS (bl) low	9.62	17.10	7.90	15.61	ns
21	(Rx) CK high to FS (bl) low	10.30	19.54	8.58	18.05	ns
22	(Tx) CK high to FS (wl) high	9.62	17.10	7.90	15.61	ns
23	(Rx) CK high to FS (wl) high	10.30	19.54	8.58	18.05	ns
24	(Tx) CK high to FS (wl) low	9.62	17.10	7.90	15.61	ns
25	(Rx) CK high to FS (wl) low	10.30	19.54	8.58	18.05	ns
26	(Tx) CK high to STXD valid from high impedance	9.02	16.46	7.29	14.97	ns
27a	(Tx) CK high to STXD high	8.48	15.32	6.75	13.83	ns
27b	(Tx) CK high to STXD low	8.48	15.32	6.75	13.83	ns

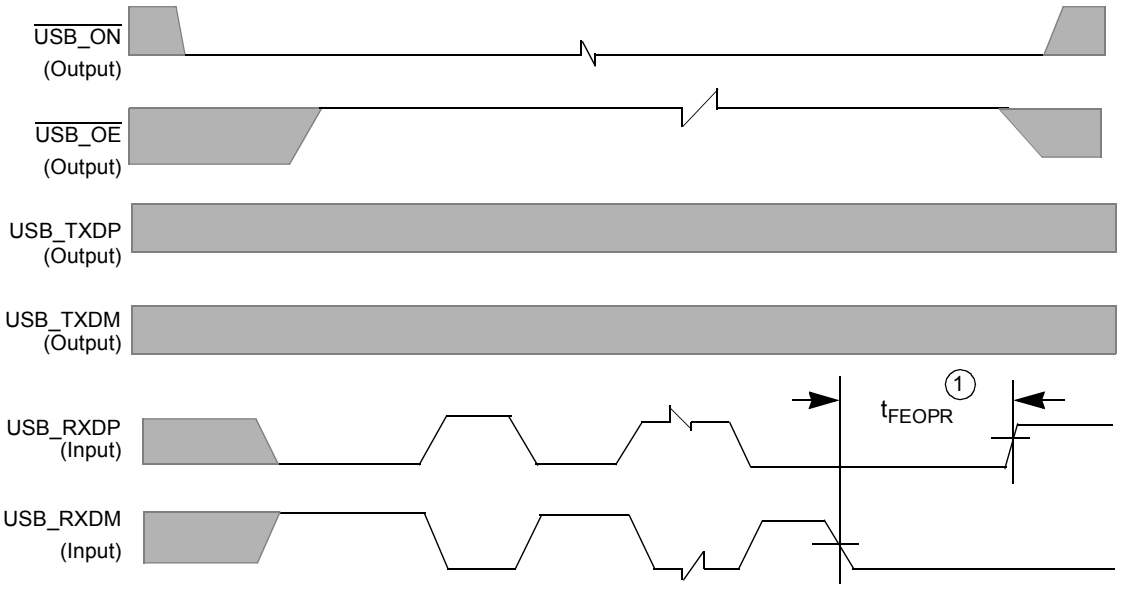


Figure 51. USB Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 41. USB Timing Parameters for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	–	ns

The USBOTG I^2C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

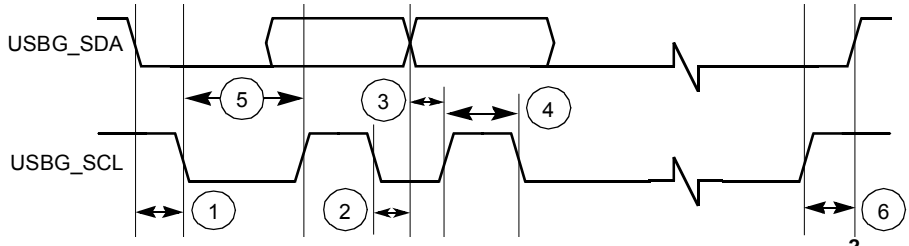


Figure 52. USB Timing Diagram for Data Transfer from USB Transceiver (I^2C)

Table 42. USB Timing Parameters for Data Transfer from USB Transceiver (I^2C)

Ref No.	Parameter	1.8 V ± 0.1 V		Unit
		Minimum	Maximum	
1	Hold time (repeated) START condition	188	–	ns
2	Data hold time	0	188	ns
3	Data setup time	88	–	ns
4	HIGH period of the SCL clock	500	–	ns
5	LOW period of the SCL clock	500	–	ns
6	Setup time for STOP condition	185	–	ns

Note: Signals listed with lower case letters are internal to the device.

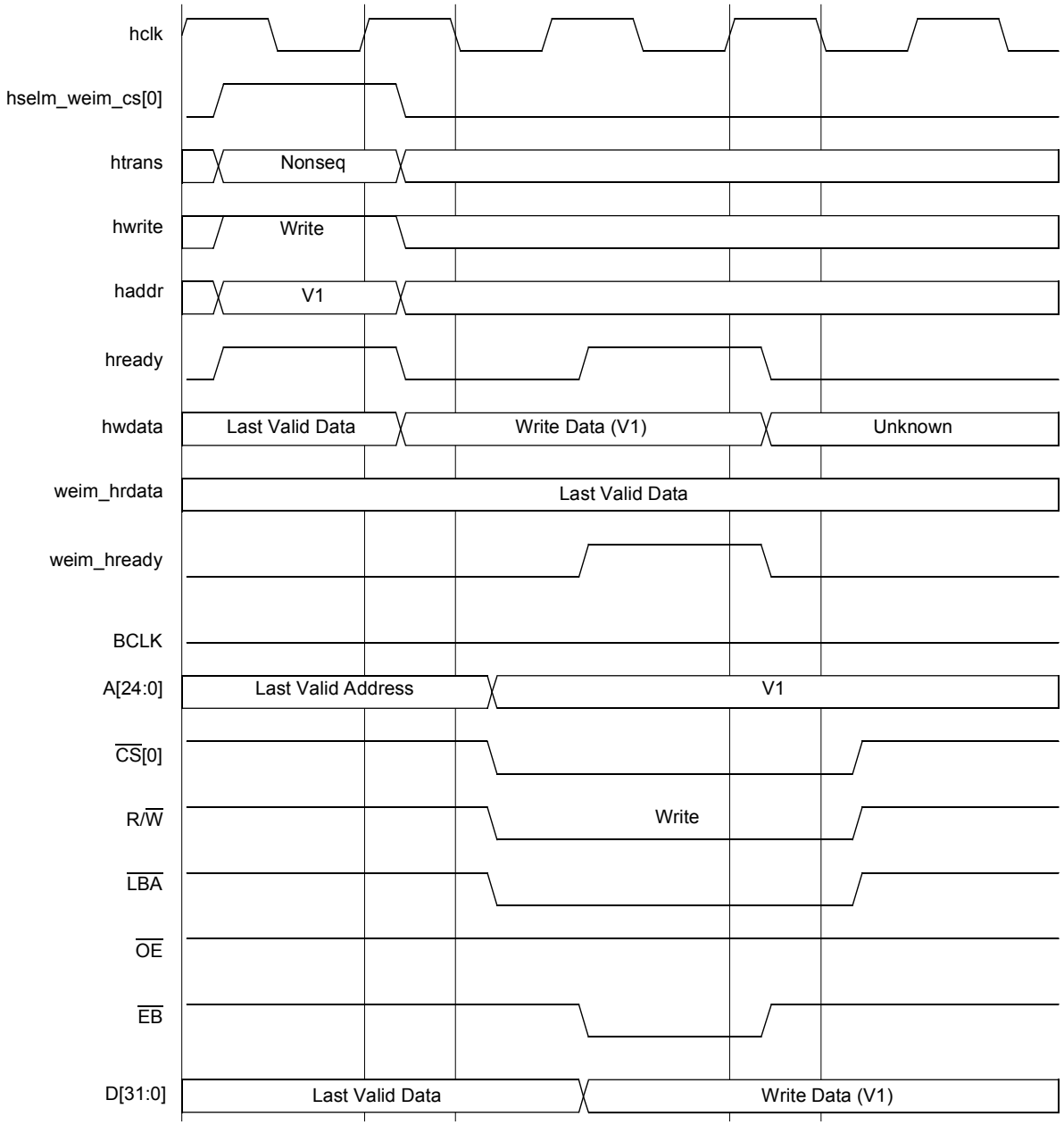


Figure 55. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

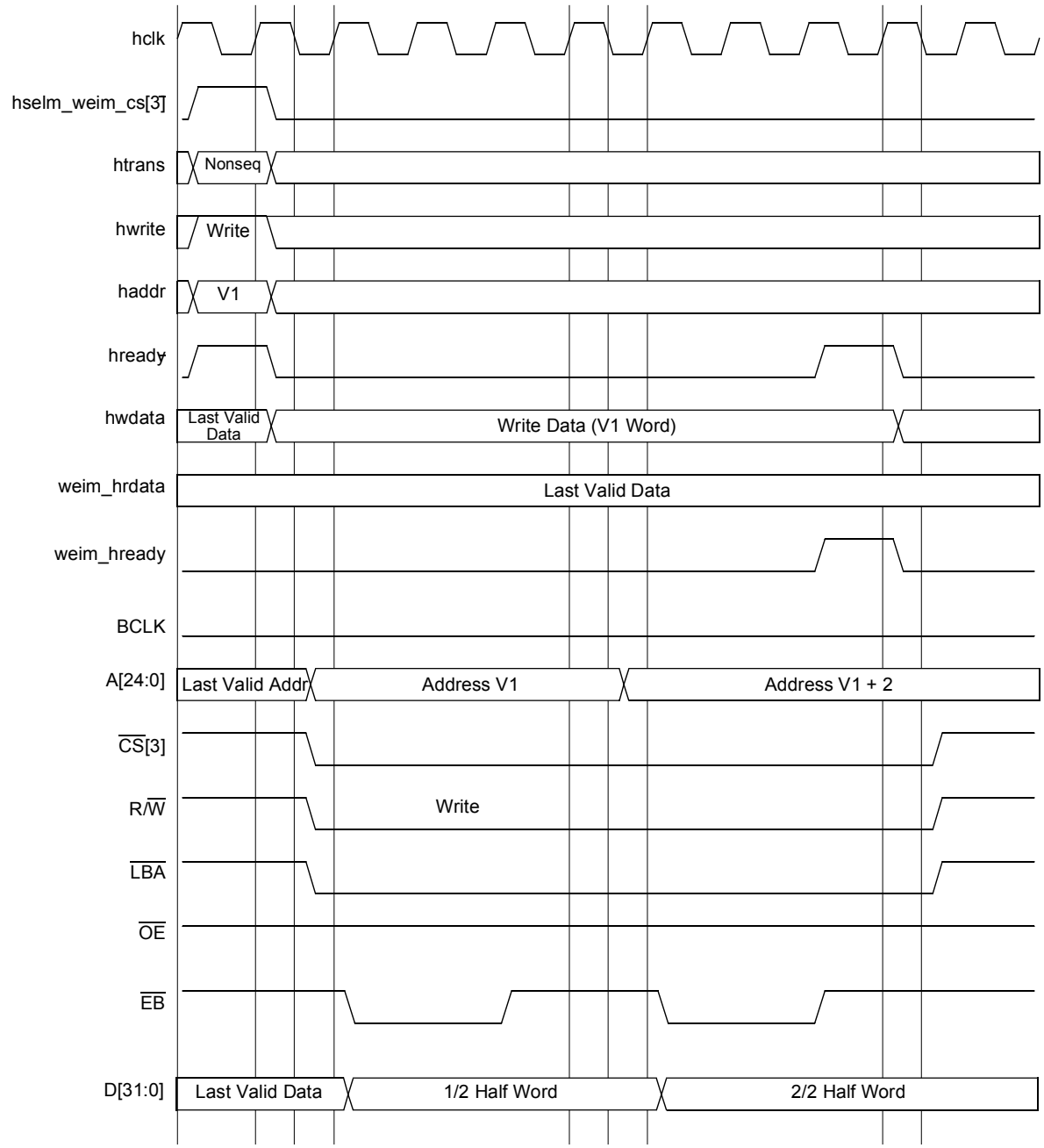


Figure 59. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

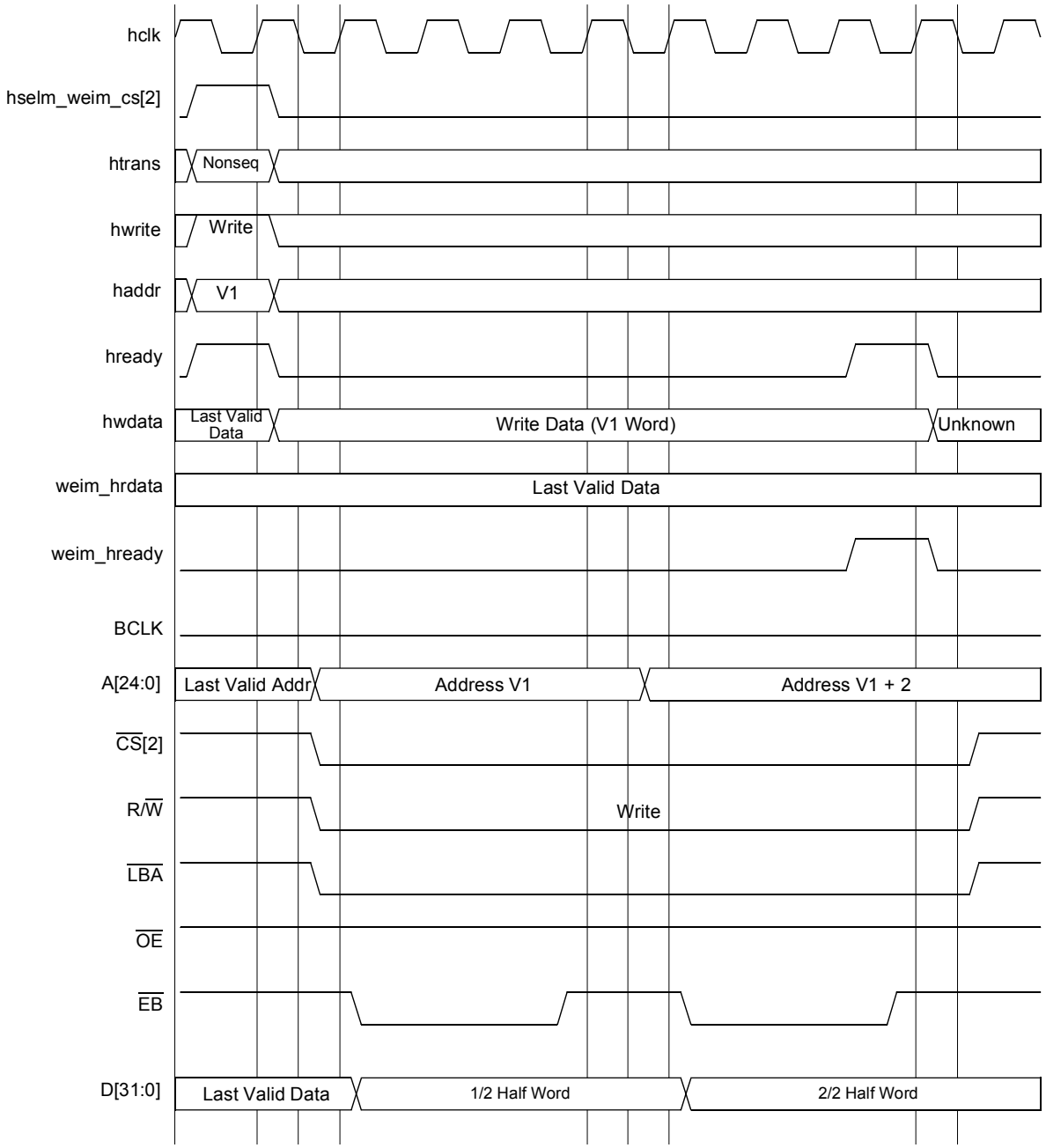


Figure 65. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

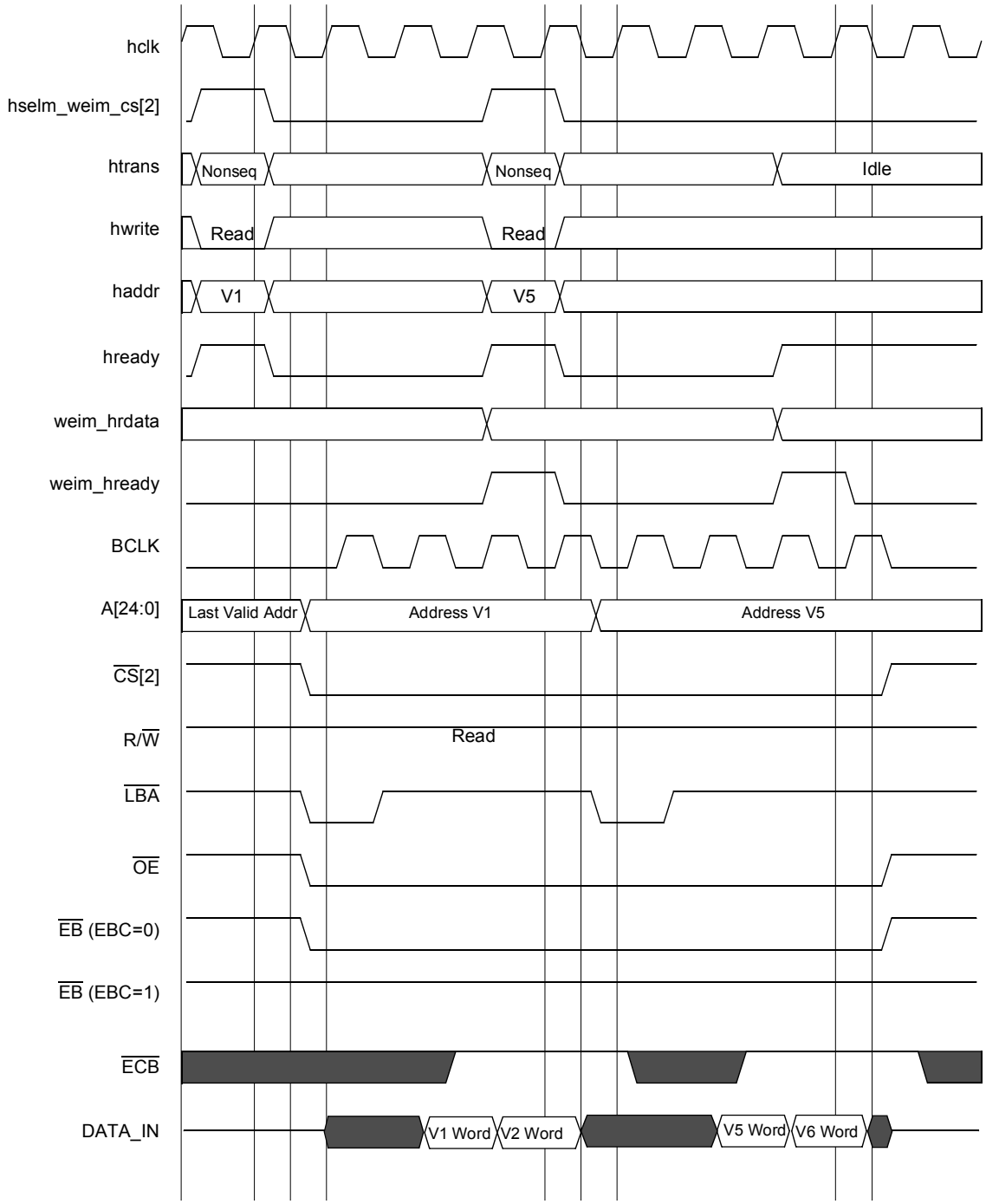


Figure 72. WSC = 3, SYNC = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

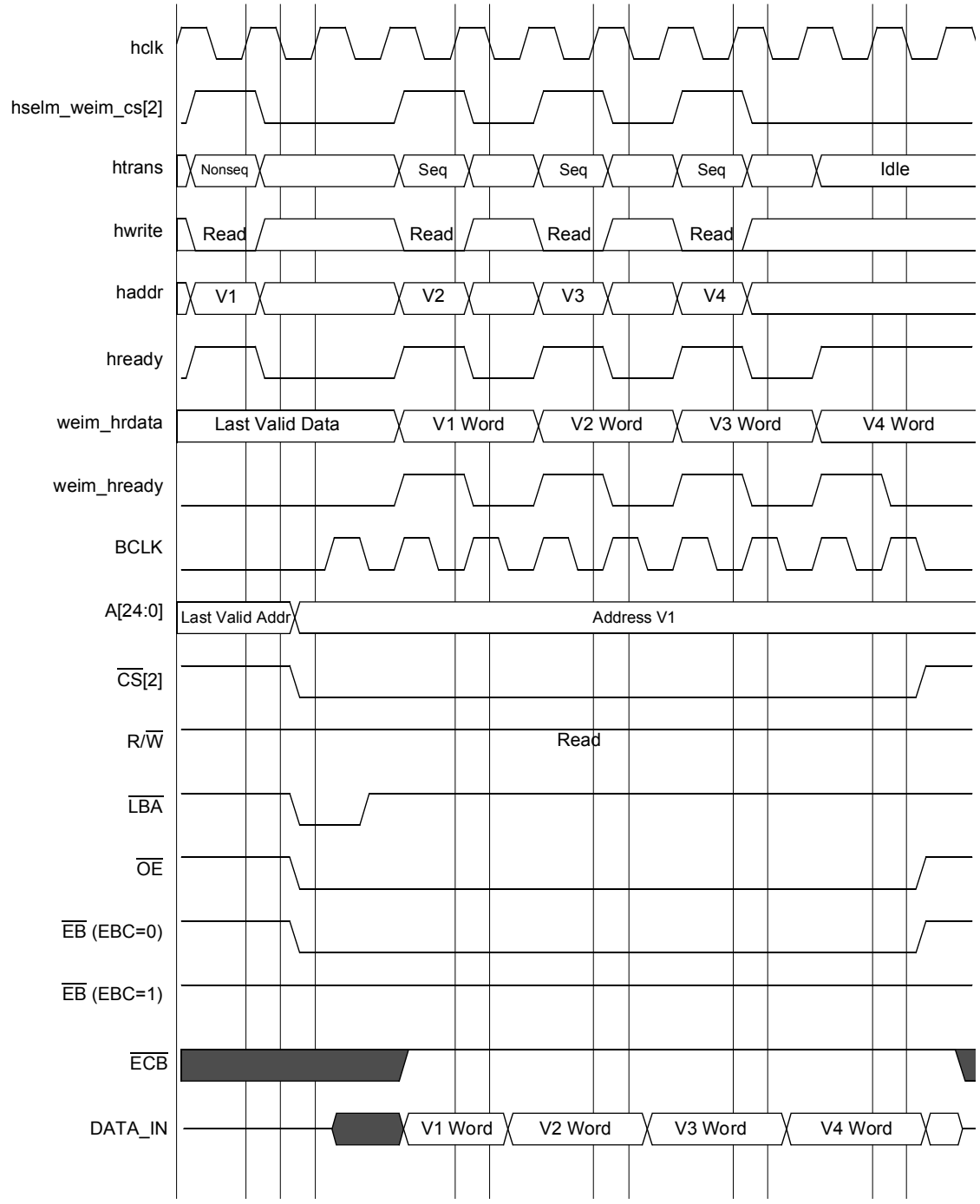


Figure 73. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Note: Signals listed with lower case letters are internal to the device.

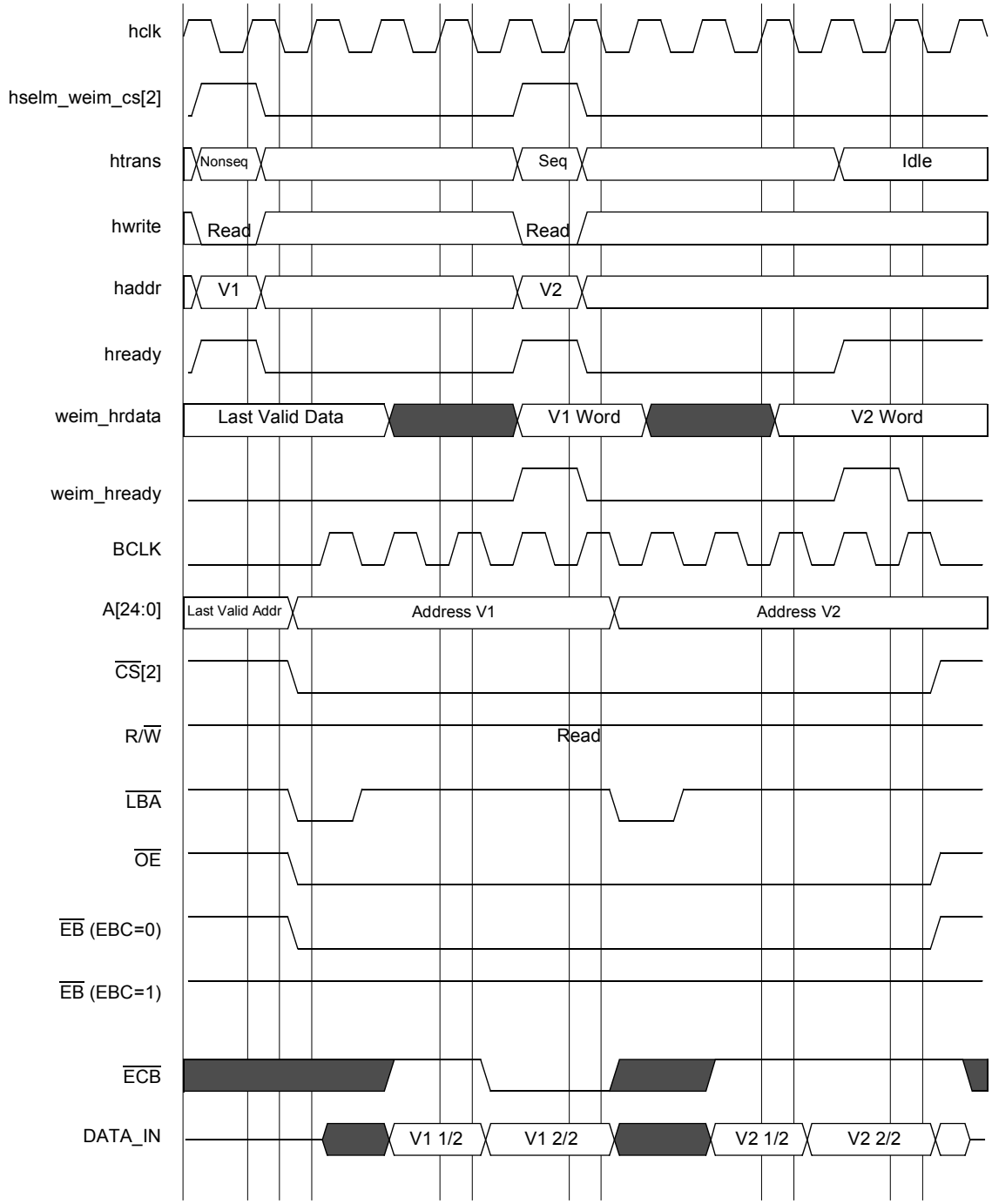


Figure 74. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

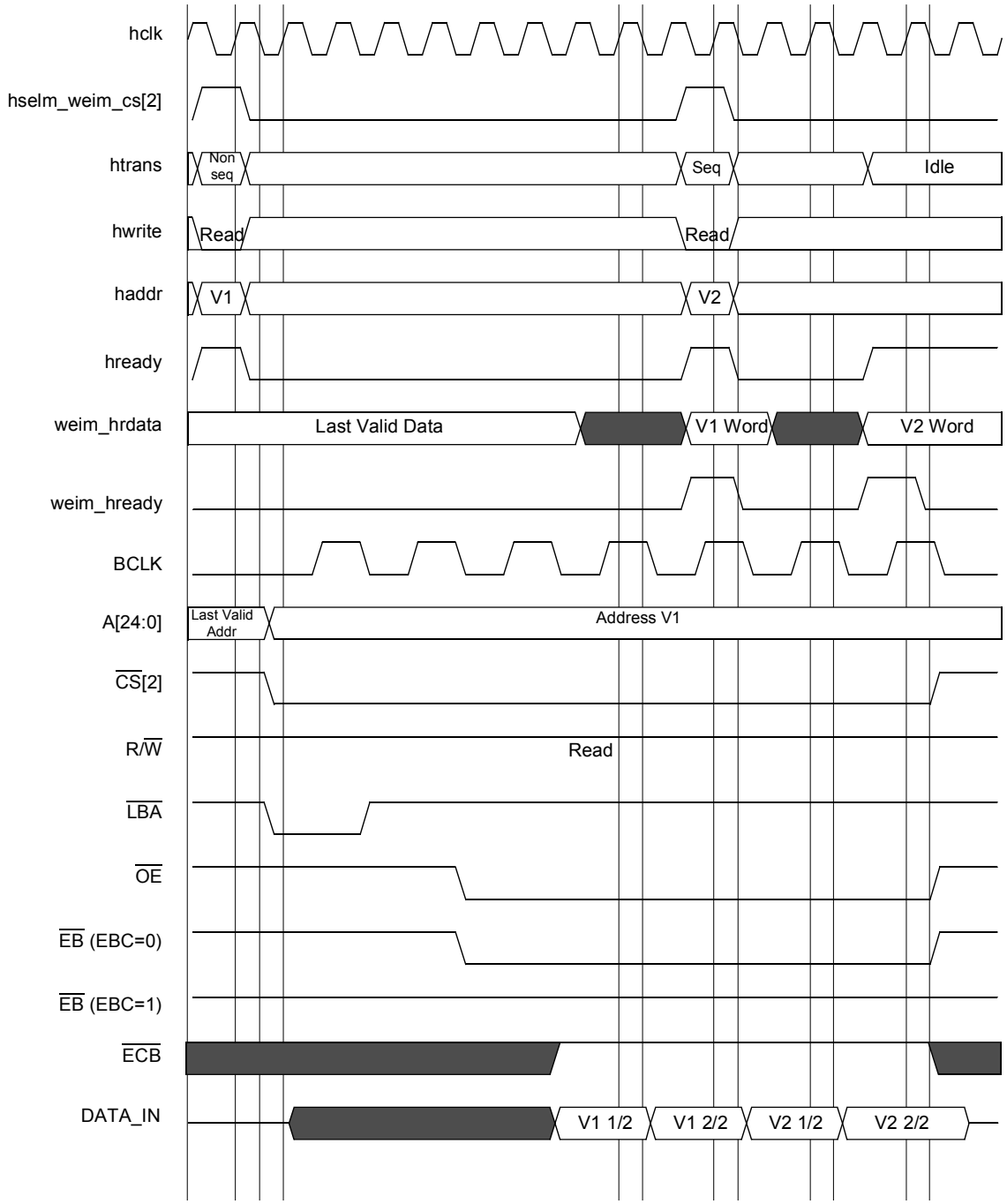


Figure 76. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

3.20 DTACK Mode Memory Access Timing Diagrams

When enabled, the DTACK input signal is used to externally terminate a data transfer. For DTACK enabled operations, a bus time-out monitor generates a bus error when an external bus cycle is not terminated by the DTACK input signal after 1024 HCLK clock cycles have elapsed, where HCLK is the internal system clock driven from the PLL module. For a 133 MHz HCLK setting, this time equates to 7.7 µs. Refer to the Section 3.5, "DPLL Timing Specifications" for more information on how to generate different HCLK frequencies.

There are two modes of operation for the DTACK input signal: rising edge detection or level sensitive detection with a programmable insensitivity time. DTACK is only used during external asynchronous data transfers, thus the SYNC bit in the chip select control registers must be cleared.

During edge detection mode, the EIM will terminate an external data transfer following the detection of the DTACK signal's rising edge, so long as it occurs within the 1024 HCLK cycle time. Edge detection mode is used for devices that follow the PCMCIA standard. Note that DTACK rising edge detection mode can only be used for $\overline{CS}$[5] operations. To configure $\overline{CS}$[5] for DTACK rising edge detection, the following bits must be programmed in the Chip Select 5 Control Register and EIM Configuration Register:

- WSC bit field set to 0x3F and CSA (or CSN) set to 1 or greater in the Chip Select 5 Control Register
- AGE bit set in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device. The requirement of setting CSA or CSN is required to allow the EIM to wait for the rising edge of DTACK during back-to-back external transfers, such as during DMA transfers or an internal 32-bit access through an external 16-bit data port.

During level sensitive detection, the EIM will first hold off sampling the DTACK signal for at least 2 HCLK cycles, and up to 5 HCLK cycles as programmed by the DCT bits in the Chip Select Control Register. After this insensitivity time, the EIM will sample DTACK and if it detects that DTACK is logic high, it will continue the data transfer at the programmed number of wait states. However, if the EIM detects that DTACK is logic low, it will wait until DTACK goes to logic high to continue the access, so long as this occurs within the 1024 HCLK cycle time. If at anytime during an external data transfer DTACK goes to logic low, the EIM will wait until DTACK returns to logic high to resume the data transfer. Level detection is often used for asynchronous devices such graphic controller chips. Level detection may be used with any chip select except CS[4] as it is multiplexed with the DTACK signal. To configure a chip select for DTACK level sensitive detection, the following bits must be programmed in the Chip Select Control Register and EIM Configuration Register:

- EW bit set, WSC set to > 1, and CSN set to < 3 in the Chip Select Control Register
- BCD/DCT set to desired "insensitivity time" in the Chip Select Control Register. The "insensitivity time" is dictated by the external device's timing requirements.
- AGE bit cleared in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device.

The waveforms in the following section provide examples of the DTACK signal operation.

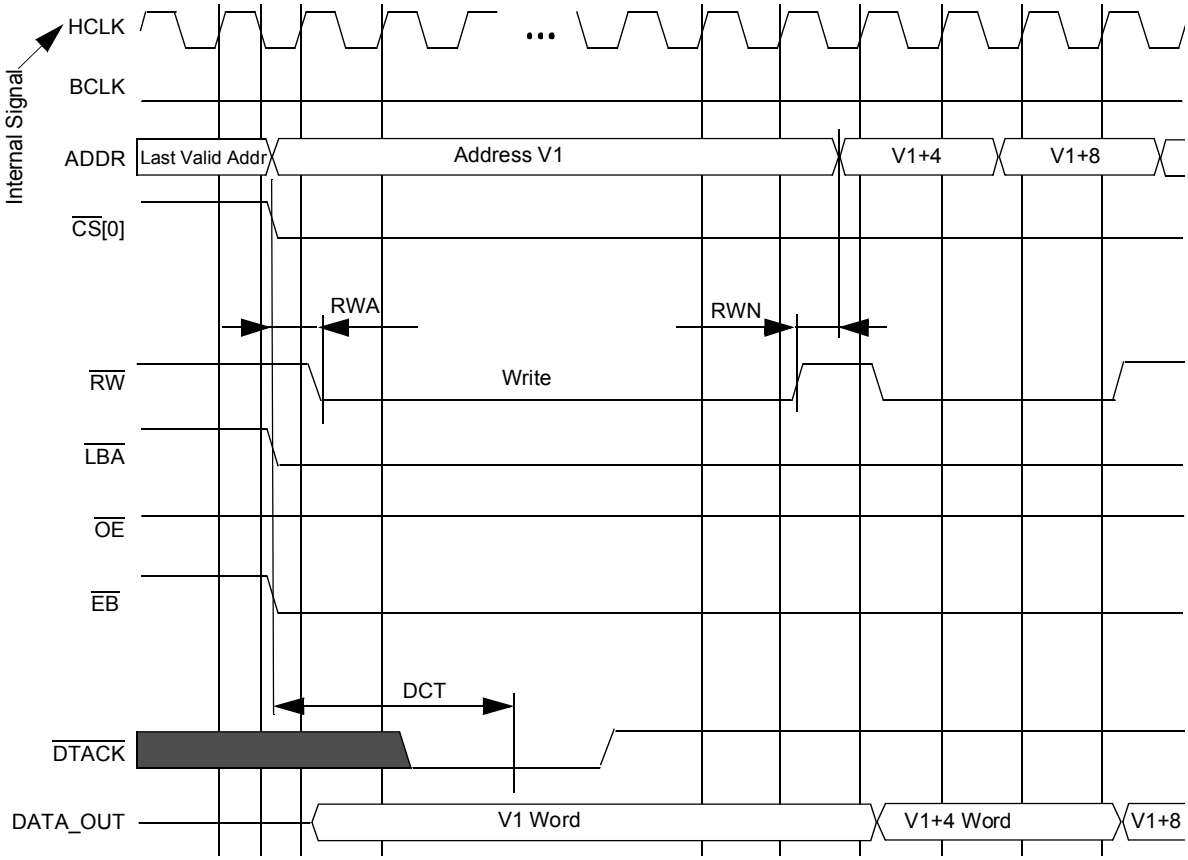
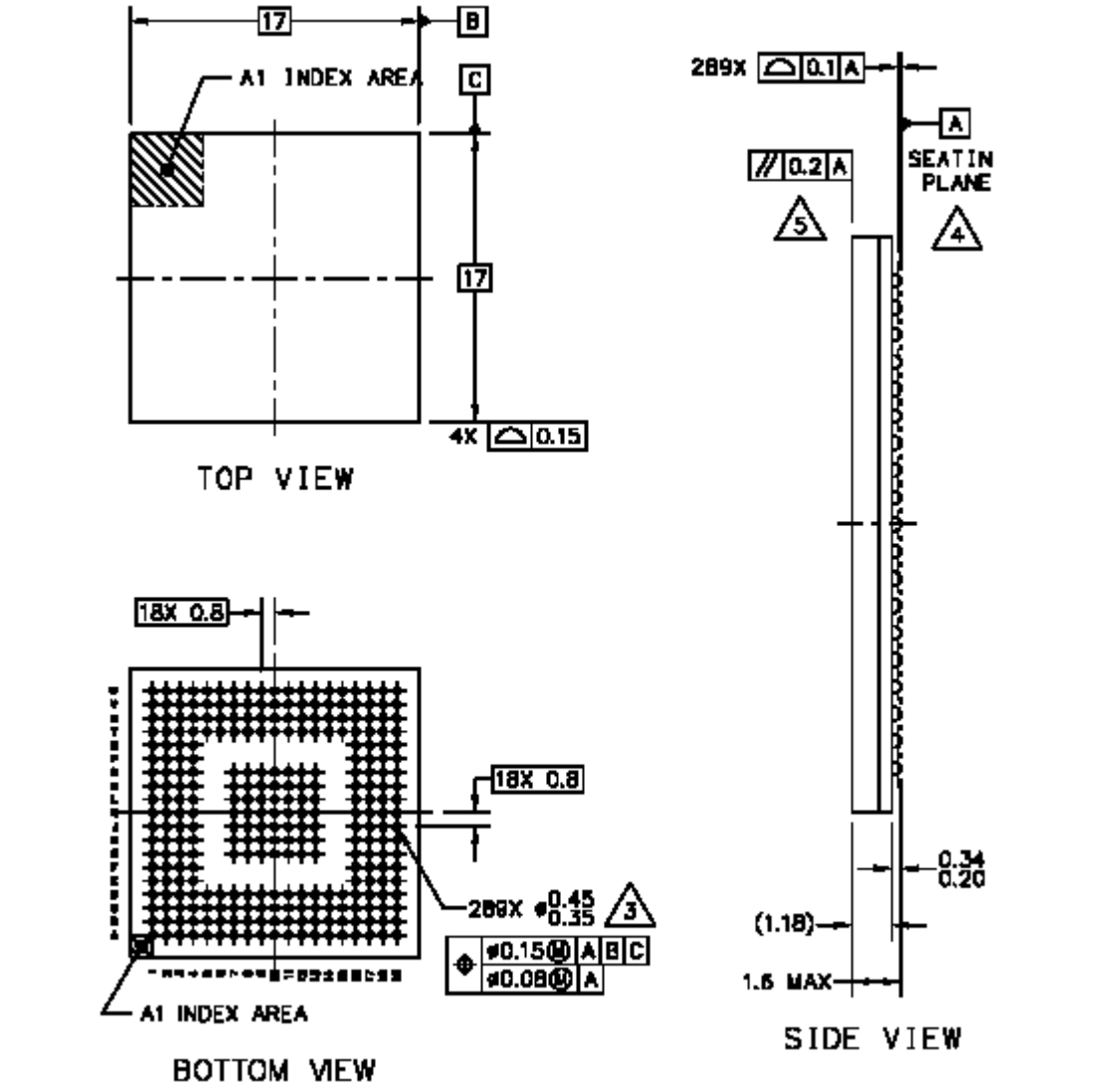


Figure 79. DTACK Level Sensitive Sequential Write Accesses, WSC=2, EW=1, RWA=1, RWN=1, DCT=1, AGE=0 (Example of DTACK Asserting)

4.2 MAPBGA Package Dimensions

Figure 86 illustrates the MAPBGA 17 mm × 17 mm × 1.45 mm package, which has 0.8 mm spacing between the pads.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 86. i.MX21 MAPBGA Mechanical Drawing