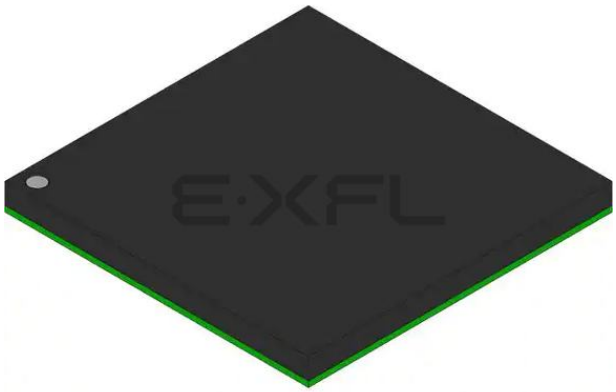


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx21dvmr2

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

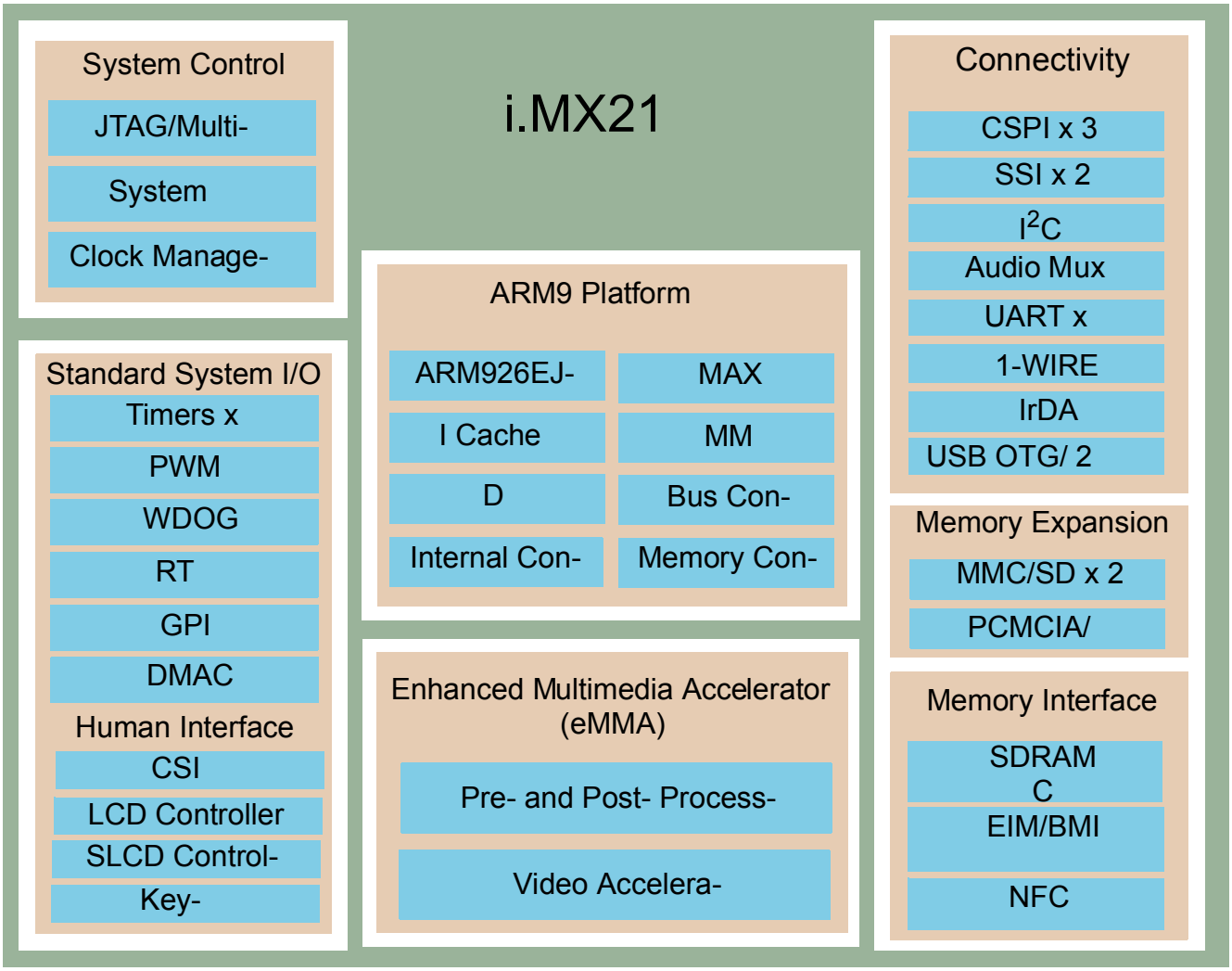


Figure 1. i.MX21 Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.

- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Target Applications

The i.MX21 is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers based on the popular Palm OS platform, and messaging applications.

1.3 Reference Documentation

The following documents are required for a complete description of the i.MX21 and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM7TDMI Data Sheet (ARM Ltd., order number ARM DDI 0029)

ARM920T Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

MC9328MX21 Product Brief (order number MC9328MX21P)

MC9328MX21 Reference Manual (order number MC9328MX21R*M)*

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.4 Ordering Information

Table 1 provides ordering information for the device.

Table 1. Ordering Information[1]

Part Order Number	Package Size	Package Type	Operating Range
MC9328MX21VK!	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	0°C–70°C
MC9328MX21VM!	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	0°C–70°C

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH2_FS	USB Host2 Full Speed output signal. This signal is multiplexed with CSPI2_SS[0] of CSPI2.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added. This signal is multiplexed with CSPI3_MOSI.
SD1_CLK	SD Output Clock. This signal is multiplexed with CSPI3_SCLK.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART2_RXD	Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP.
UART2_TXD	Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP.
$\overline{\text{UART2\_RTS}}$	Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP.
$\overline{\text{UART2\_CTS}}$	Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP.
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.
KP_ROW[7:0]	Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2\_RTS}}$ and $\overline{\text{UART2\_RXD}}$ signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available.
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6.
NVSS	Noisy Ground for the I/O pins

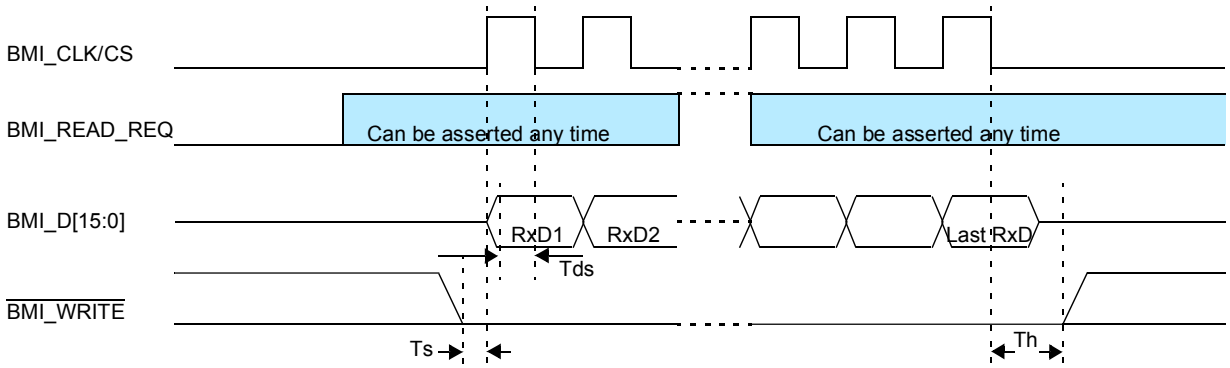


Figure 7. MMD (ATI) Drives Clock, MMD Write BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0, MMD_CLKOUT=0)

Table 15. MMD Write BMI Timing

Item	Symbol	Minimum	Typical	Maximum	Unit
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
$\overline{\text{write}}$ old ime h t	Th	0	–	–	ns
receive data setup time	Tds	5	–	–	ns

Note: All timings assume that the hclk is running at 133 MHz.

Note: At this mode, the maximum frequency of the BMI_CLK/CS can be up to 36 MHz (doubles as maximum data pad speed).

3.8.1.2 BMI Drives the BMI_CLK/CS

In this mode MMD_MODE_SEL and MMD_CLKOUT are both set. The software must know which mode it is now (READ or WRITE). When the $\overline{\text{BMI\_WRITE}}$ is high, BMI drives BMI_CLK/CS out if the TxFIFO is not emptied. When $\overline{\text{BMI\_WRITE}}$ is low, user can write a 1 to READ bit of control register1 to issue a write cycle (MMD write BMI).

3.8.1.3 MMD Read BMI Timing

Figure 13 shows the MMD read BMI timing when BMI drives the BMI_CLK/CS. When the $\overline{\text{BMI\_WRITE}}$ is high, the BMI drives BMI_CLK/CS out if data is written to TxFIFO (BMI_READ_REQ become high), BMI puts data into data bus and enable data out on the rising edge of BMI_CLK/CS. The MMD devices can latch the data on each falling edge of BMI_CLK/CS.

It is recommended that the MMD do not change the $\overline{\text{BMI\_WRITE}}$ signal from high to low when the BMI_READ_REQ is asserted. If user writes data to the TxFIFO when the $\overline{\text{BMI\_WRITE}}$ is low, the BMI will drive BMI_CLK/CS out once the $\overline{\text{BMI\_WRITE}}$ is changed from low to high.

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

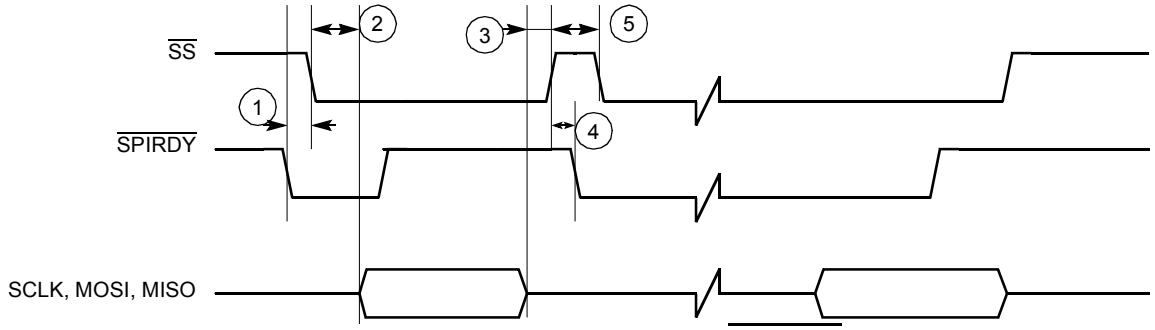


Figure 14. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger

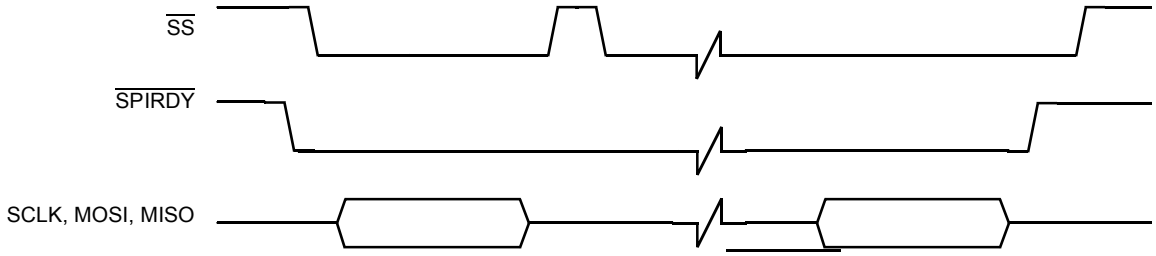


Figure 15. Master CSPI Timing Diagram Using SPI_RDY Level Trigger

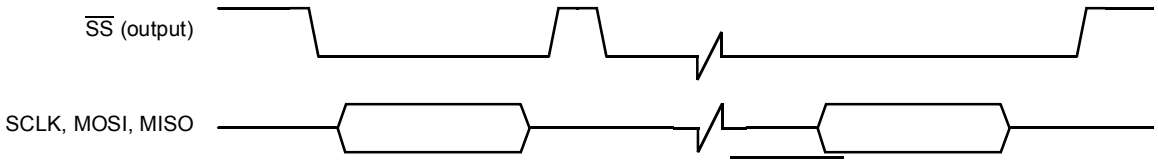


Figure 16. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger

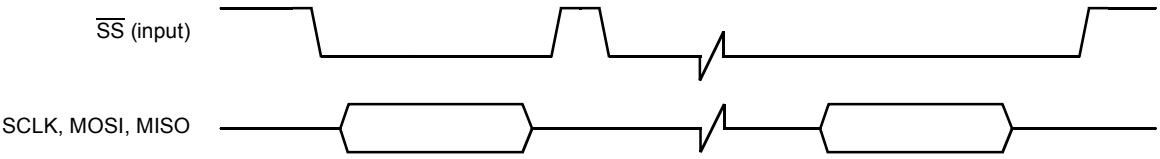


Figure 17. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT

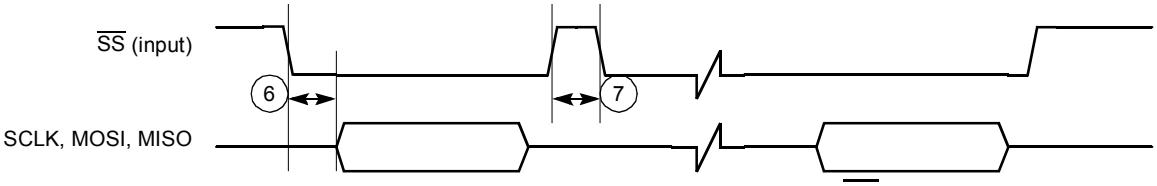


Figure 18. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge

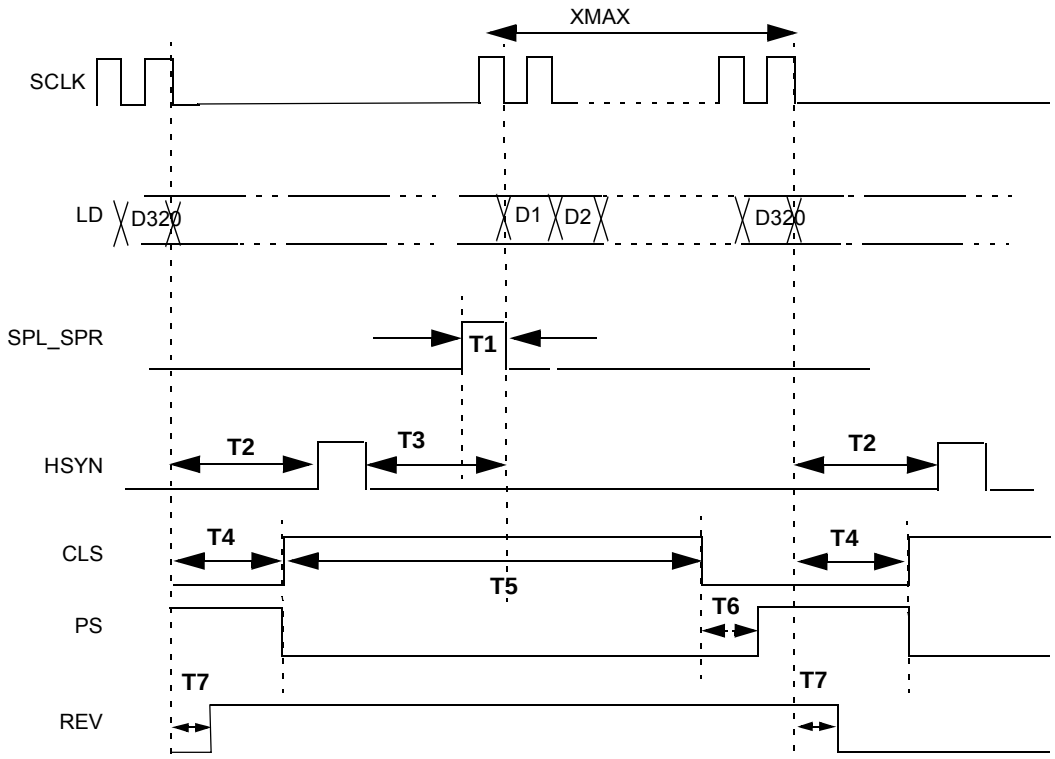


Figure 21. Sharp TFT Panel Timing

Table 22. Sharp TFT Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	SPL/SPR pulse width	–	1	Ts
T2	End of LD of line to beginning of HSYN	1	HWAIT1+1	Ts
T3	End of HSYN to beginning of LD of line	4	HWAIT2 + 4	Ts
T4	CLS rise delay from end of LD of line	3	CLS_RISE_DELAY+1	Ts
T5	CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	PS rise delay from CLS negation	0	PS_RISE_DELAY	Ts
T7	REV toggle delay from last LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note:
- Falling of SPL/SPR aligns with first LD of line.
- Falling of PS aligns with rising edge of CLS.
- REV toggles in every HSYN period.

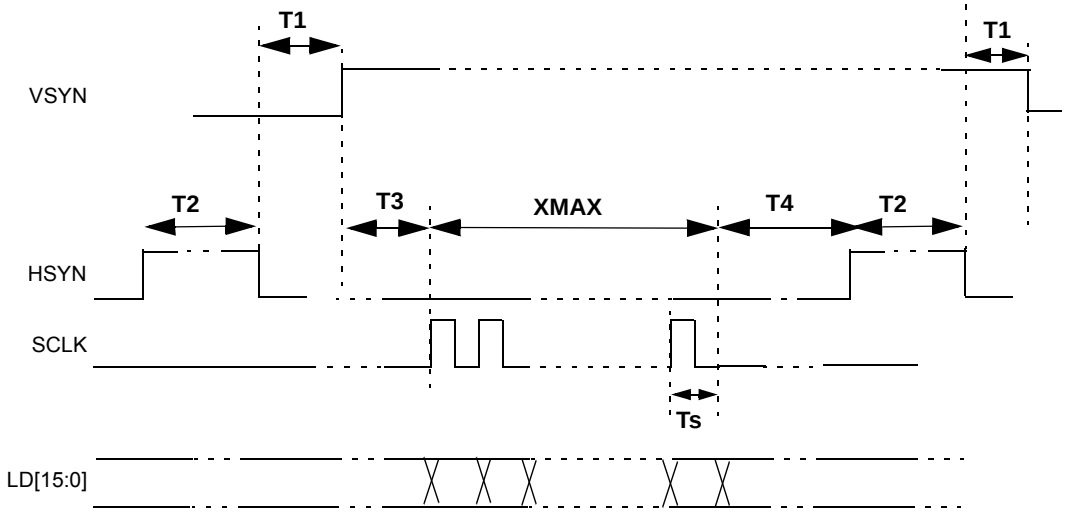


Figure 22. Non-TFT Mode Panel Timing

Table 23. Non-TFT Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	HSYN to VSYN delay	2	HWAIT2+2	Tpix
T2	HSYN pulse width	1	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts$	–
T4	SCLK to HSYN	1	HWAIT1+1	Tpix

Note:
- Ts is the SCLK period while Tpix is the pixel clock period.
- VSYN, HSYN and SCLK can be programmed as active high or active low. In Figure 67, all these 3 signals are active high.
- When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts.
- When it is in monochrome mode with bus width = 2, 4, and 8, T3 = 1, 2 and 4 Tpix respectively.

3.12 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

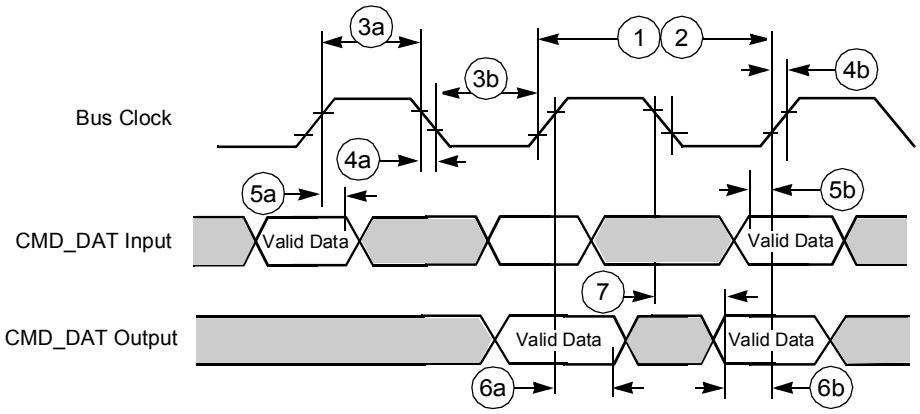


Figure 25. Chip-Select Read Cycle Timing Diagram

Table 26. SDHC Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Min	Max	Min	Max	
1	CLK frequency at Data transfer Mode (PP)[1]—10/30 cards	0	25/5	0	25/5	MHz
2	$\overline{\text{CLK}}$ frequency at Identification Mode[2]	0	400	0	400	kHz
3a	Clock high time[1]—10/30 cards	6/33	–	10/50	–	ns
3b	Clock low time[1]—10/30 cards	15/75	–	10/50	–	ns
4a	Clock fall time[1]—10/30 cards	–	10/50 (5.00)[3]	–	10/50	ns
4b	Clock rise time[1]—10/30 cards	–	14/67 (6.67)[3]	–	10/50	ns
5a	Input hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
5b	Input setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6a	Output hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6b	Output setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
7	Output delay time[3]	0	16	0	14	ns

1. $C_L \leq 100$ pF / 250 pF (10/30 cards)
2. $C_L \leq 250$ pF (21 cards)
3. $C_L \leq 25$ pF (1 card)

Table 32. SDRAM Write Cycle Timing Parameter

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	SDRAM clock low-level width	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
4	Address setup time	3.67	–	2	–	ns
5	Address hold time	2.95	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP}[2]	–	ns
7	Active to read/write command delay	t_{RCD}[2]	–	t_{RCD}[2]	–	ns
8	Data setup time	3.41	–	2	–	ns
9	Data hold time	2.45	–	2	–	ns

1. Precharge cycle timing is included in the write timing diagram.
2. t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

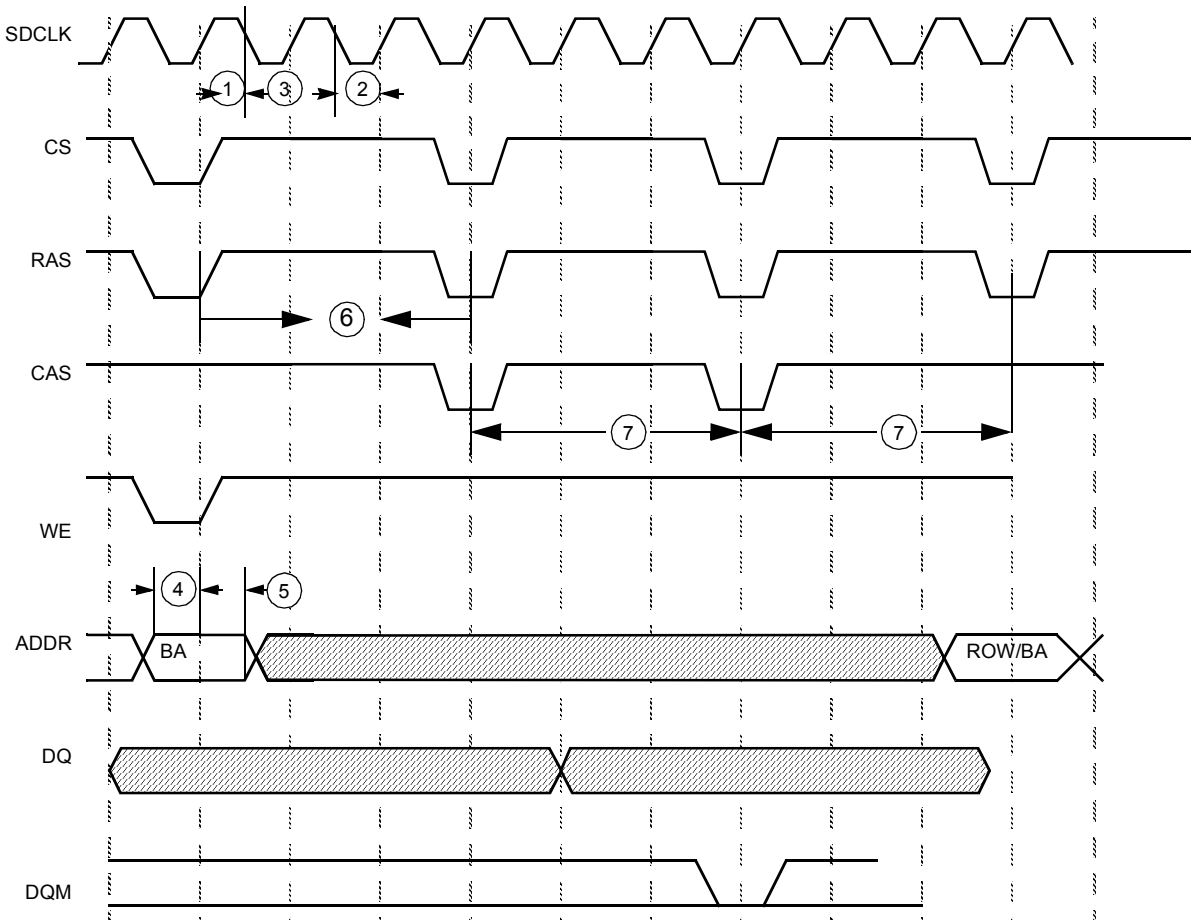


Figure 40. SDRAM Refresh Timing Diagram

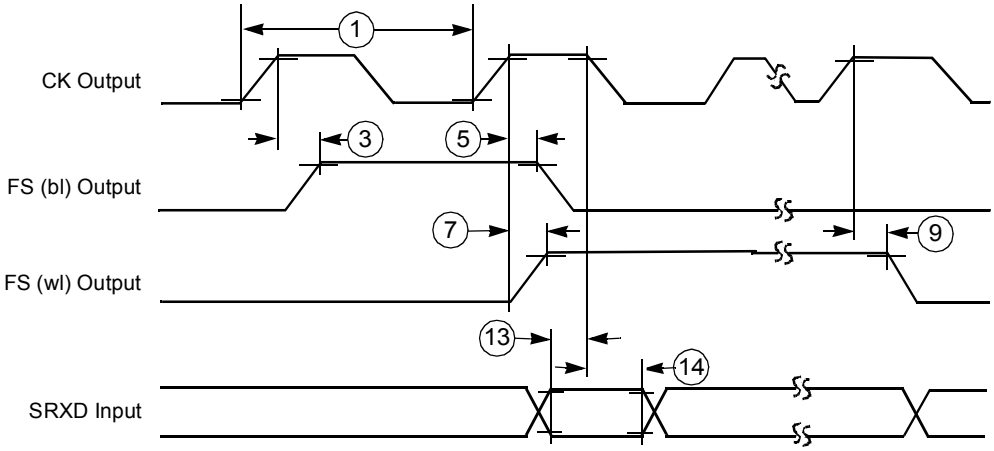
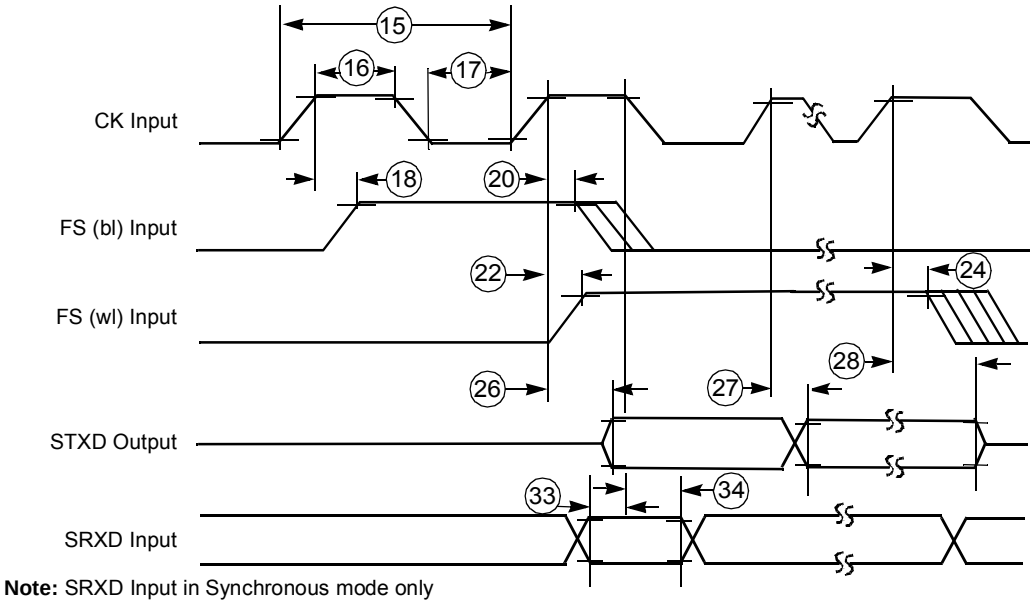


Figure 43. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 44. SSI Transmitter External Clock Timing Diagram

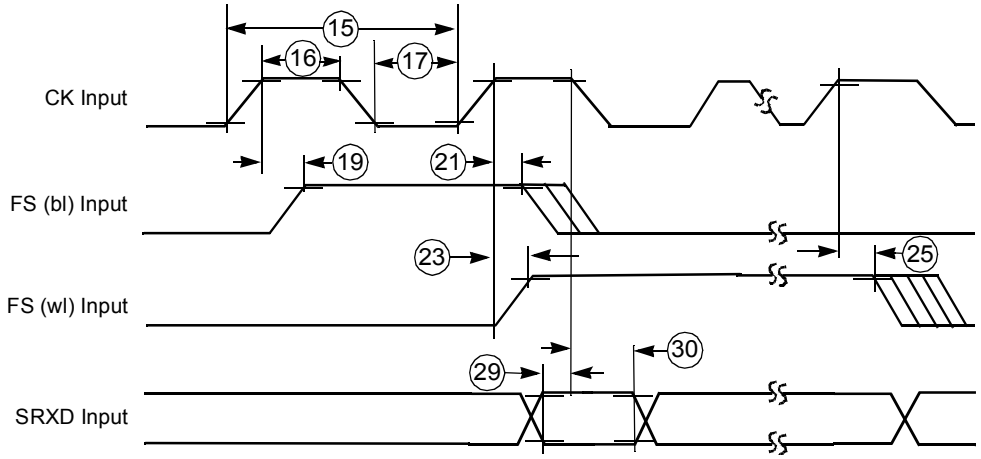


Figure 45. SSI Receiver External Clock Timing Diagram

Table 36. SSI to SSI2 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
11a	(Tx) CK high to STXD high	0.34	0.72	0.34	0.72	ns
11b	(Tx) CK high to STXD low	0.34	0.72	0.34	0.72	ns
12	(Tx) CK high to STXD high impedance	0.34	0.48	0.34	0.48	ns
13	SRXD setup time before (Rx) CK low	21.50	–	21.50	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI2 Ports)						
15	(Tx/Rx) CK clock period[1] 90	.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.40	17.37	8.67	15.88	ns
19	(Rx) CK high to FS (bl) high	11.00	19.70	9.28	18.21	ns
20	(Tx) CK high to FS (bl) low	10.40	17.37	8.67	15.88	ns
21	(Rx) CK high to FS (bl) low	11.00	19.70	9.28	18.21	ns
22	(Tx) CK high to FS (wl) high	10.40	17.37	8.67	15.88	ns
23	(Rx) CK high to FS (wl) high	11.00	19.70	9.28	18.21	ns
24	(Tx) CK high to FS (wl) low	10.40	17.37	8.67	15.88	ns
25	(Rx) CK high to FS (wl) low	11.00	19.70	9.28	18.21	ns
26	(Tx) CK high to STXD valid from high impedance	9.59	17.08	7.86	15.59	ns
27a	(Tx) CK high to STXD high	9.59	17.08	7.86	15.59	ns
27b	(Tx) CK high to STXD low	9.59	17.08	7.86	15.59	ns
28	(Tx) CK high to STXD high impedance	9.59	16.84	7.86	15.35	ns
29	SRXD setup time before (Rx) CK low	2.52	–	2.52	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI2 Ports)						
31	SRXD setup before (Tx) CK falling	20.78	–	20.78	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI2 Ports)						
33	SRXD setup before (Tx) CK falling	4.42	–	4.42	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 37. SSI to SSI3 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	(Tx) CK high to STXD high impedance	9.02	16.46	7.29	14.97	ns
29	SRXD setup time before (Rx) CK low	1.49	–	1.49	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI3 Ports)						
31	SRXD setup before (Tx) CK falling	21.99	–	21.99	–	ns
32	SRXD old fter Txh) Kafalling C	0	–	0	–	ns
Synchronous External Clock Operation (SSI3 Ports)						
33	SRXD setup before (Tx) CK falling	3.80	–	3.80	–	ns
34	SRXD old fter Txh) Kafalling C	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

3.17 1-Wire Interface Timing

3.17.1 Reset Sequence with Reset Pulse Presence Pulse

To begin any communications with the DS2502, it is required that an initialization procedure be issued. A reset pulse must be generated and then a presence pulse must be detected. The minimum reset pulse length is 480 us. The bus master (one-wire) will generate this pulse, then after the DS2502 detects a rising edge on the one-wire bus, it will wait 15-60 us before it will transmit back a presence pulse. The presence pulse will exist for 60-240 us.

The timing diagram for this sequence is shown in Figure 46.

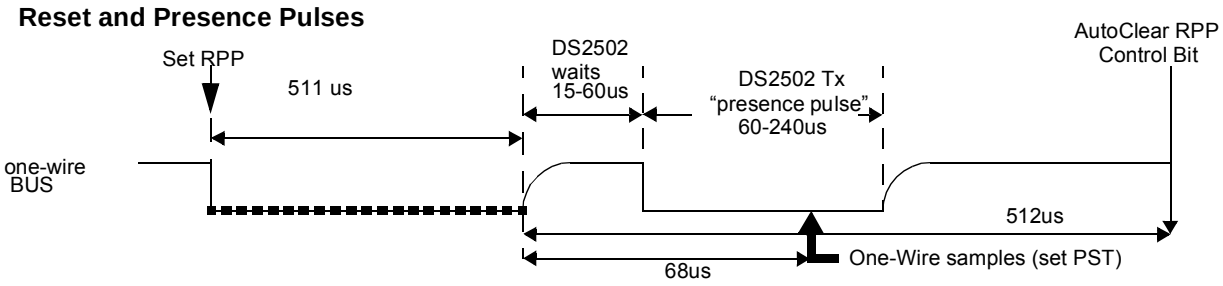


Figure 46. 1-Wire Initialization

The reset pulse begins the initialization sequence and it is initiated when the RPP control register bit is set. When the presence pulse is detected, this bit will be cleared. The presence pulse is used by the bus master to determine if at least one DS2502 is connected. Software will determine if more than one DS2502 exists. The one-wire will sample for the DS2502 presence pulse. The presence pulse is latched in the one-wire

3.18 USB On-The-Go

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, but because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

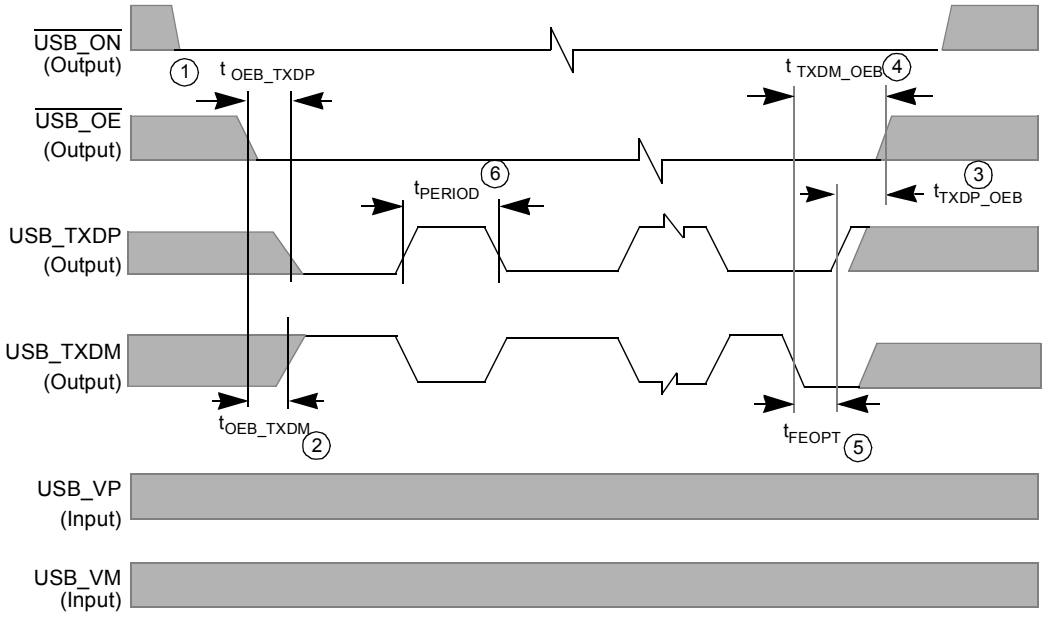


Figure 50. USB Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 40. USB Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{OEB_TXDP}; $\overline{USBD\_OE}$ active to USBD_TXDP low	83.14	83.47	ns
2	t_{OEB_TXDM}; $\overline{USBD\_OE}$ active to USBD_TXDM high	81.55	81.98	ns
3	t_{TXDP_OEB}; USBD_TXDP high to $\overline{USBD\_OE}$ deactivated	83.54	83.8	ns
4	t_{TXDM_OEB}; USBD_TXDM low to $\overline{USBD\_OE}$ deactivated (includes SE0)	248.9	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160	175	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

Note: Signals listed with lower case letters are internal to the device.

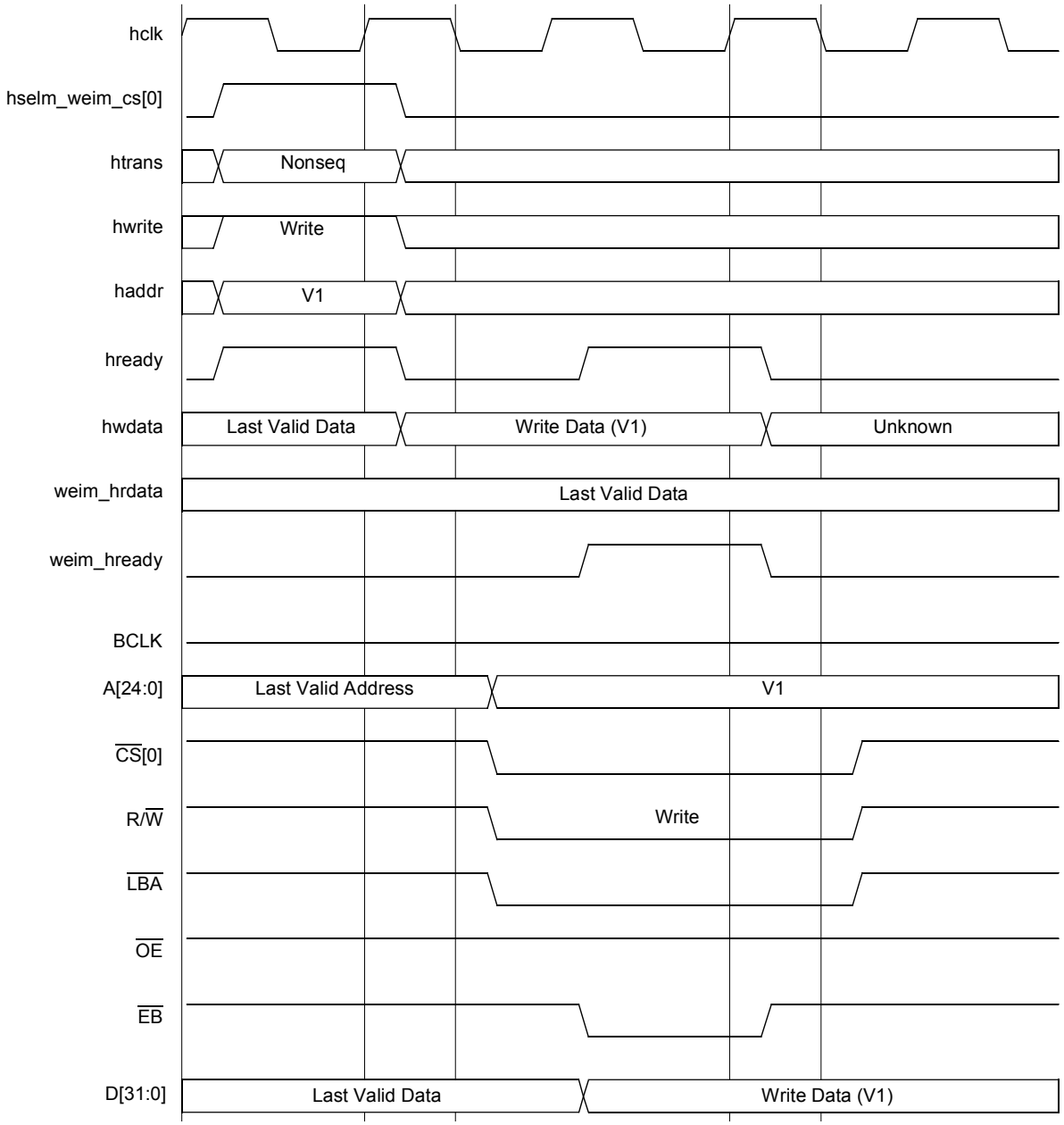


Figure 55. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

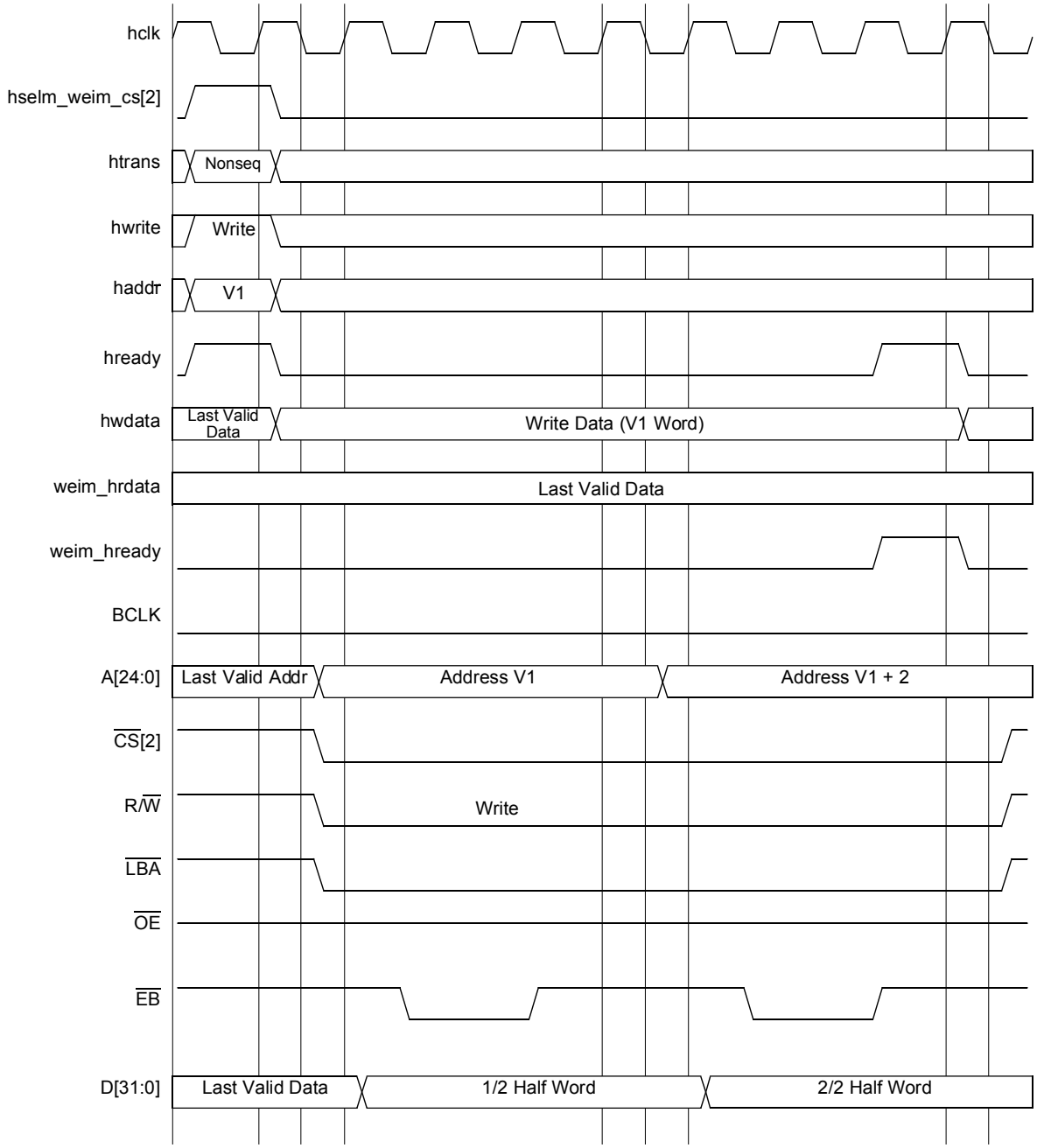


Figure 61. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

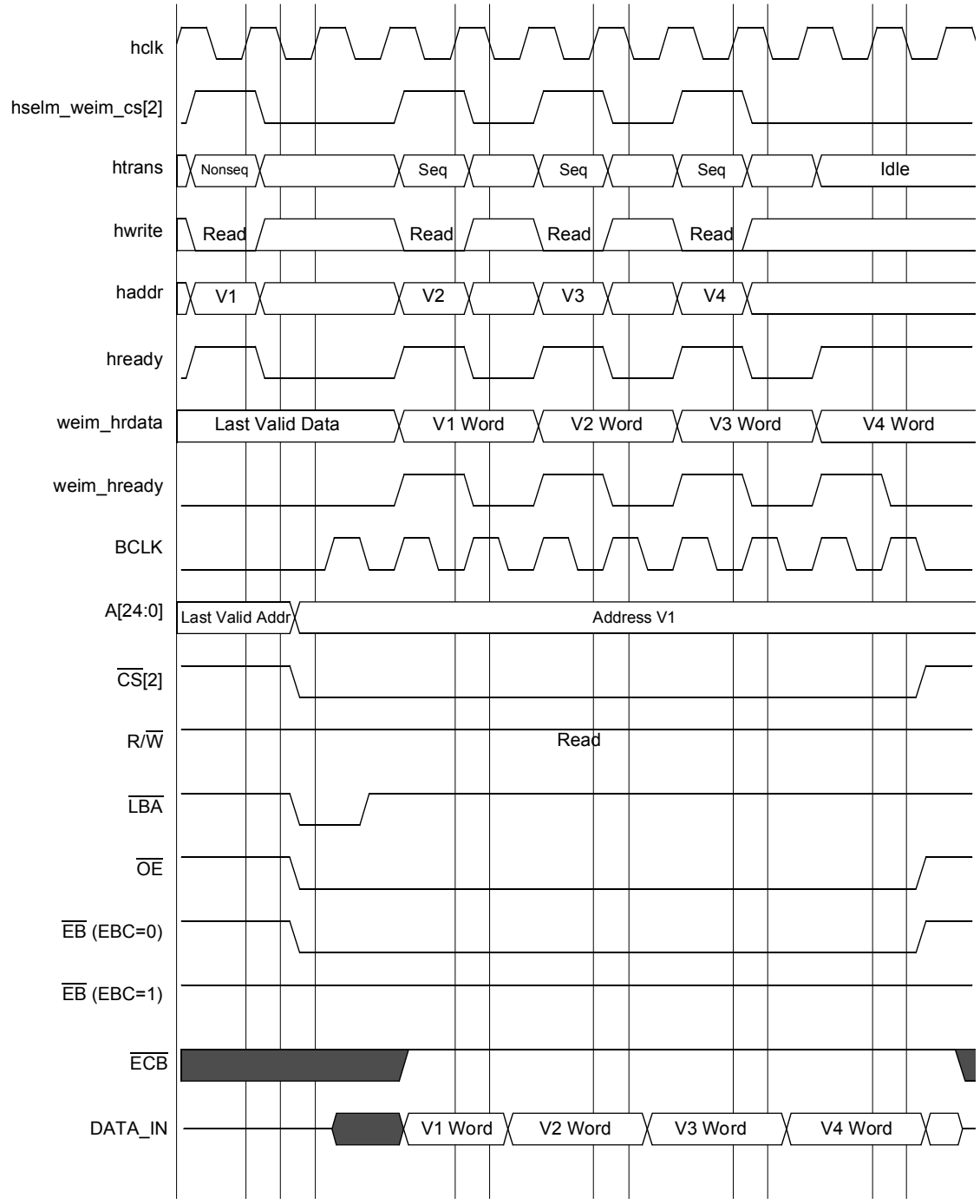


Figure 73. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Note: Signals listed with lower case letters are internal to the device.

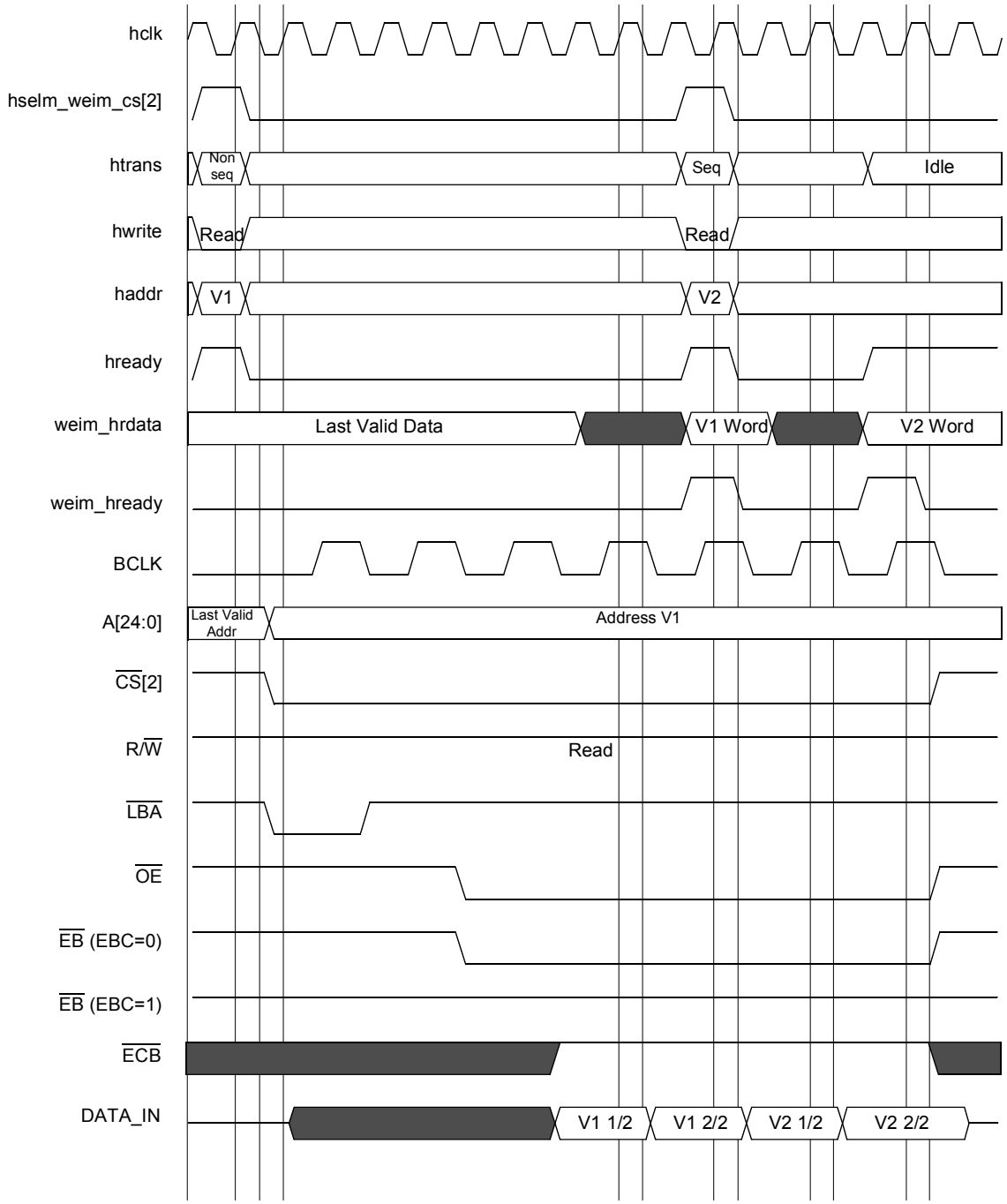


Figure 76. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

3.21 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

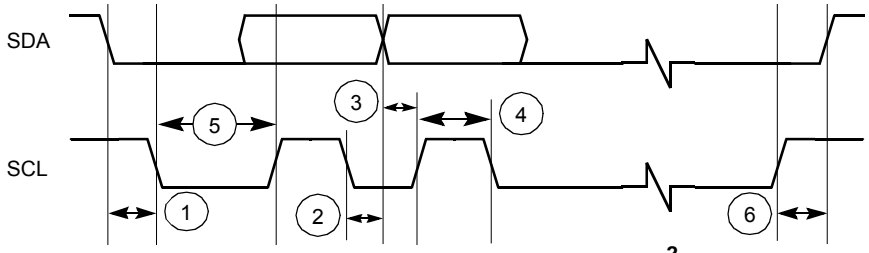


Figure 80. Definition of Bus Timing for I²C

Table 44. I²C Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
	SCL Clock Frequency	0	100	0	100	kHz
1	Hold time (repeated) START condition	114.8	–	111.1	–	ns
2	Data hold time	0	69.7	0	72.3	ns
3	Data setup time	3.1	–	1.76	–	ns
4	HIGH period of the SCL clock	69.7	–	68.3	–	ns
5	LOW period of the SCL clock	336.4	–	335.1	–	ns
6	Setup time for STOP condition	110.5	–	111.1	–	ns

3.22 CMOS Sensor Interface

The CSI module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32 × 32 image data receive FIFO, and a 16 × 32 statistic data FIFO.

3.22.1 Gated Clock Mode

Figure 81 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 82 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 45. The formula for calculating the pixel clock rise and fall time is located in Section 3.22.3, “Calculation of Pixel Clock Rise/ Fall Time.”

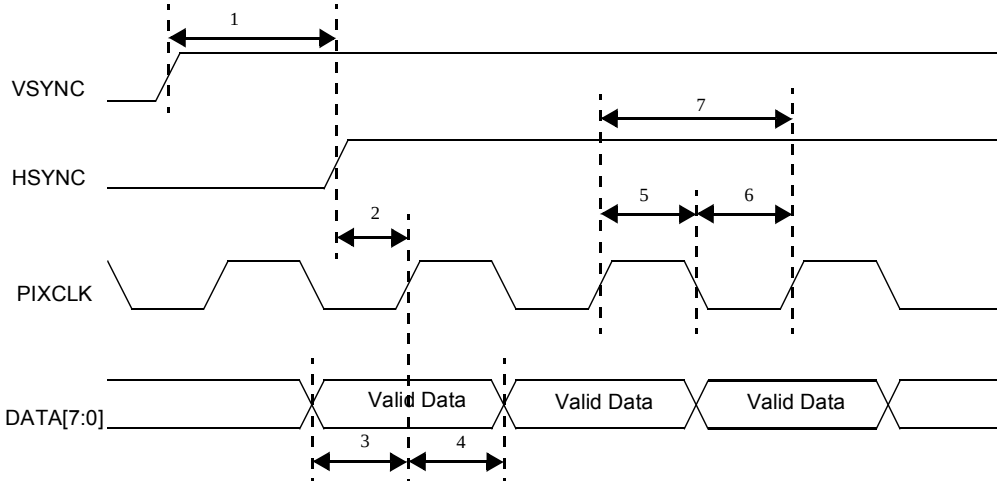


Figure 81. Sensor Output Data on Pixel Clock Falling Edge CSI Latches Data on Pixel Clock Rising Edge

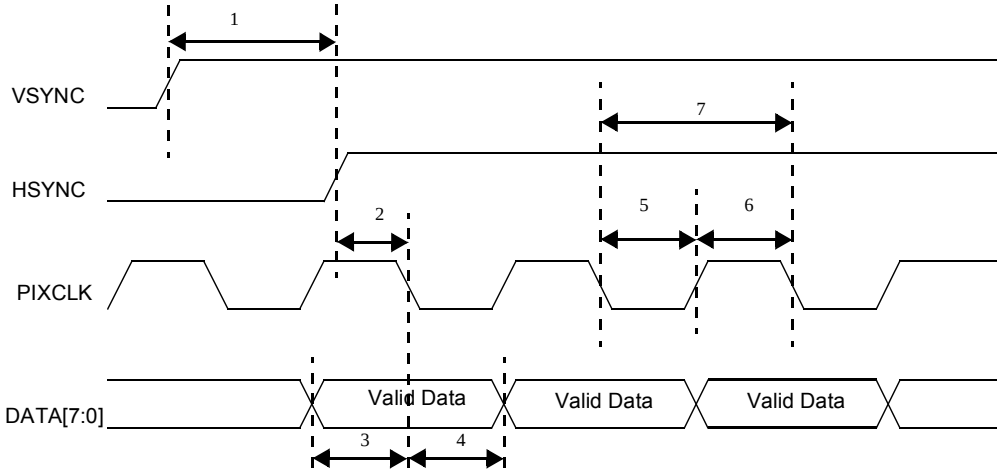


Figure 82. Sensor Output Data on Pixel Clock Rising Edge CSI Latches Data on Pixel Clock Falling Edge

Table 45. Gated Clock Mode Timing Parameters

Number	Parameter	Minimum	Maximum	Unit
1	csi_vsync to csi_hsync	9 * T_{HCLK}	–	ns
2	csi_hsync to csi_pixclk	3	(T_P/2) - 3	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	T_{HCLK}	–	ns
6	csi_pixclk low time	T_{HCLK}	–	ns
7	csi_pixclk frequency	0	HCLK / 2	MHz

HCLK = AHB System Clock, T_{HCLK} = Period for HCLK, T_P = Period of CSI_PIXCLK