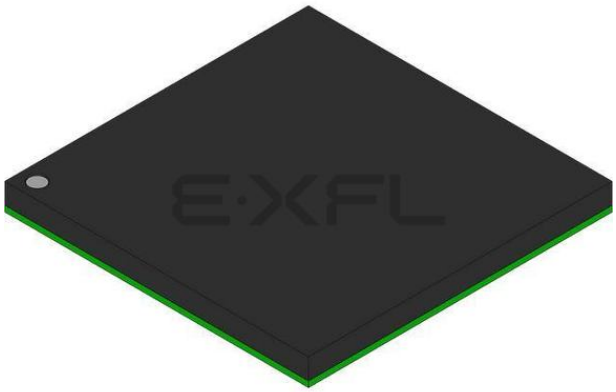

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Details	
Product Status	Active
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Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx21vk

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH2_FS	USB Host2 Full Speed output signal. This signal is multiplexed with CSPI2_SS[0] of CSPI2.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added. This signal is multiplexed with CSPI3_MOSI.
SD1_CLK	SD Output Clock. This signal is multiplexed with CSPI3_SCLK.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART2_RXD	Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP.
UART2_TXD	Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP.
$\overline{\text{UART2\_RTS}}$	Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP.
$\overline{\text{UART2\_CTS}}$	Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP.
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK, VM	T_A	0	70	°C
	DVK, DVM	T_A	-30	70	°C
	CVK, CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V

All timing is measured at 30 pF loading with the exception of fast I/O signals as discussed below. Refer to the reference manual's System Control Chapter for details on drive strength settings.

Table 8 provides the maximum loading guidelines that can be tolerated on a memory I/O signal (also known as Fast I/O) to achieve 133 MHz operation. These critical signals include the SDRAM Clock (SDCLK), Data Bus signals (D[31:0]), lower order address signals such as A0-A10, MA10, MA11, and other signals required to meet 133 MHz timing.

The values shown in Table 8 apply over the recommended operating temperature range. Care must be taken to minimize parasitic capacitance of associated printed circuit board traces.

Table 8. Loading Guidelines for Fast IO Signals to Achieve 133 MHz Operation

Drive Strength Setting (DSCR2–DSCR12)	Maximum I/O Loading at 1.8 V	Maximum I/O Loading at 3.0 V
000: 3.5 mA	9 pF	12 pF
001: 4.5 mA	12 pF	16 pF
011: 5.5 mA	15 pF	21 pF
111: 6.5 mA	19 pF	26 pF

Table 9. 32k/26M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak) for both System PLL and MCUPLL	–	5	20	ns
EXTAL32k input jitter (peak to peak) for MCUPLL only	–	5	100	ns
EXTAL32k startup time	800	–	–	ms

Table 10. CLKO Rise/Fall Time (at 30pF Loaded)

	Best Case	Typical	Worst Case	Units
Rise Time	0.80	1.00	1.40	ns
Fall Time	0.74	1.08	1.67	ns

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–

The output External Grant signal from the DMAC is an active-low signal.When the following conditions are true, the External DMA Grant signal is asserted with the initiation of the DMA burst.

- The DMA channel for which the DMA burst is ongoing has request source as external DMA Request
  (as per source select register setting).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

After the grant is asserted, the External DMA request will not be sampled until completion of the DMA burst. As the external request is synchronized, the request synchronization will not be done during this period. The priority of the external request becomes low for the next consecutive burst, if another DMA request signal is asserted.

Worst case—that is, the smallest burst (1 byte read/write) timing diagrams are shown in Figure 4 and Figure 5. Minimum and maximum timings for the External request and External grant signals are present in Table 13.

Figure 4 shows the minimum time for which the External Grant signal remains asserted when an External DMA request is de-asserted immediately after sensing grant signal active.

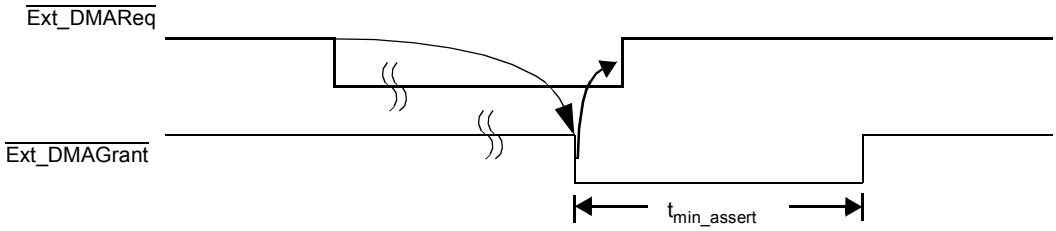
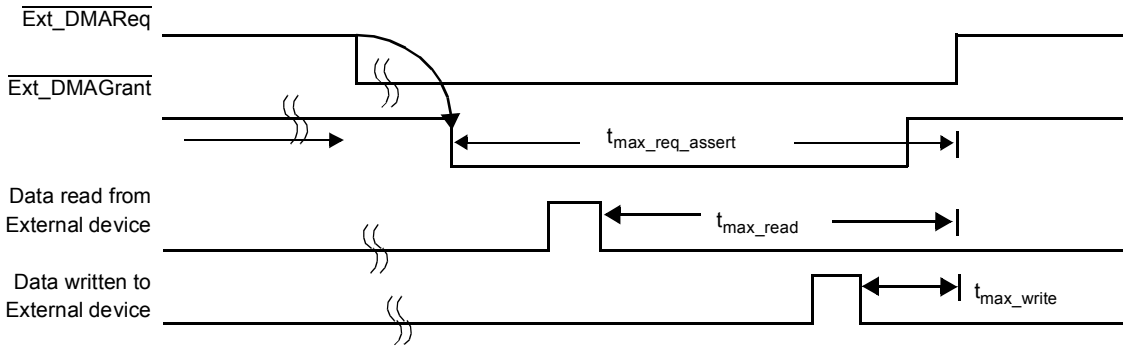


Figure 4. Assertion of DMA External Grant Signal

Figure 5 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.



NOTE: Assuming in worst case the data is read/written from/to External device as per the above waveform.

Figure 5. Safe Maximum Timings for External Request De-Assertion

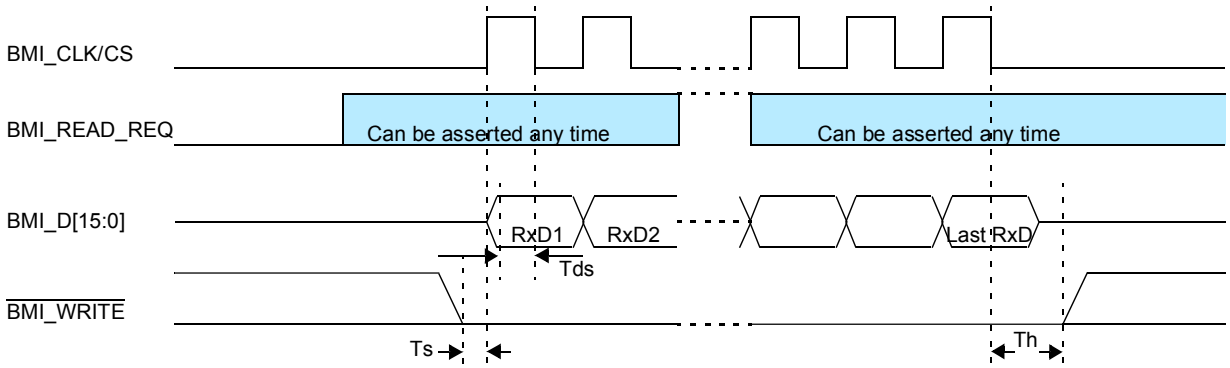


Figure 7. MMD (ATI) Drives Clock, MMD Write BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0, MMD_CLKOUT=0)

Table 15. MMD Write BMI Timing

Item	Symbol	Minimum	Typical	Maximum	Unit
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
$\overline{\text{write}}$ old ime h t	Th	0	–	–	ns
receive data setup time	Tds	5	–	–	ns

Note: All timings assume that the hclk is running at 133 MHz.

Note: At this mode, the maximum frequency of the BMI_CLK/CS can be up to 36 MHz (doubles as maximum data pad speed).

3.8.1.2 BMI Drives the BMI_CLK/CS

In this mode MMD_MODE_SEL and MMD_CLKOUT are both set. The software must know which mode it is now (READ or WRITE). When the $\overline{\text{BMI\_WRITE}}$ is high, BMI drives BMI_CLK/CS out if the TxFIFO is not emptied. When $\overline{\text{BMI\_WRITE}}$ is low, user can write a 1 to READ bit of control register1 to issue a write cycle (MMD write BMI).

3.8.1.3 MMD Read BMI Timing

Figure 13 shows the MMD read BMI timing when BMI drives the BMI_CLK/CS. When the $\overline{\text{BMI\_WRITE}}$ is high, the BMI drives BMI_CLK/CS out if data is written to TxFIFO (BMI_READ_REQ become high), BMI puts data into data bus and enable data out on the rising edge of BMI_CLK/CS. The MMD devices can latch the data on each falling edge of BMI_CLK/CS.

It is recommended that the MMD do not change the $\overline{\text{BMI\_WRITE}}$ signal from high to low when the BMI_READ_REQ is asserted. If user writes data to the TxFIFO when the $\overline{\text{BMI\_WRITE}}$ is low, the BMI will drive BMI_CLK/CS out once the $\overline{\text{BMI\_WRITE}}$ is changed from low to high.

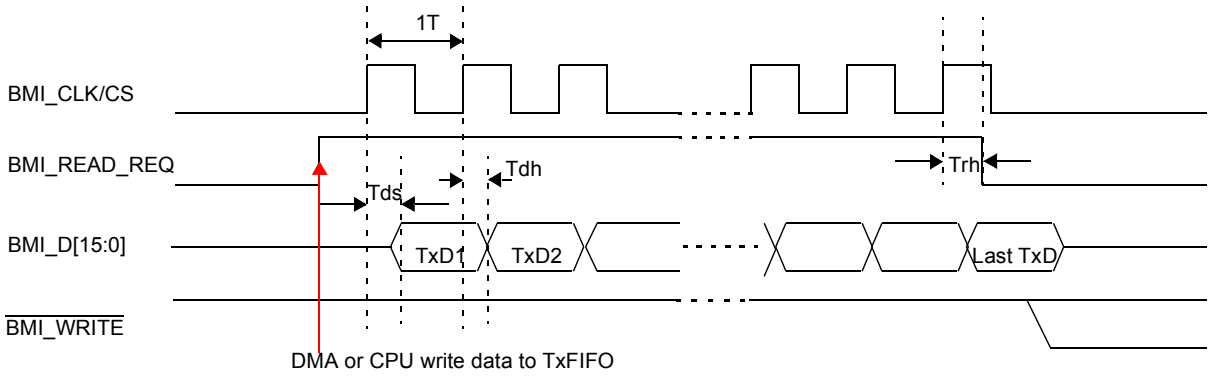


Figure 8. BMI Drives Clock, MMD Read BMI Timing (MASTER_MODE_SEL=0, MMD_MODE_SEL=1, MMD_CLKOUT=1)

Table 16. MMD Read BMI Timing Table when BMI Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Transfer data setup time	Tds	2	–	8	ns
Transfer data hold time	Tdh	2	–	8	ns
Read_req hold time	Trh	2	–	18	ns

Note: In this mode, the max frequency of the BMI_CLK/CS can be up to 36MHz (double as max data pad speed).

Note: The BMI_CLK/CS can only be divided by 2,4,8,16 from HCLK.

3.8.1.4 MMD Write BMI Timing

Figure 9 shows the MMD write BMI timing when BMI drives BMI_CLK/CS.

When the $\overline{\text{BMI\_WRITE}}$ signal is asserted, the BMI can write a 1 to READ bit of control register to issue a WRITE cycle. This bit is cleared automatically when the WRITE operation is completed. In a WRITE burst the MMD will write COUNT+1 data to the BMI. The user can issue another WRITE operation if the MMD still has data to write after the first operation completed.

The BMI can latch the data either at falling edge or the next rising edge of the BMI_CLK/CS according to the DATA_LATCH bit. When the DATA_LATCH bit is set, the BMI latch data at the next rising edge and latch the last data using the internal clock.

$\overline{\text{BMI\_WRITE}}$ signal can not be negated when the WRITE operation is proceeding.

3.11 Smart LCD Controller

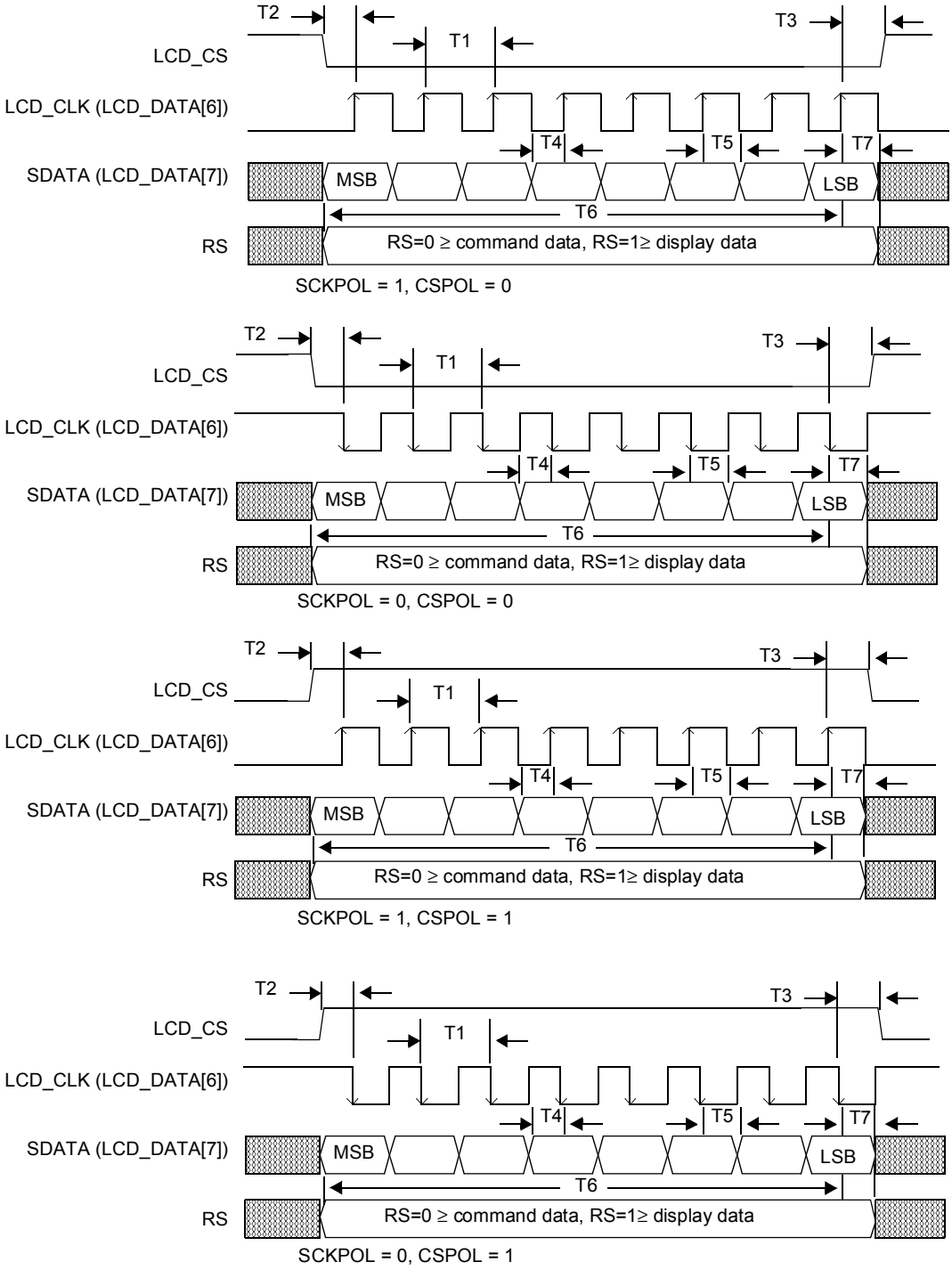


Figure 23. SLCDC Serial Transfer Timing

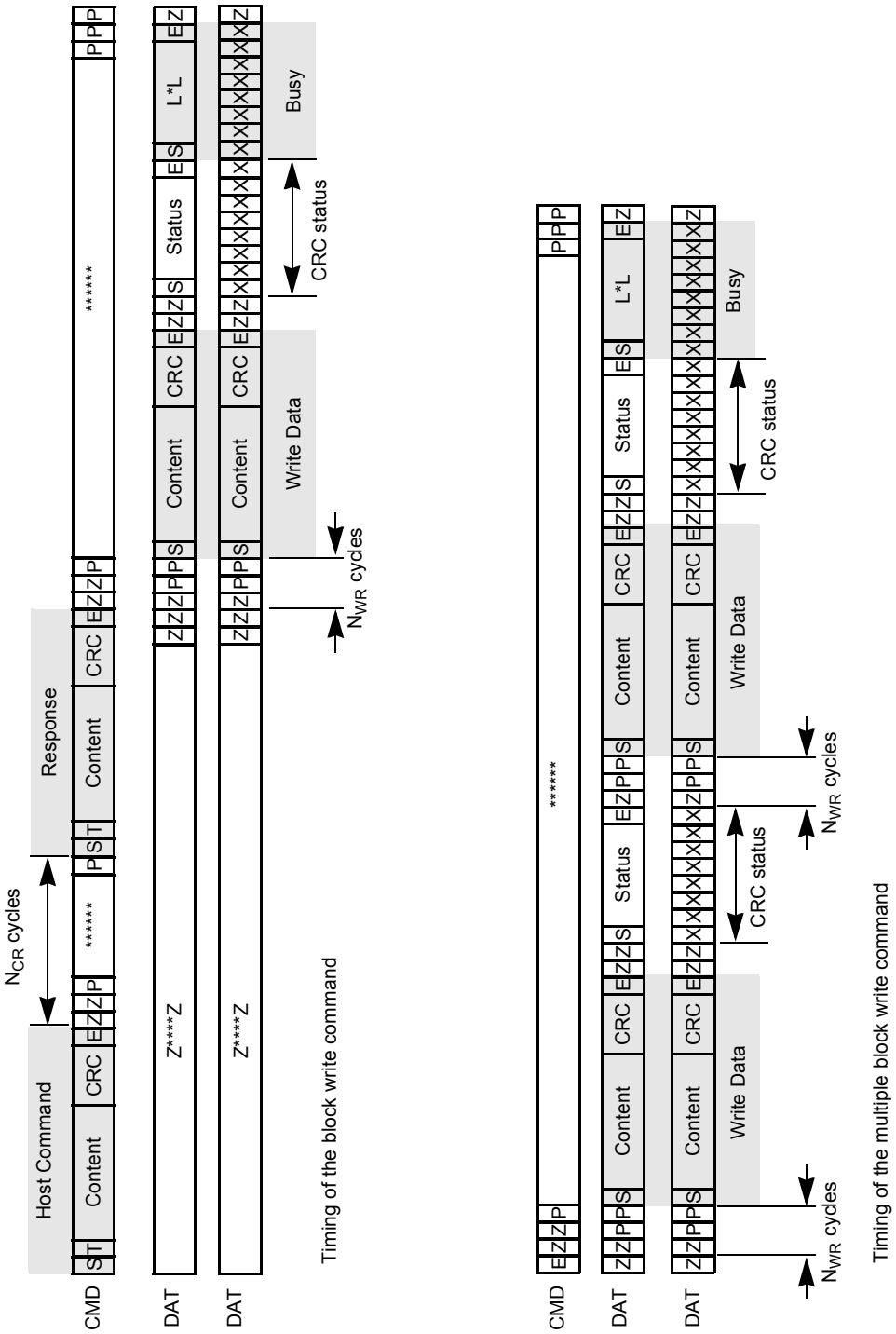


Figure 29. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 30 shows the different scenarios on the bus.

Table 28. Timing Values for Figure 26 through Figure 30 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]				

3.12.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the *Interrupt Period* during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

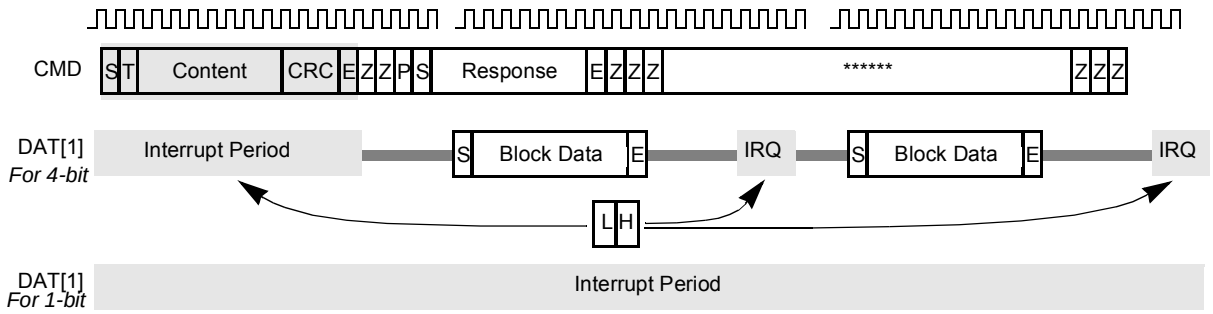


Figure 31. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

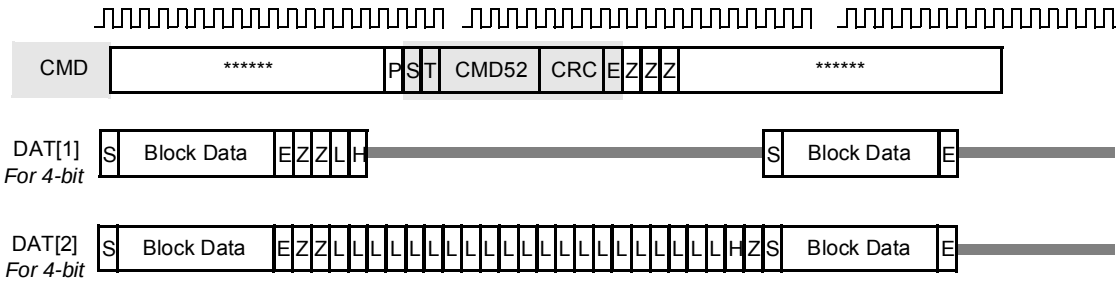


Figure 32. SDIO ReadWait Timing Diagram

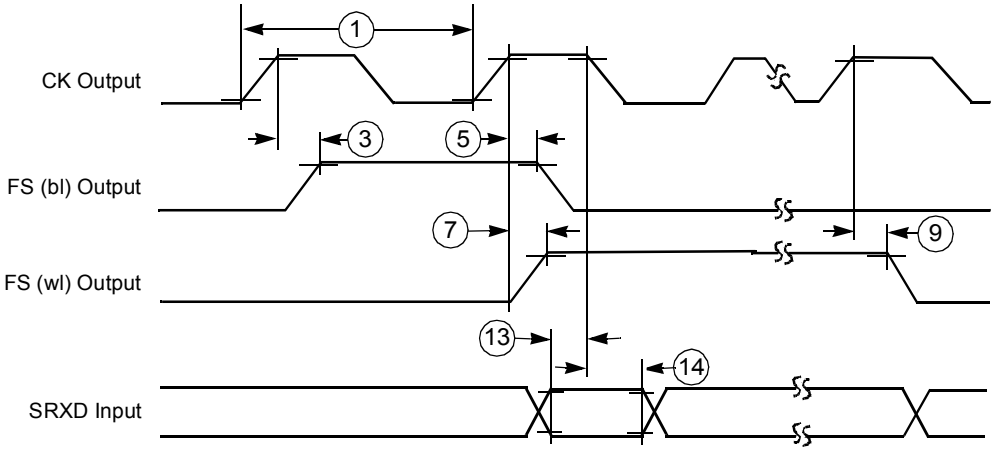
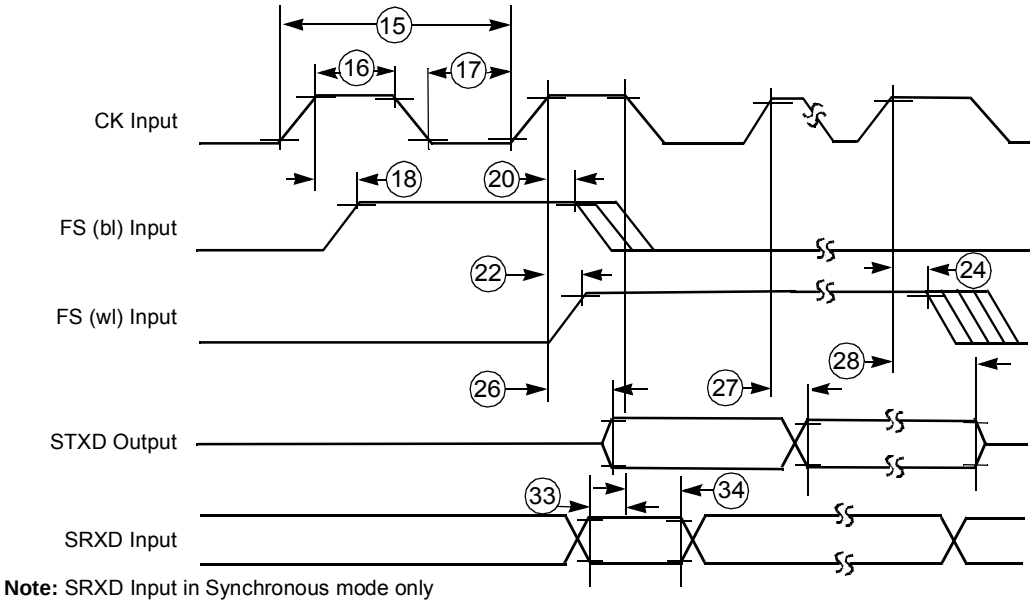


Figure 43. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 44. SSI Transmitter External Clock Timing Diagram

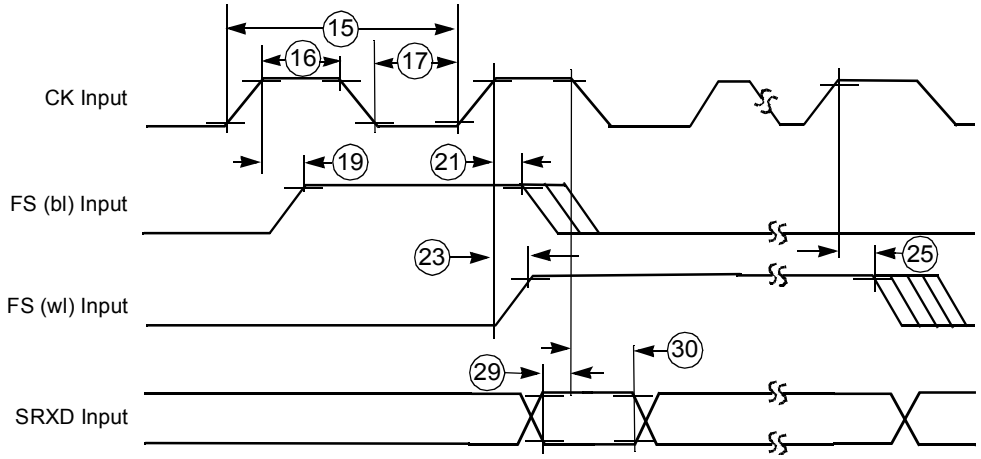


Figure 45. SSI Receiver External Clock Timing Diagram

Table 34. SSI to SAP Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SAP Ports)						
1	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-3.30	-1.16	-2.98	-1.10	ns
3	(Rx) CK high to FS (bl) high	-3.93	-1.34	-4.18	-1.43	ns
4	(Tx) CK high to FS (bl) low	-3.30	-1.16	-2.98	-1.10	ns
5	(Rx) CK high to FS (bl) low	-3.93	-1.34	-4.18	-1.43	ns
6	(Tx) CK high to FS (wl) high	-3.30	-1.16	-2.98	-1.10	ns
7	(Rx) CK high to FS (wl) high	-3.93	-1.34	-4.18	-1.43	ns
8	(Tx) CK high to FS (wl) low	-3.30	-1.16	-2.98	-1.10	ns
9	(Rx) CK high to FS (wl) low	-3.93	-1.34	-4.18	-1.43	ns
10	(Tx) CK high to STXD valid from high impedance	-2.44	-0.60	-2.65	-0.98	ns
11a	(Tx) CK high to STXD high	-2.44	-0.60	-2.65	-0.98	ns
11b	(Tx) CK high to STXD low	-2.44	-0.60	-2.65	-0.98	ns
12	(Tx) CK high to STXD high impedance	-2.67	-0.99	-2.65	-0.98	ns
13	SRXD setup time before (Rx) CK low	23.68	–	22.09	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SAP Ports)						
15	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.24	19.50	7.16	8.65	ns
19	(Rx) CK high to FS (bl) high	10.89	21.27	7.63	9.12	ns
20	(Tx) CK high to FS (bl) low	10.24	19.50	7.16	8.65	ns
21	(Rx) CK high to FS (bl) low	10.89	21.27	7.63	9.12	ns
22	(Tx) CK high to FS (wl) high	10.24	19.50	7.16	8.65	ns
23	(Rx) CK high to FS (wl) high	10.89	21.27	7.63	9.12	ns
24	(Tx) CK high to FS (wl) low	10.24	19.50	7.16	8.65	ns
25	(Rx) CK high to FS (wl) low	10.89	21.27	7.63	9.12	ns
26	(Tx) CK high to STXD valid from high impedance	12.08	19.36	7.71	9.20	ns
27a	(Tx) CK high to STXD high	10.80	19.36	7.71	9.20	ns
27b	(Tx) CK high to STXD low	10.80	19.36	7.71	9.20	ns
28	(Tx) CK high to STXD high impedance	12.08	19.36	7.71	9.20	ns
29	SRXD setup time before (Rx) CK low	0.37	–	0.42	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns

Table 43. EIM Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V			1.8 V ± 0.1 V	Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	3.97	6.02	9.89	3.83	5.89	9.79	ns
1b	Clock fall to address invalid	3.93	6.00	9.86	3.81	5.86	9.76	ns
2a	Clock fall to chip-select valid	3.47	5.59	8.62	3.30	5.09	8.45	ns
2b	Clock fall to chip-select invalid	3.39	5.09	8.27	3.15	4.85	8.03	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	3.51	5.56	8.79	3.39	5.39	8.51	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	3.59	5.37	9.14	3.36	5.20	8.50	ns
4a	Clock[1] rise to Output Enable Valid	3.62	5.49	8.98	3.46	5.33	9.02	ns
4b	Clock[1] rise to Output Enable Invalid	3.70	5.61	9.26	3.46	5.37	8.81	ns
4c	Clock[1] fall to Output Enable Valid	3.60	5.48	8.77	3.44	5.30	8.88	ns
4d	Clock[1] fall to Output Enable Invalid	3.69	5.62	9.12	3.42	5.36	8.60	ns
5a	Clock[1] rise to Enable Bytes Valid	3.69	5.46	8.71	3.46	5.25	8.54	ns
5b	Clock[1] rise to Enable Bytes Invalid	4.64	5.47	8.70	3.46	5.25	8.54	ns
5c	Clock[1] fall to Enable Bytes Valid	3.52	5.06	8.39	3.41	5.18	8.36	ns
5d	Clock[1] fall to Enable Bytes Invalid	3.50	5.05	8.27	3.41	5.18	8.36	ns
6a	Clock[1] fall to Load Burst Address Valid	3.65	5.28	8.69	3.30	5.23	8.81	ns
6b	Clock[1] fall to Load Burst Address Invalid	3.65	5.67	9.36	3.41	5.43	9.13	ns
6c	Clock[1] rise to Load Burst Address Invalid	3.66	5.69	9.48	3.33	5.47	9.25	ns
7a	Clock[1] rise to Burst Clock rise	3.50	5.22	8.42	3.26	4.99	8.19	ns
7b	Clock[1]rise to Burst Clock fall	3.49	5.19	8.30	3.31	5.03	8.17	ns
7c	Clock[1] fall to Burst Clock rise	3.50	5.22	8.39	3.26	4.98	8.15	ns
7d	Clock[1] fall to Burst Clock fall	3.49	5.19	8.29	3.31	5.02	8.12	ns
8a	Read Data setup time	4.54	–	–	4.54	–	–	ns
8b	Read Data hold time	0.5	–	–	0.5	–	–	ns
9a	Clock[1] rise to Write Data Valid	4.13	5.86	9.16	3.95	6.36	10.31	ns
9b	Clock[1] fall to Write Data Invalid	4.10	5.79	9.15	4.04	6.27	9.16	ns
9c	Clock[1] rise to Write Data Invalid	4.02	5.81	9.37	4.22	5.29	9.24	ns
10a	DTACK setup time	2.65	4.63	8.40	2.64	4.61	8.41	ns
11	Burst Clock (BCLK) cycle time	15	–	–	15	–	–	ns

1. Clock refers to the system clock signal, HCLK, generated from the System DPLL

3.19.1 EIM External Bus Timing Diagrams

The following timing diagrams show the timing of accesses to memory or a peripheral.

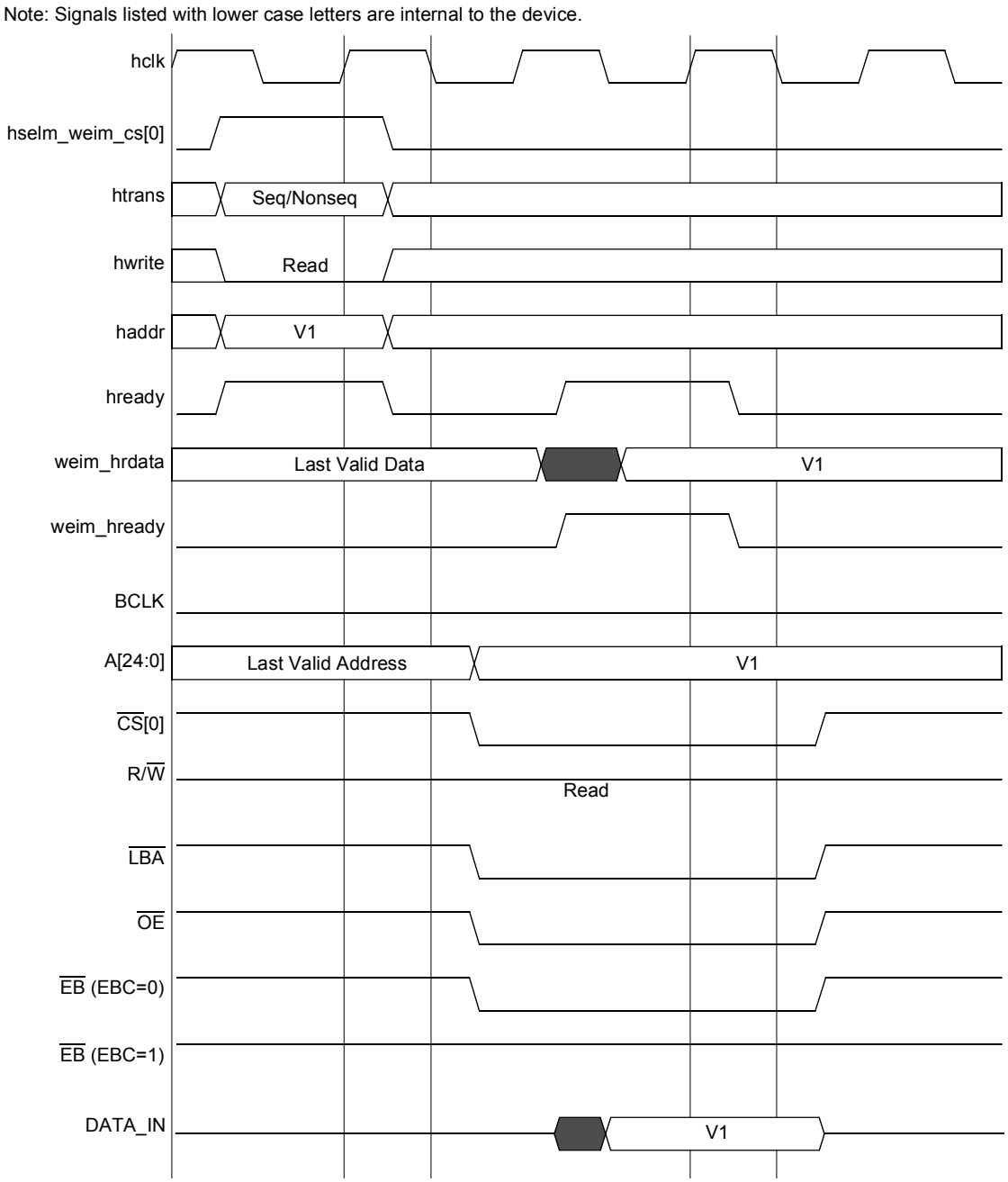


Figure 54. WSC = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

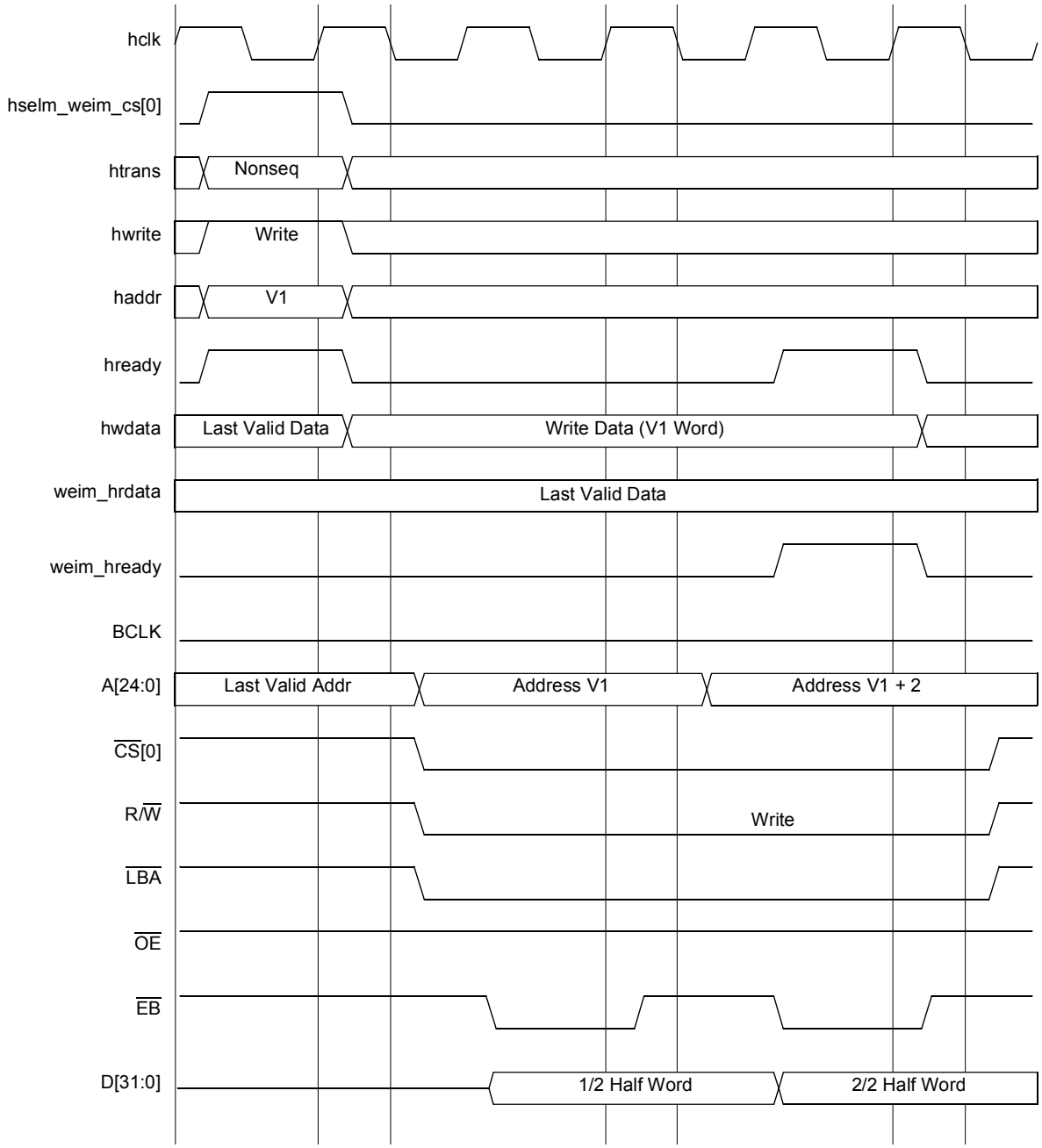


Figure 57. WSC = 1, WEA = 1, WEN = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

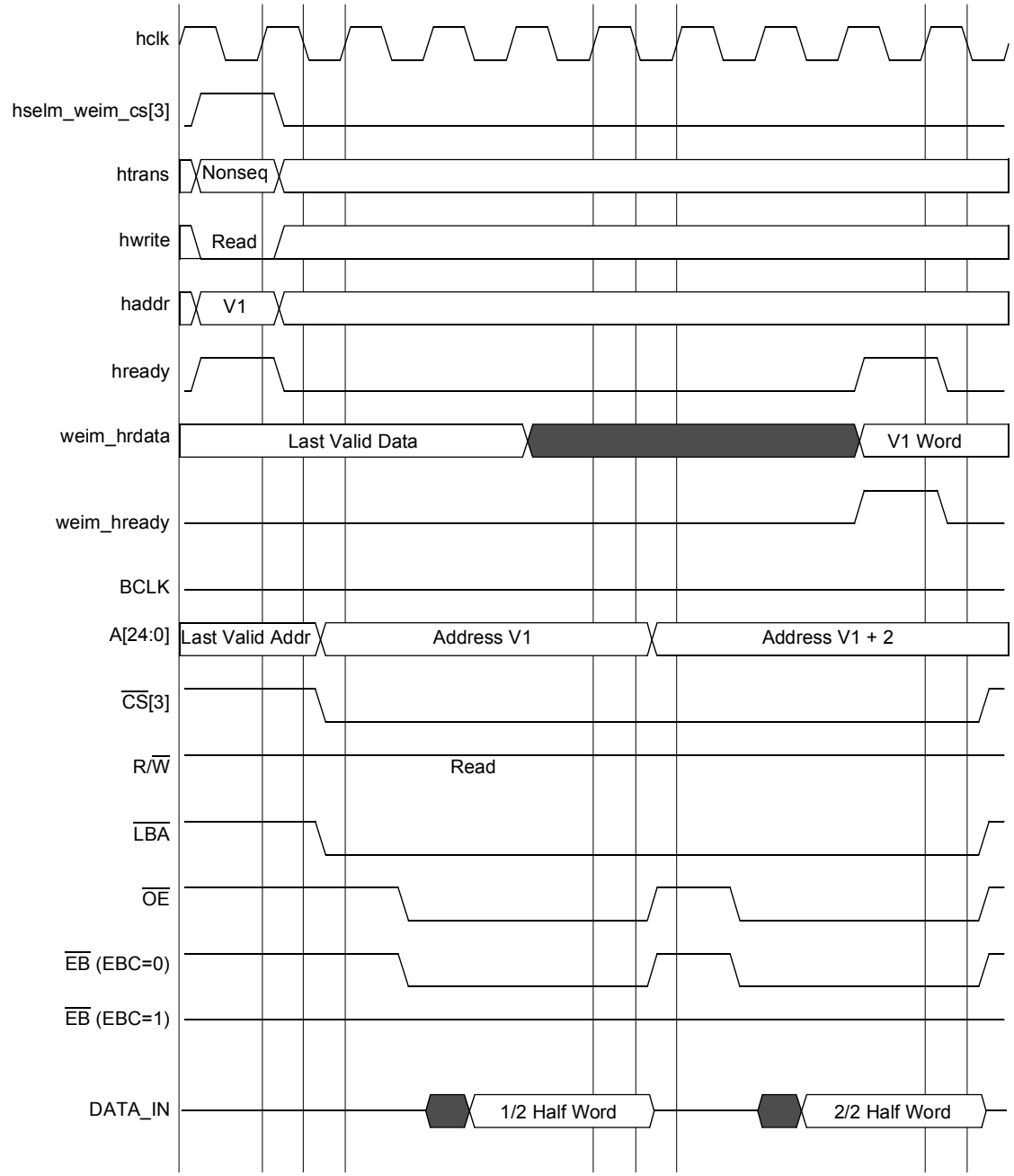


Figure 58. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

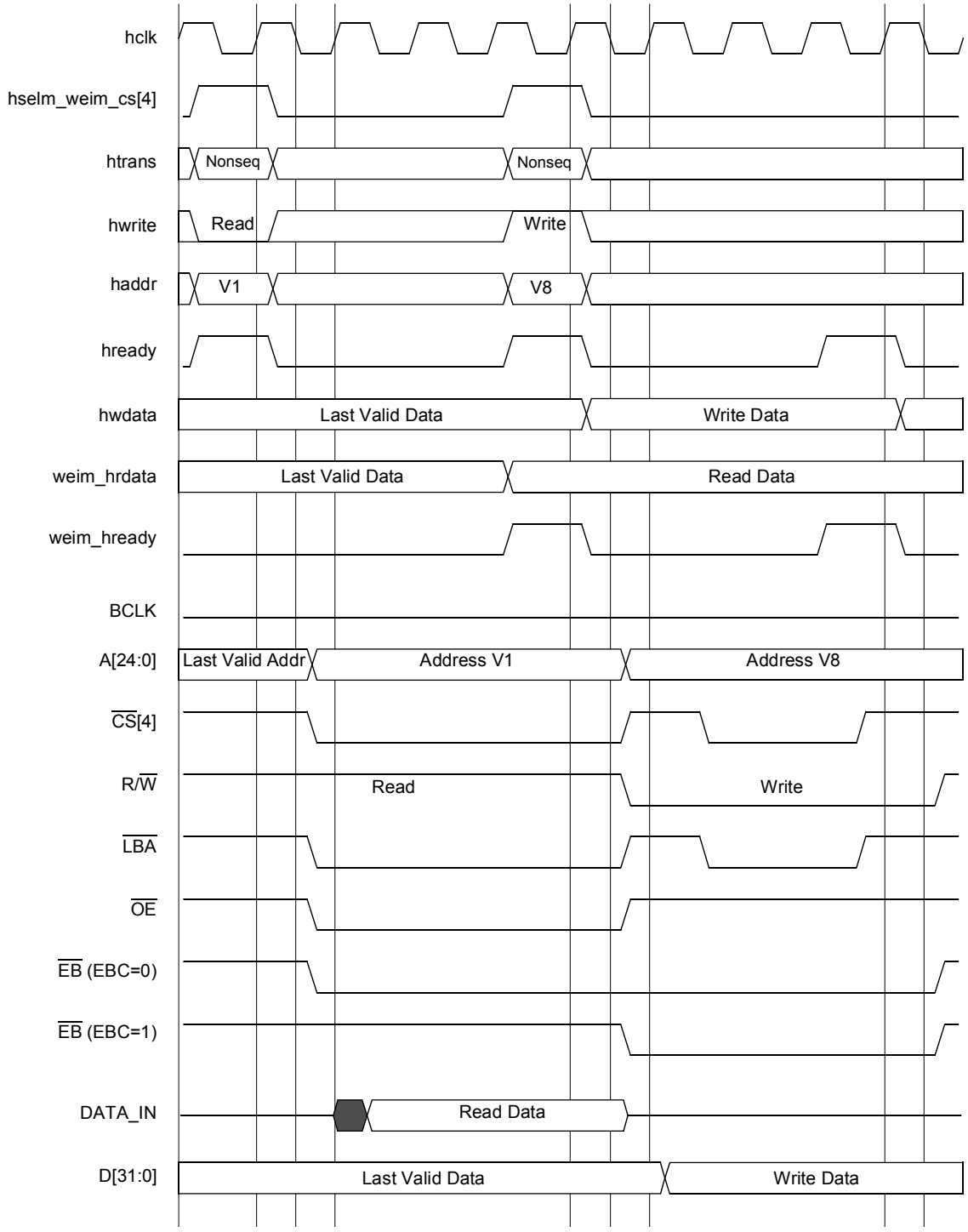


Figure 69. WSC = 3, CSA = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

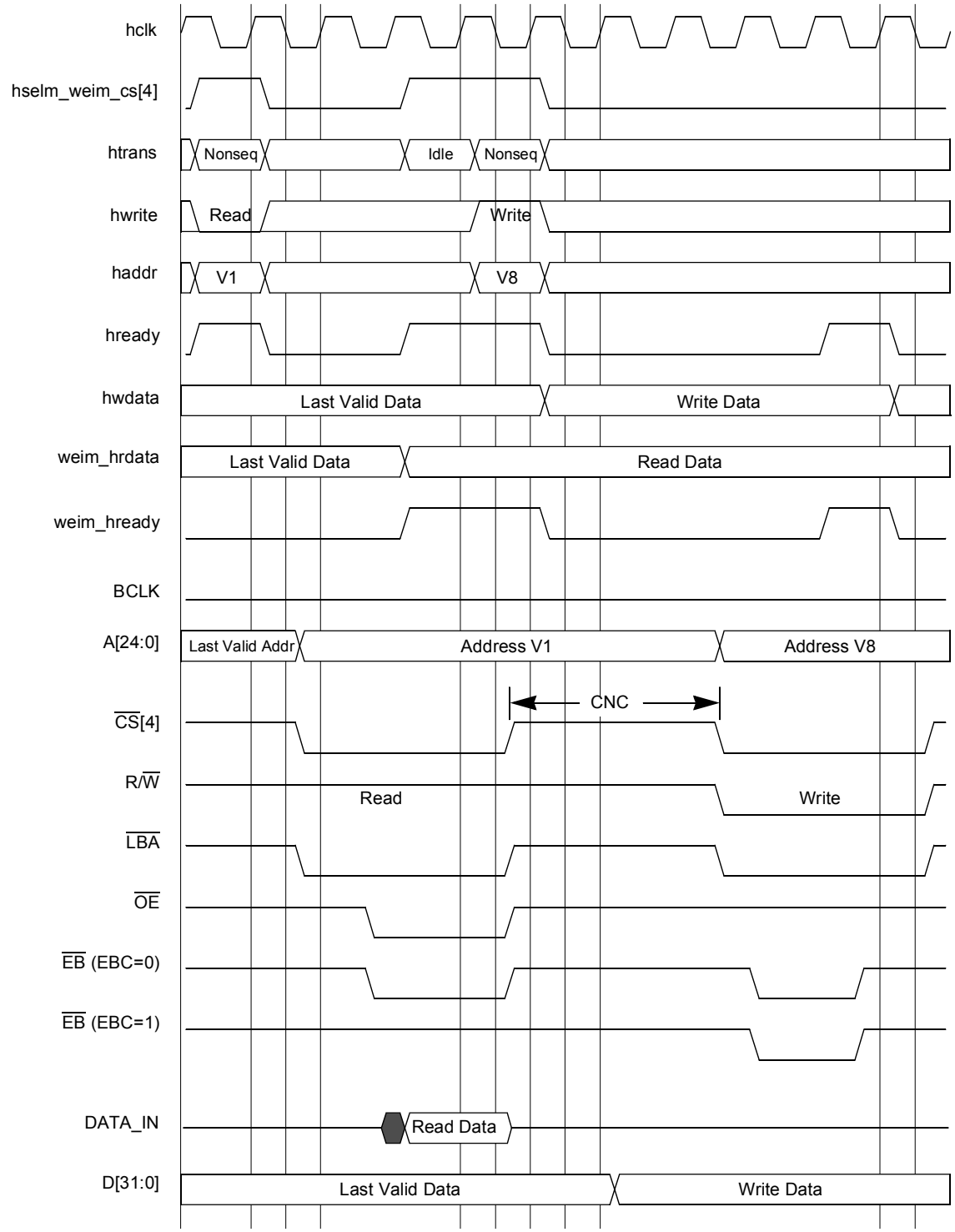


Figure 71. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

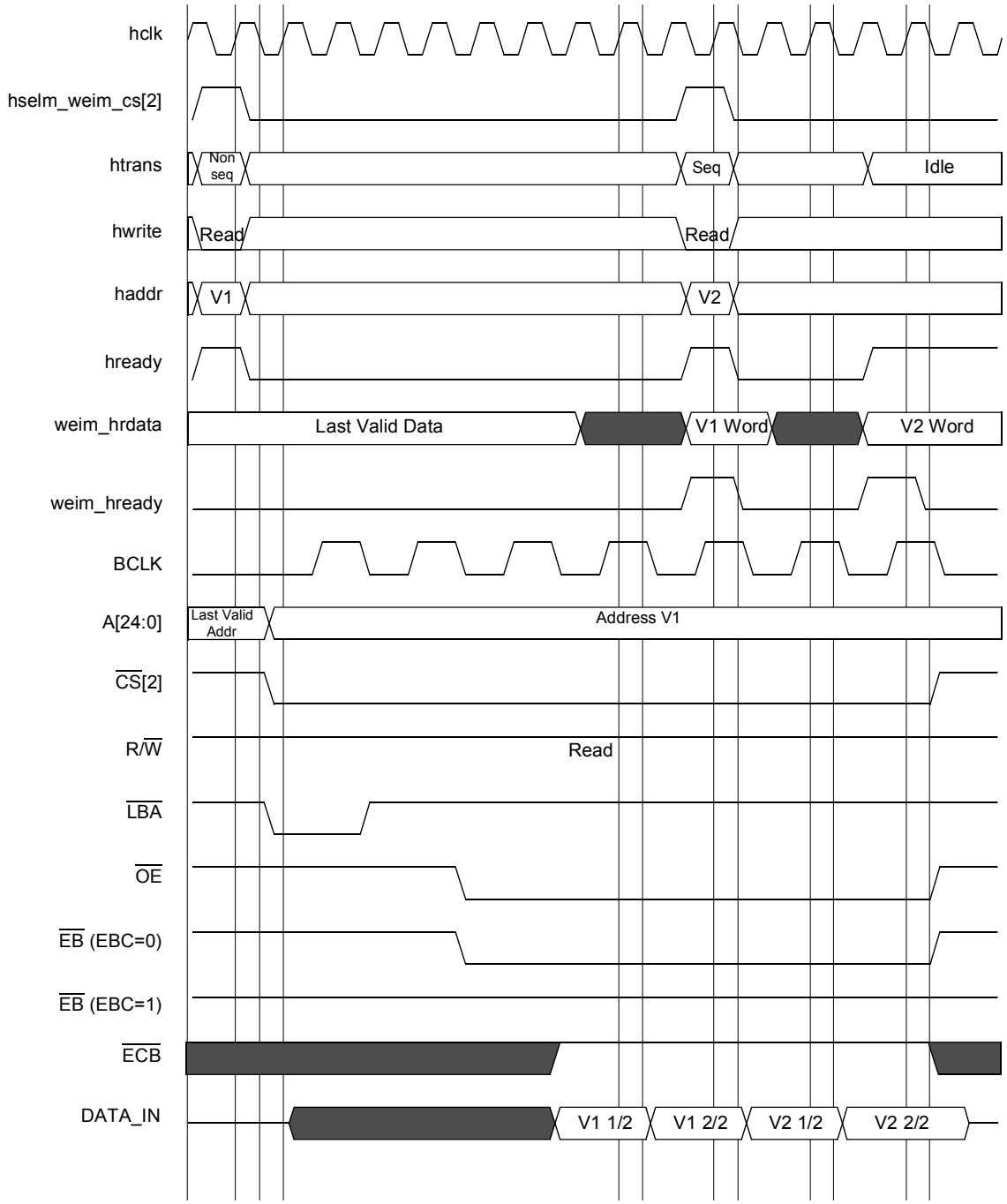


Figure 76. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

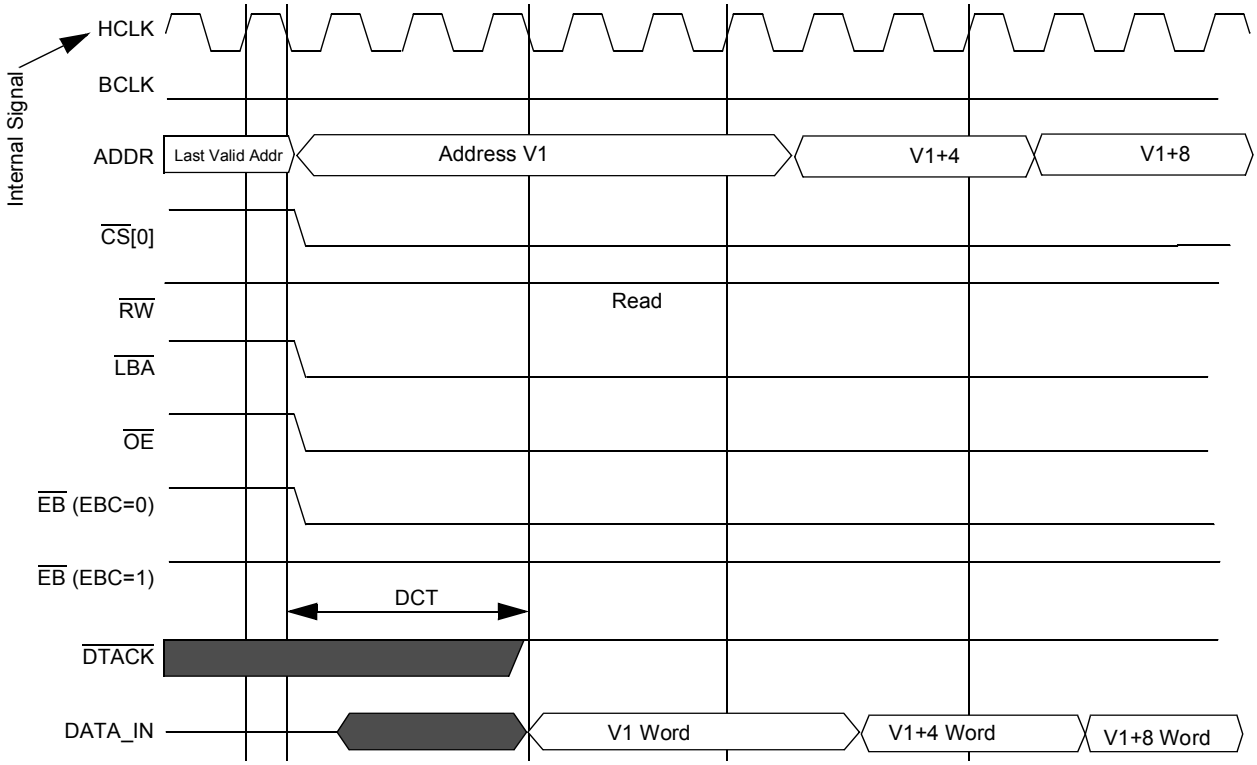


Figure 78. DTACK Level Sensitive Sequential Read Accesses, WSC=2, EW=1, DCT=1, AGE=0 (Example of DTACK Remaining High)

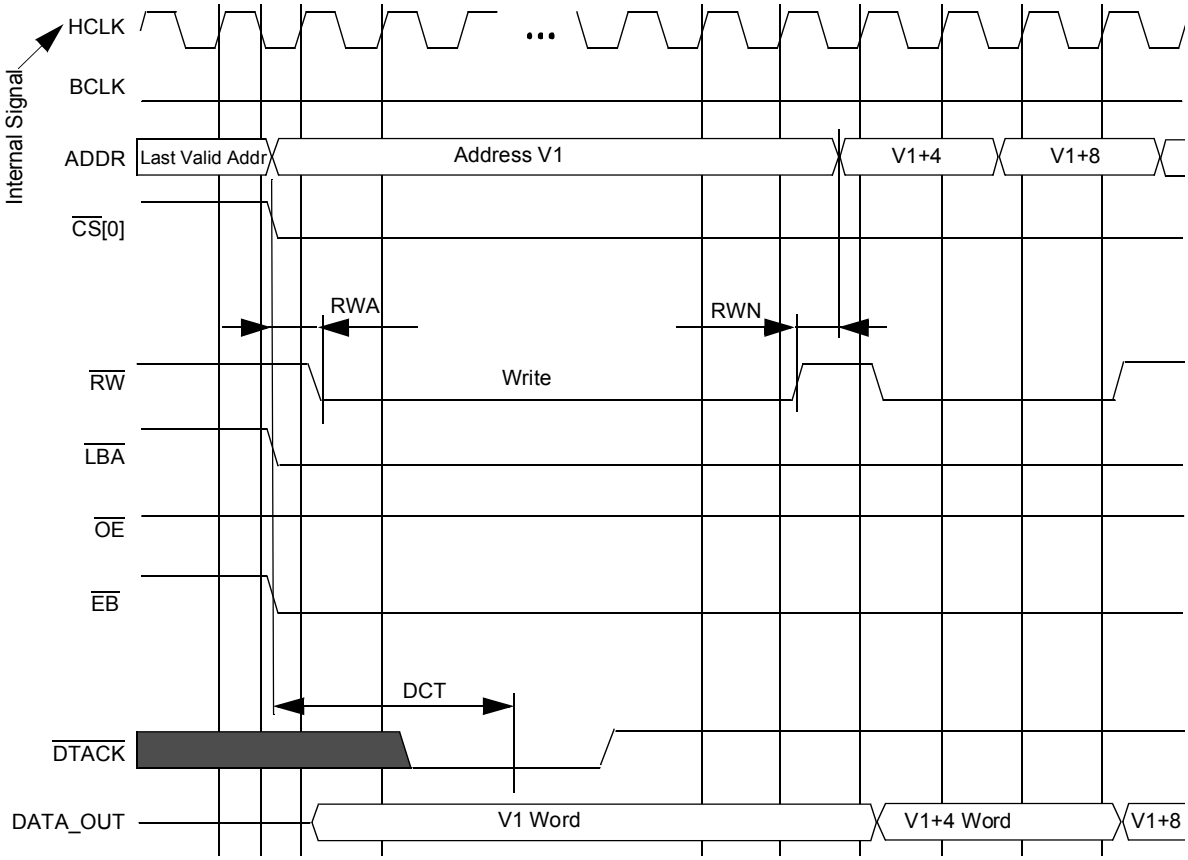


Figure 79. DTACK Level Sensitive Sequential Write Accesses, WSC=2, EW=1, RWA=1, RWN=1, DCT=1, AGE=0 (Example of DTACK Asserting)