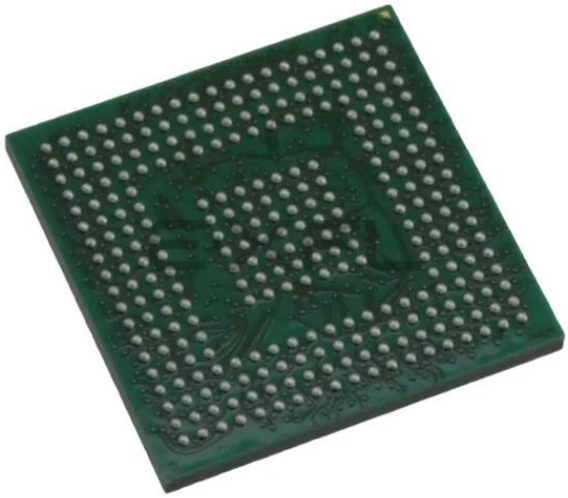

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21vmr2

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

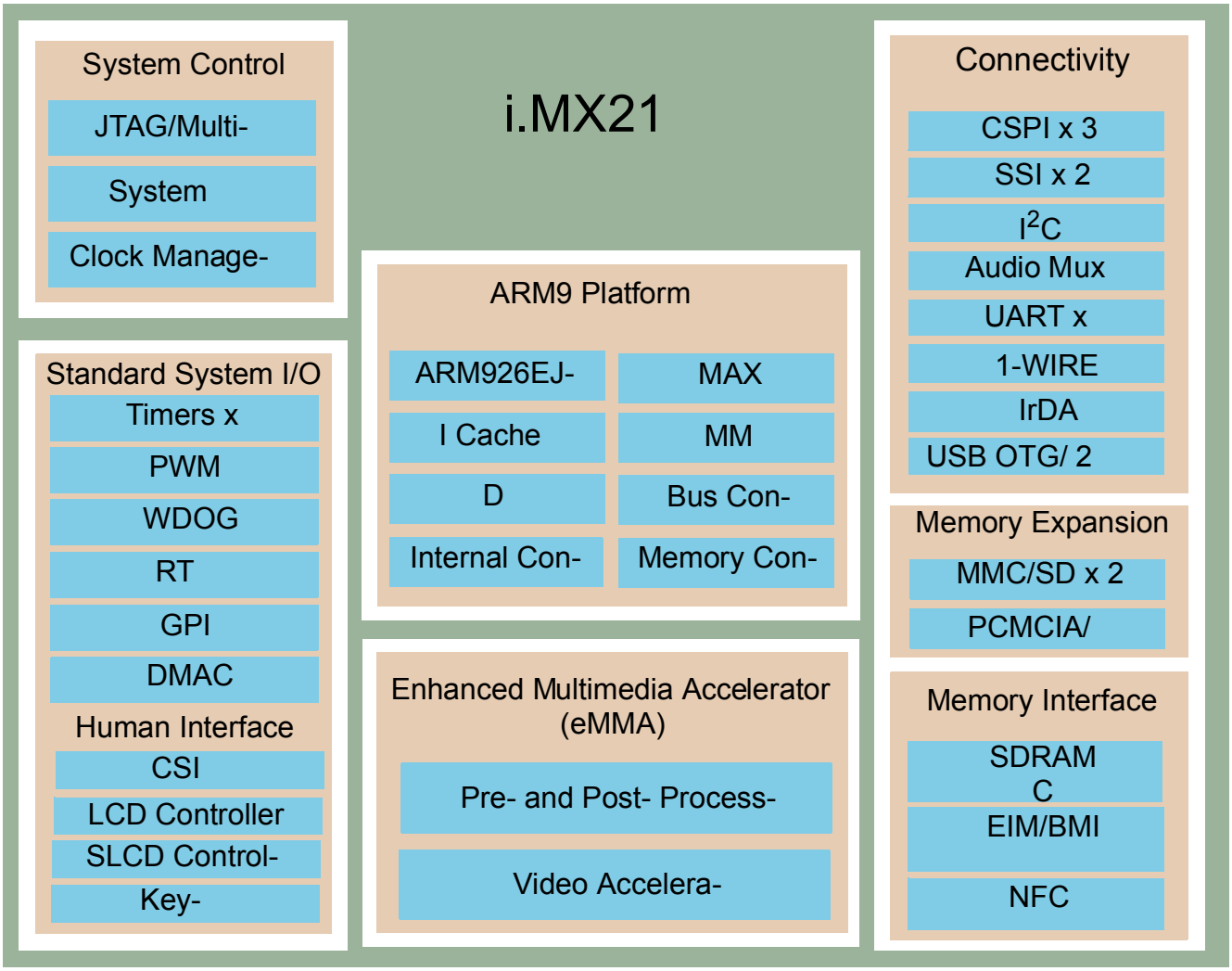


Figure 1. i.MX21 Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.

Table 1. Ordering Information[1] (Continued)

Part Order Number	Package Size	Package Type	Operating Range
MC9328MX21DVK!	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-30°C–70°C
MC9328MX21DVM!	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-30°C–70°C
MC9328MX21CVK!	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-40°C–85°C
MC9328MX21CVM!	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-40°C–85°C
MC9328MX21CJM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-40°C–85°C

1.5 Features

The i.MX21 boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21 features.

- ARM926EJ-S Core Complex
- enhanced Multimedia Accelerator (eMMA)
- Display and Video Modules
  - LCD Controller (LCDC)
  - Smart LCD Controller (SLCDC)
  - CMOS Sensor Interface (CSI)
- Bus Master Interface (BMI)
- Wireless Connectivity
  - Fast Infra-Red Interface (FIRI)
- Wired Connectivity
  - USB On-The-Go (USBOTG) Controller
  - Four Universal Asynchronous Receiver/Transmitters (UART*x*)
  - Three Configurable Serial Peripheral Interfaces (CSPI*x*) for High Speed Data Transfer
  - Inter-IC (I^2C) Bus Module
  - Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound (I^2S)
  - Digital Audio Mux
  - One-Wire Controller
  - Keypad Interface
- Memory Expansion and I/O Card Support
  - Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules

Table 13. DMA External Request and Grant Timing Parameters

Parameter	Description	3.0 V		1.8 V		Unit
		WCS	BCS	WCS	BCS	
t_{min_assert}	Minimum assertion time of External Grant signal	8 hclk + 8.6	8 hclk + 2.74	8 hclk + 7.17	8 hclk + 3.25	ns
$t_{max\_req\_assert}$	Maximum External request assertion time after assertion of Grant signal	9 hclk - 20.66	9 hclk - 6.7	9 hclk - 17.96	9 hclk - 8.16	ns
t_{max_read}	Maximum External request assertion time after first read completion	8 hclk - 6.21	8 hclk - 0.77	8 hclk - 5.84	8 hclk - 0.66	ns
t_{max_write}	Maximum External request assertion time after completion of first write	3 hclk - 15.87	3 hclk - 8.83	3 hclk - 15.9	3 hclk - 9.12	ns

3.8 BMI Interface Timing Diagram

3.8.1 Connecting BMI to ATI MMD Devices

3.8.1.1 ATI MMD Devices Drive the BMI_CLK/CS

In this mode MMD_MODE_SEL bit is set and MMD_CLKOUT bit is cleared. $\overline{\text{BMI\_WRITE}}$ and BMI_CLK/CS are input signals to BMI driving by ATI MMD chip set. Output signal BMI_READ_REQ can be used as interrupt signal to inform MMD that data is ready in BMI TxFIFO for read access. MMD can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

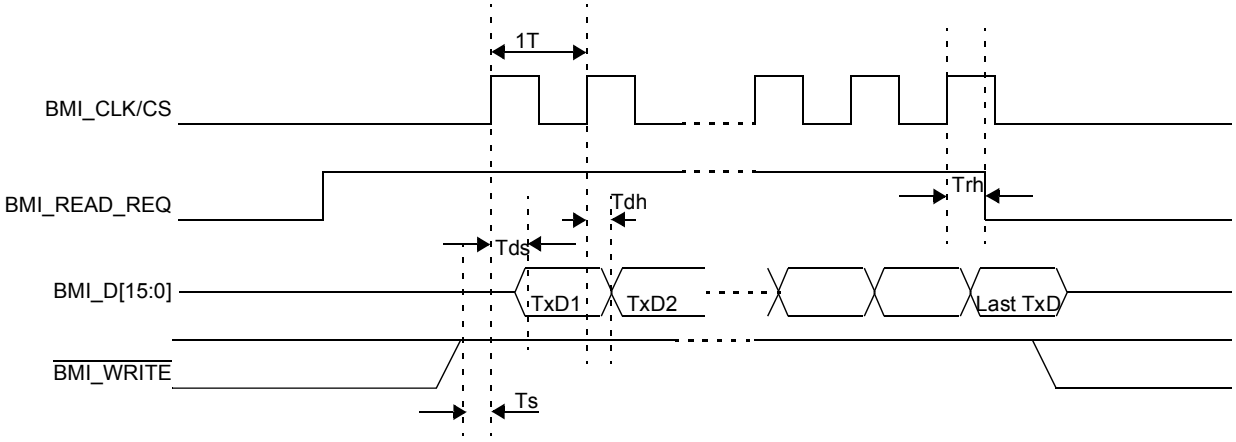


Figure 6. MMD (ATI) Drives Clock, MMD Read BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0,MMD_CLKOUT=0)

Table 14. MMD Read BMI Timing Table when MMD Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Clock period	1T	33.3	–	–	ns
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
read_req hold time	Trh	6	–	24	ns
transfer data setup time	Tds	6	–	14	ns
transfer data hold time	Tdh	6	-	14	ns

Note: All the timings assume that the hclk is running at 133 MHz.

Note: The MIN period of the 1T is assumed that MMD latch data at falling edge.

Note: If the MMD latch data at next rising edge, the ideally max clock can be as much as double, but because the BMI data pads are slow pads and it max frequency can only up to 18MHz, the max clock frequency can only up to 36 MHz.

3.8.1.1.2 MMD Write BMI Timing

Figure 7 shows the MMD write BMI timing when MMD drives clock. On each falling edge of BMI_CLK/$\overline{\text{CS}}$ BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a write cycle. If the $\overline{\text{BMI\_WRITE}}$ is logic low, it latches data into the RxFIFO on each falling edge of BMI_CLK/CS signal.

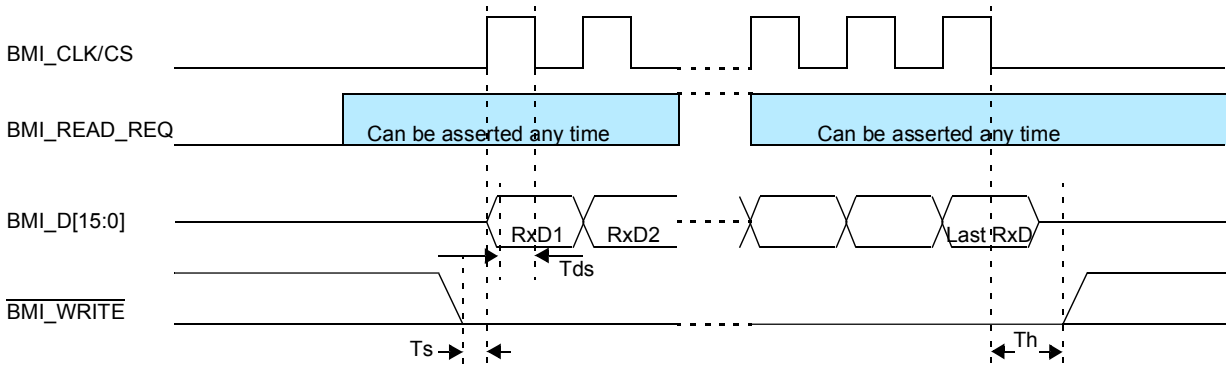


Figure 7. MMD (ATI) Drives Clock, MMD Write BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0, MMD_CLKOUT=0)

Table 15. MMD Write BMI Timing

Item	Symbol	Minimum	Typical	Maximum	Unit
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
$\overline{\text{write}}$ old ime h t	Th	0	–	–	ns
receive data setup time	Tds	5	–	–	ns

Note: All timings assume that the hclk is running at 133 MHz.

Note: At this mode, the maximum frequency of the BMI_CLK/CS can be up to 36 MHz (doubles as maximum data pad speed).

3.8.1.2 BMI Drives the BMI_CLK/CS

In this mode MMD_MODE_SEL and MMD_CLKOUT are both set. The software must know which mode it is now (READ or WRITE). When the $\overline{\text{BMI\_WRITE}}$ is high, BMI drives BMI_CLK/CS out if the TxFIFO is not emptied. When $\overline{\text{BMI\_WRITE}}$ is low, user can write a 1 to READ bit of control register1 to issue a write cycle (MMD write BMI).

3.8.1.3 MMD Read BMI Timing

Figure 13 shows the MMD read BMI timing when BMI drives the BMI_CLK/CS. When the $\overline{\text{BMI\_WRITE}}$ is high, the BMI drives BMI_CLK/CS out if data is written to TxFIFO (BMI_READ_REQ become high), BMI puts data into data bus and enable data out on the rising edge of BMI_CLK/CS. The MMD devices can latch the data on each falling edge of BMI_CLK/CS.

It is recommended that the MMD do not change the $\overline{\text{BMI\_WRITE}}$ signal from high to low when the BMI_READ_REQ is asserted. If user writes data to the TxFIFO when the $\overline{\text{BMI\_WRITE}}$ is low, the BMI will drive BMI_CLK/CS out once the $\overline{\text{BMI\_WRITE}}$ is changed from low to high.

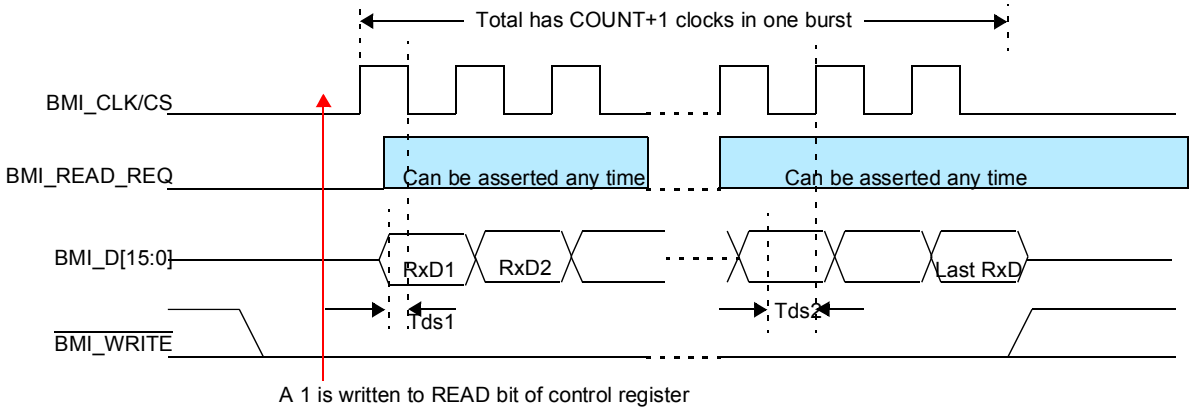


Figure 9. BMI Drives Clock, MMD Write BMI Timing (MASTER_MODE_SEL=0, MMD_MODE_SEL=1, MMD_CLKOUT=1)

Table 17. MMD Write BMI Timing Table when BMI Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Receive data setup time1	Tds1	14	–	–	ns
Receive data setup time2	Tds2	14	–	–	ns

Note: The BMI_CLK/CS can only be up to 30MHz if BMI latch data at the falling edge and can be up to 36MHz (double as max data pad speed) if BMI latch data at the next rising edge.

Note: Tds1 is the receive data setup time when BMI latch data at the falling edge.

Note: Tds2 is the receive data setup time when BMI latch data at the next rising edge.

3.8.2 Connecting BMI to External Bus Master Devices

In this mode both MASTER_SEL bit and MMD_MODE_SEL bit are cleared and the MMD_CLKOUT bit is no useful. $\overline{\text{BMI\_WRITE}}$ and BMI_CLK/CS are input signals driving by the external bus master. The Output signal BMI_READ_REQ can be used as an interrupt signal to inform external bus master that data is ready in the BMI TxFIFO for a read access. The external bus master can write data to the BMI RxFIFO anytime since the CPU or DMA can move data out from RxFIFO much faster than the BMI interface. An overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

Each falling edge of BMI_CLK/CS will determine if the current cycle is read or write cycle. It drives data and enables data out if $\overline{\text{BMI\_WRITE}}$ is logic high. The D_EN signal remains active only while BMI_CLK/CS is logic low and $\overline{\text{BMI\_WRITE}}$ is logic high.

Each rising edge of BMI_CLK/CS will determine if data should be latched to RxFIFO from the data bus.

Table 19. Timing Parameters for Figure 14 through Figure 18

Ref No.	Parameter	Minimum	Maximum	Unit
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T [1]	–	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3·Tsclk [2]	–	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2·Tsclk	–	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	–	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	–	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	–	ns
7	$\overline{\text{SS}}$ input pulse width	T	–	ns

1. T = CSPI system clock period (PERCLK2).
2. Tsclk = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

3.10 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *i.MX21 Reference Manual*.

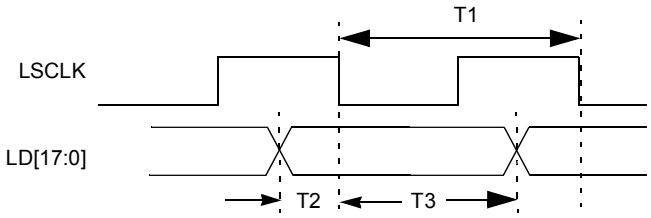


Figure 19. SCLK to LD Timing Diagram

Table 20. LCDC SCLK Timing Parameters

Symbol	Parameter	3.0 ± 0.3V		Unit
		Minimum	Maximum	
T1	SCLK period	23	2000	ns
T2	Pixel data setup time	11	–	ns
T3	Pixel data up time	11	–	ns
The pixel clock is equal to LCDC_CLK / (PCD + 1). When it is in CSTN, TFT or monochrome mode with bus width = 1, SCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, SCLK is equal to the pixel clock divided by bus width. The polarity of SCLK and LD can also be programmed. Maximum frequency of SCLK is HCLK / 3 for TFT and CSTN, otherwise LD output will be incorrect.				

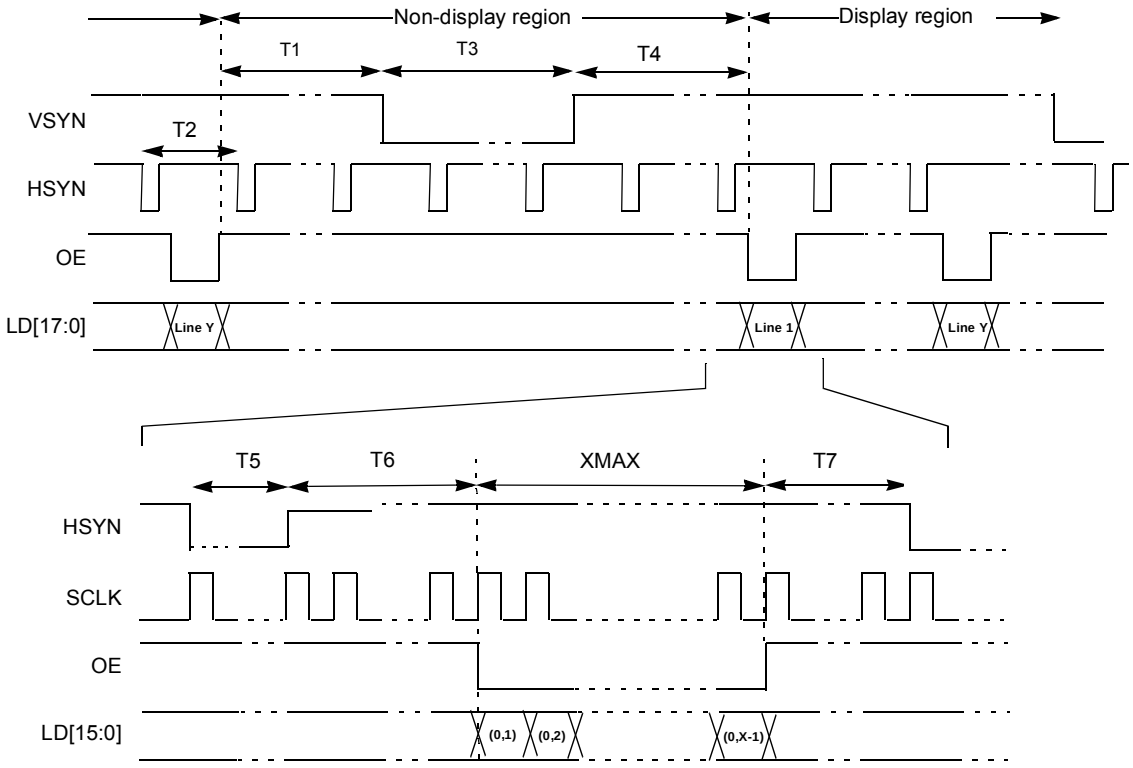


Figure 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 21. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	End of OE to beginning of VSYN	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	HSYN period	–	XMAX+T5+T6+T7	Ts
T3	VSYN pulse width	T2	VWIDTH·T2	Ts
T4	End of VSYN to beginning of OE	1	(VWAIT2·T2)+1	Ts
T5	HSYN pulse width	1	HWIDTH+1	Ts
T6	End of HSYN to beginning to OE	3	HWAIT2+3	Ts
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts

Note:
- Ts is the SCLK period.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 20, all 3 signals are active low.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 20, SCLK is always active.
- XMAX is defined in number of pixels in one line.

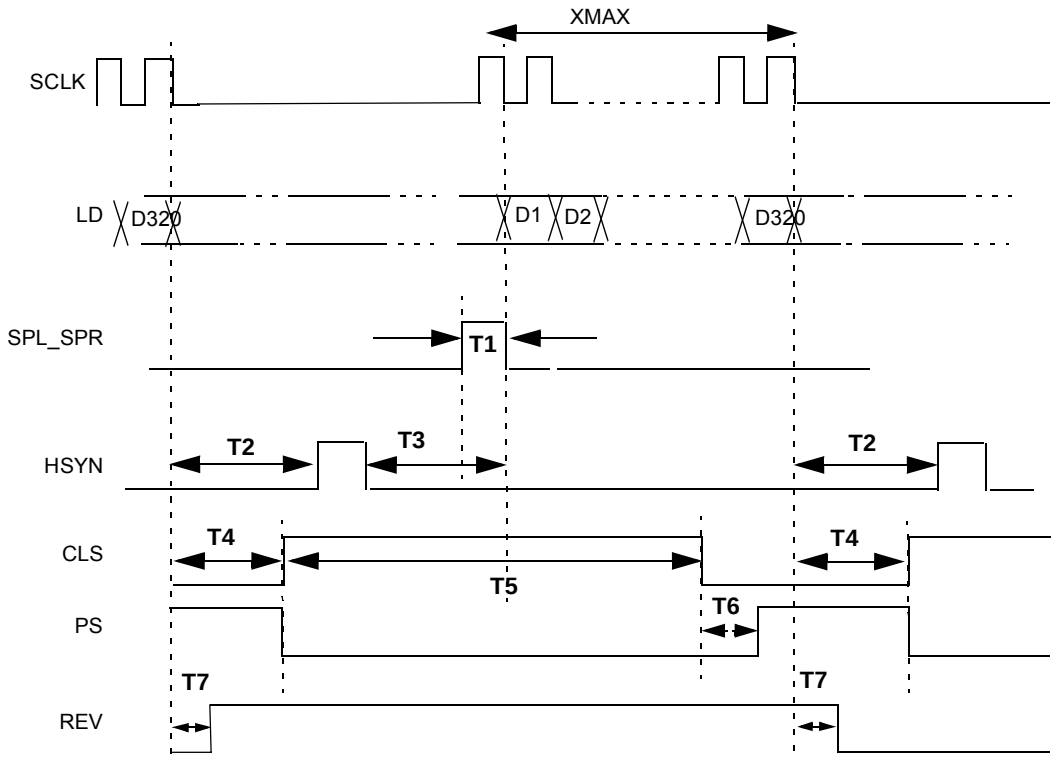


Figure 21. Sharp TFT Panel Timing

Table 22. Sharp TFT Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	SPL/SPR pulse width	–	1	Ts
T2	End of LD of line to beginning of HSYN	1	HWAIT1+1	Ts
T3	End of HSYN to beginning of LD of line	4	HWAIT2 + 4	Ts
T4	CLS rise delay from end of LD of line	3	CLS_RISE_DELAY+1	Ts
T5	CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	PS rise delay from CLS negation	0	PS_RISE_DELAY	Ts
T7	REV toggle delay from last LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note:
- Falling of SPL/SPR aligns with first LD of line.
- Falling of PS aligns with rising edge of CLS.
- REV toggles in every HSYN period.

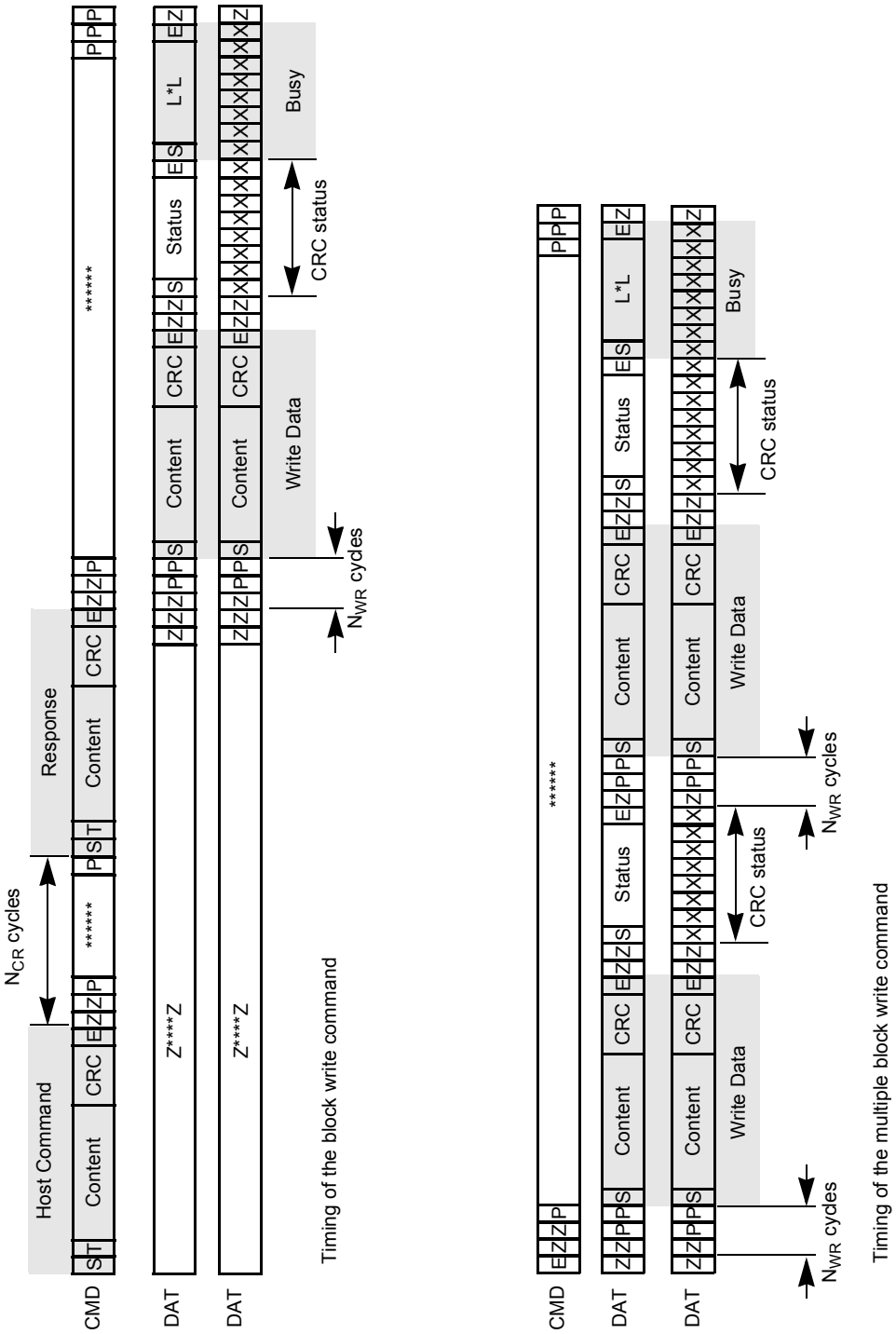


Figure 29. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 30 shows the different scenarios on the bus.

3.13 External Memory Interface (EMI) Electricals

3.13.1 NAND-Flash Controller (NFC) Interface

Figure 33, Figure 34, Figure 35, and Figure 36 depict the relative timing requirements among different signals of the NFC at module level, and Table 29 lists the timing parameters. The NAND Flash Controller (NFC) timing parameters are based on the internal NFC clock generated by the Clock Controller module, where time T is the period of the NFC clock in ns. Per the i.MX21 Reference Manual, specifically the *Phase-Locked (PLL), Clock, and Reset Controller* chapter, the NFC clock is derived from the same clock which drives the CPU clock (FCLK) that is fed through the NFCDIV block to generate the NFC clock. The relationship between the NFC clock and the external timing parameters of the NFC is provided in Table 29.

Table 29 also provides two examples of external timing parameters with NFC clock frequencies of 22.17 MHz and 33.25 MHz. For example, assuming a 266 MHz FCLK (CPU clock), NFCDIV should be set to divide-by-12 to generate a 22.17 MHz NFC clock and divide-by-8 to generate a 33.25 MHz NFC clock. The user should compare the parameters of the selected NAND Flash memory with the NFC external timing parameters to determine the proper NFC clock. *The maximum NFC clock allowed is 66 MHz*. It should also be noted that the default NFC clock on power up is 16.63 MHz.

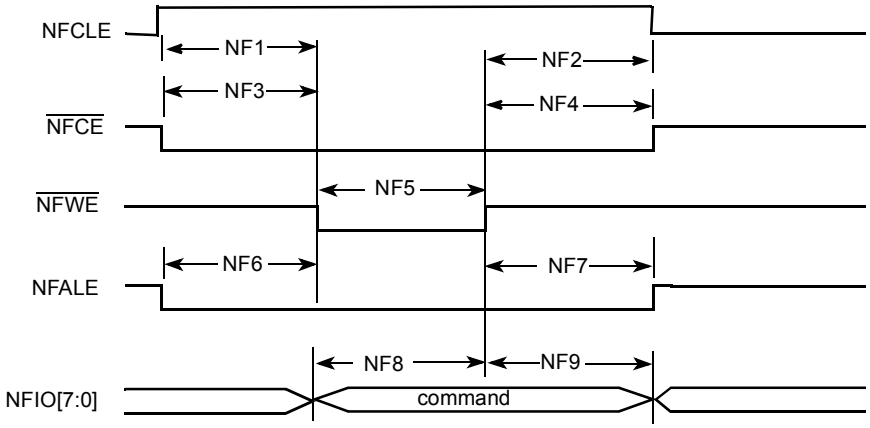


Figure 33. Command Latch Cycle Timing Diagram

Table 29. NFC Target Timing Parameters[1],[2]

ID	Parameter	Symbol	Relationship to NFC Clock Period (T)		NFC Clock 22.17 MHz T = 45 ns		NFC Clock 33.25 MHz T = 30 ns		Unit
			Min	Max	Min	Max	Min	Max	
NF1	NFCLE Setup Time	tCLS	T	–	45	–	30	–	ns
NF2	NFCLE Hold Time	tCLH	T	–	45	–	30	–	ns
NF3	$\overline{\text{NFCE}}$ Setup Time	tCS	T	–	45	–	30	–	ns
NF4	$\overline{\text{NFCE}}$ Hold Time	tCH	T	–	45	–	30	–	ns
NF5	$\overline{\text{NF\_WP}}$ Pulse Width	tWP	T	–	45	–	30	–	ns
NF6	NFALE Setup Time	tALS	T	–	45	–	30	–	ns
NF7	NFALE Hold Time	tALH	T	–	45	–	30	–	ns
NF8	Data Setup Time	tDS	T	–	45	–	30	–	ns
NF9	Data Hold Time	tDH	T	–	45	–	30	–	ns
NF10	Write Cycle Time	tWC	2T	–	90	–	60	–	ns
NF11	$\overline{\text{NFWE}}$ Hold Time	tWH	T	–	45	–	30	–	ns
NF12	Ready to $\overline{\text{NFRE}}$ Low	tRR	4T	–	180	–	120	–	ns
NF13	$\overline{\text{NFRE}}$ Pulse Width	tRP	1.5T	–	67.5	–	45	–	ns
NF14	READ Cycle Time	tRC	2T	–	90	–	60	–	ns
NF15	$\overline{\text{NFRE}}$ High Hold Time	tREH	0.5T	–	22.5	–	15	–	ns
NF16	Data Setup on READ	tDSR	15	–	15	–	15	–	ns
NF17	Data Hold on READ	tDHR	0	–	0	–	0	–	ns

1. High is defined as 80% of signal value and low is defined as 20% of signal value. All timings are listed according to this NFC clock frequency (multiples of NFC clock period) except NF16, which is not NFC clock related.
2. The read data is generated by the NAND Flash device and sampled with the internal NFC clock.

Table 35. SSI to SSI1 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
20	(Tx) CK high to FS (bl) low	10.22	17.63	8.82	16.24	ns
21	(Rx) CK high to FS (bl) low	10.79	19.67	9.39	18.28	ns
22	(Tx) CK high to FS (wl) high	10.22	17.63	8.82	16.24	ns
23	(Rx) CK high to FS (wl) high	10.79	19.67	9.39	18.28	ns
24	(Tx) CK high to FS (wl) low	10.22	17.63	8.82	16.24	ns
25	(Rx) CK high to FS (wl) low	10.79	19.67	9.39	18.28	ns
26	(Tx) CK high to STXD valid from high impedance	10.05	15.75	8.66	14.36	ns
27a	(Tx) CK high to STXD high	10.00	15.63	8.61	14.24	ns
27b	(Tx) CK high to STXD low	10.00	15.63	8.61	14.24	ns
28	(Tx) CK high to STXD high impedance	10.05	15.75	8.66	14.36	ns
29	SRXD setup time before (Rx) CK low	0.78	–	0.47	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI1 Ports)						
31	SRXD setup before (Tx) CK falling	19.90	–	19.90	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI1 Ports)						
33	SRXD setup before (Tx) CK falling	2.59	–	2.28	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 36. SSI to SSI2 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI2 Ports)						
1	(Tx/Rx) CK clock period[1] 90	.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	0.01	0.15	0.01	0.15	ns
3	(Rx) CK high to FS (bl) high	-0.21	0.05	-0.21	0.05	ns
4	(Tx) CK high to FS (bl) low	0.01	0.15	0.01	0.15	ns
5	(Rx) CK high to FS (bl) low	-0.21	0.05	-0.21	0.05	ns
6	(Tx) CK high to FS (wl) high	0.01	0.15	0.01	0.15	ns
7	(Rx) CK high to FS (wl) high	-0.21	0.05	-0.21	0.05	ns
8	(Tx) CK high to FS (wl) low	0.01	0.15	0.01	0.15	ns
9	(Rx) CK high to FS (wl) low	-0.21	0.05	-0.21	0.05	ns
10	(Tx) CK high to STXD valid from high impedance	0.34	0.72	0.34	0.72	ns

Table 37. SSI to SSI3 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI3 Ports)						
1	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-2.09	-0.66	-2.09	-0.66	ns
3	(Rx) CK high to FS (bl) high	-2.74	-0.84	-2.74	-0.84	ns
4	(Tx) CK high to FS (bl) low	-2.09	-0.66	-2.09	-0.66	ns
5	(Rx) CK high to FS (bl) low	-2.74	-0.84	-2.74	-0.84	ns
6	(Tx) CK high to FS (wl) high	-2.09	-0.66	-2.09	-0.66	ns
7	(Rx) CK high to FS (wl) high	-2.74	-0.84	-2.74	-0.84	ns
8	(Tx) CK high to FS (wl) low	-2.09	-0.66	-2.09	-0.66	ns
9	(Rx) CK high to FS (wl) low	-2.74	-0.84	-2.74	-0.84	ns
10	(Tx) CK high to STXD valid from high impedance	-1.73	-0.26	-1.73	-0.26	ns
11a	(Tx) CK high to STXD high	-2.87	-0.80	-2.87	-0.80	ns
11b	(Tx) CK high to STXD low	-2.87	-0.80	-2.87	-0.80	ns
12	(Tx) CK high to STXD high impedance	-1.73	-0.26	-1.73	-0.26	ns
13	SRXD setup time before (Rx) CK low	22.77	–	22.77	–	ns
14	SRXD old ime after r Rx) CK low (	0	–	0	–	ns
External Clock Operation (SSI3 Ports)						
15	(Tx/Rx) CK clock period[1] 90.	91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	9.62	17.10	7.90	15.61	ns
19	(Rx) CK high to FS (bl) high	10.30	19.54	8.58	18.05	ns
20	(Tx) CK high to FS (bl) low	9.62	17.10	7.90	15.61	ns
21	(Rx) CK high to FS (bl) low	10.30	19.54	8.58	18.05	ns
22	(Tx) CK high to FS (wl) high	9.62	17.10	7.90	15.61	ns
23	(Rx) CK high to FS (wl) high	10.30	19.54	8.58	18.05	ns
24	(Tx) CK high to FS (wl) low	9.62	17.10	7.90	15.61	ns
25	(Rx) CK high to FS (wl) low	10.30	19.54	8.58	18.05	ns
26	(Tx) CK high to STXD valid from high impedance	9.02	16.46	7.29	14.97	ns
27a	(Tx) CK high to STXD high	8.48	15.32	6.75	13.83	ns
27b	(Tx) CK high to STXD low	8.48	15.32	6.75	13.83	ns

Note: Signals listed with lower case letters are internal to the device.

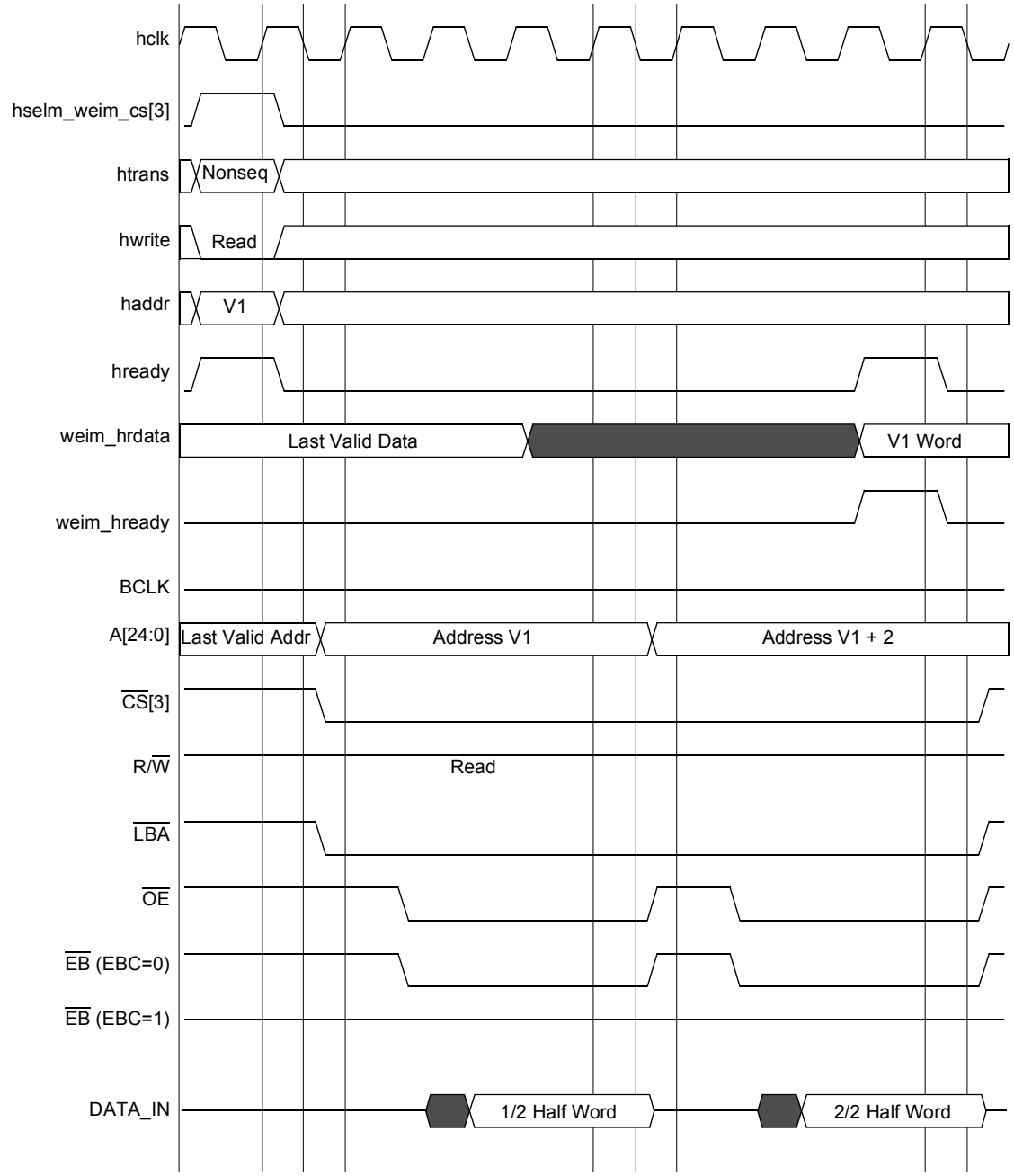


Figure 58. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

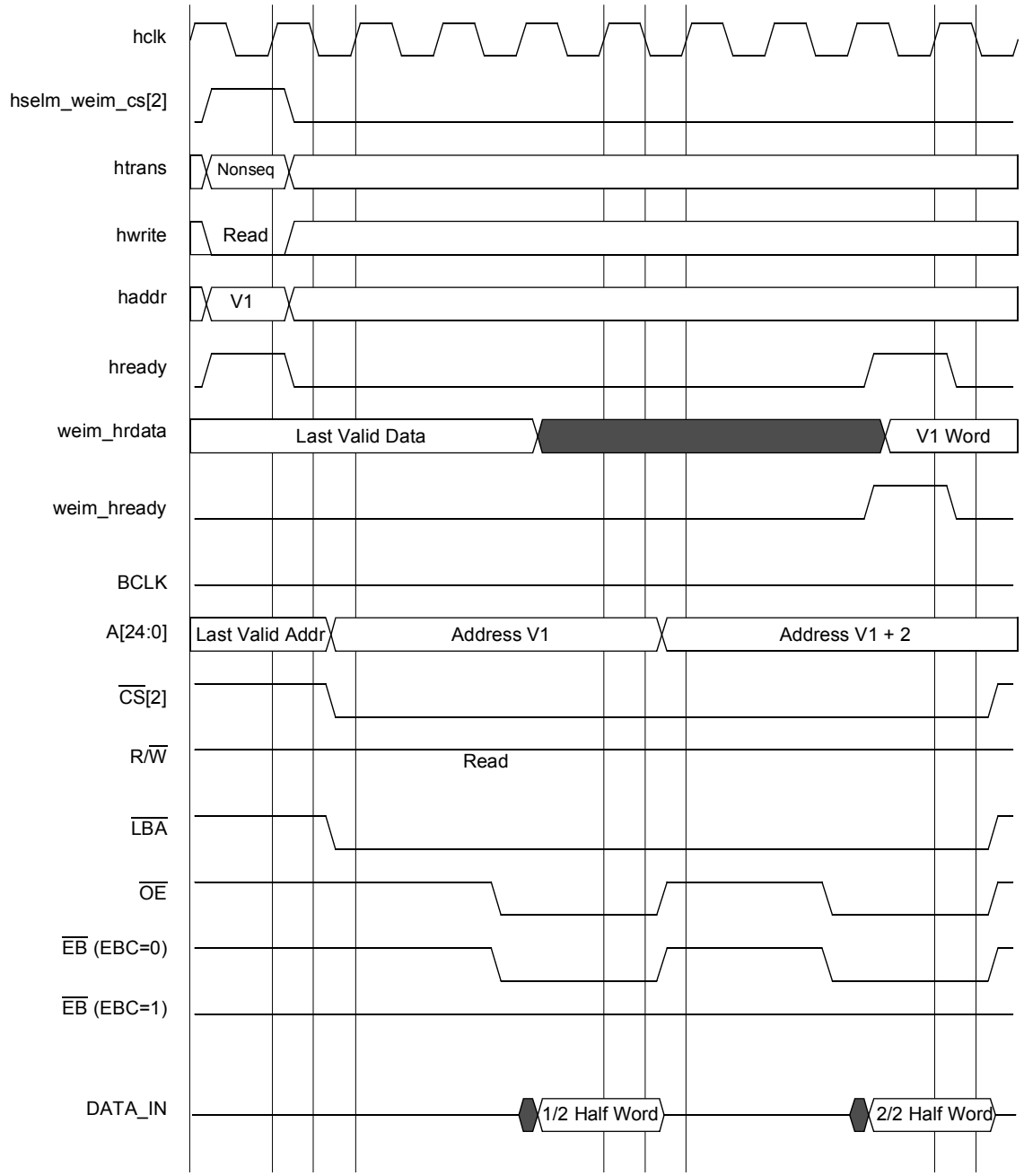


Figure 60. WSC = 3, OEA = 4, A.WORD/E.HALF

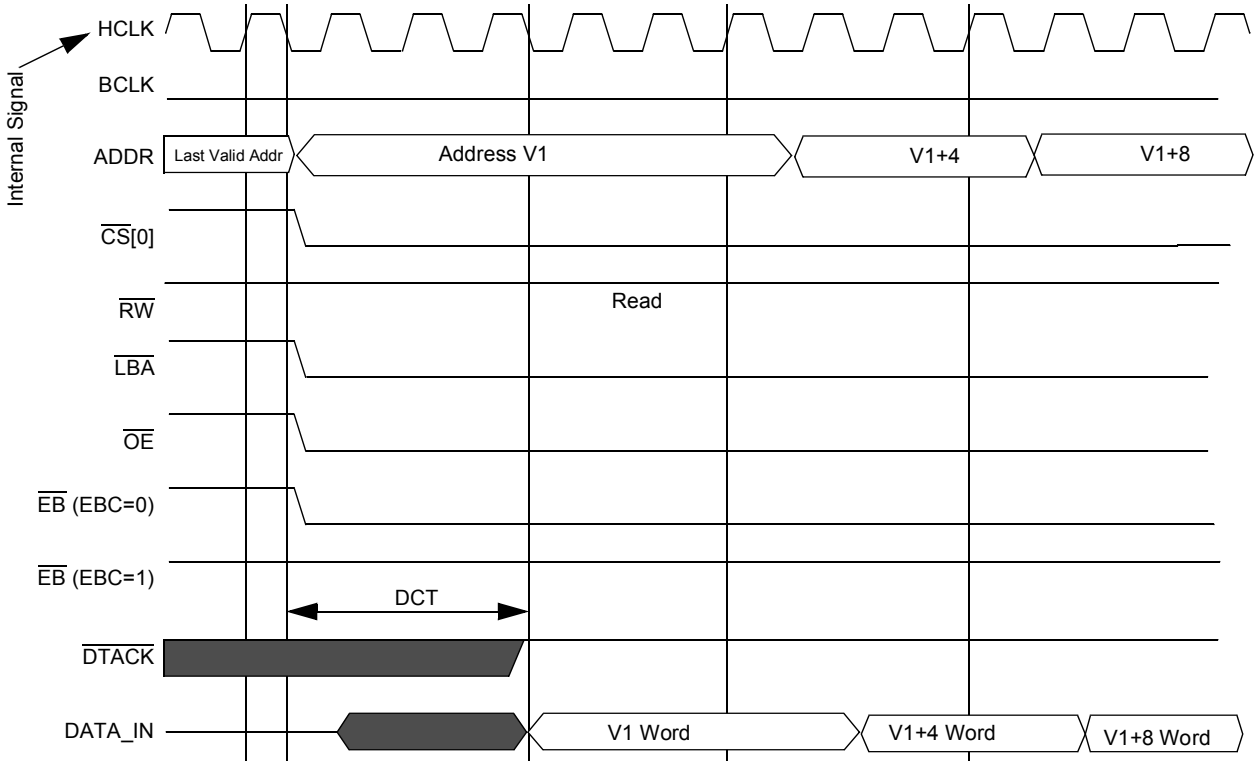


Figure 78. DTACK Level Sensitive Sequential Read Accesses, WSC=2, EW=1, DCT=1, AGE=0 (Example of DTACK Remaining High)

3.21 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

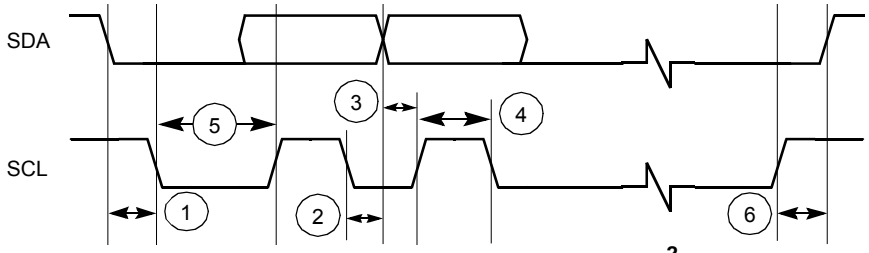


Figure 80. Definition of Bus Timing for I²C

Table 44. I²C Bus Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
	SCL Clock Frequency	0	100	0	100	kHz
1	Hold time (repeated) START condition	114.8	–	111.1	–	ns
2	Data hold time	0	69.7	0	72.3	ns
3	Data setup time	3.1	–	1.76	–	ns
4	HIGH period of the SCL clock	69.7	–	68.3	–	ns
5	LOW period of the SCL clock	336.4	–	335.1	–	ns
6	Setup time for STOP condition	110.5	–	111.1	–	ns

3.22 CMOS Sensor Interface

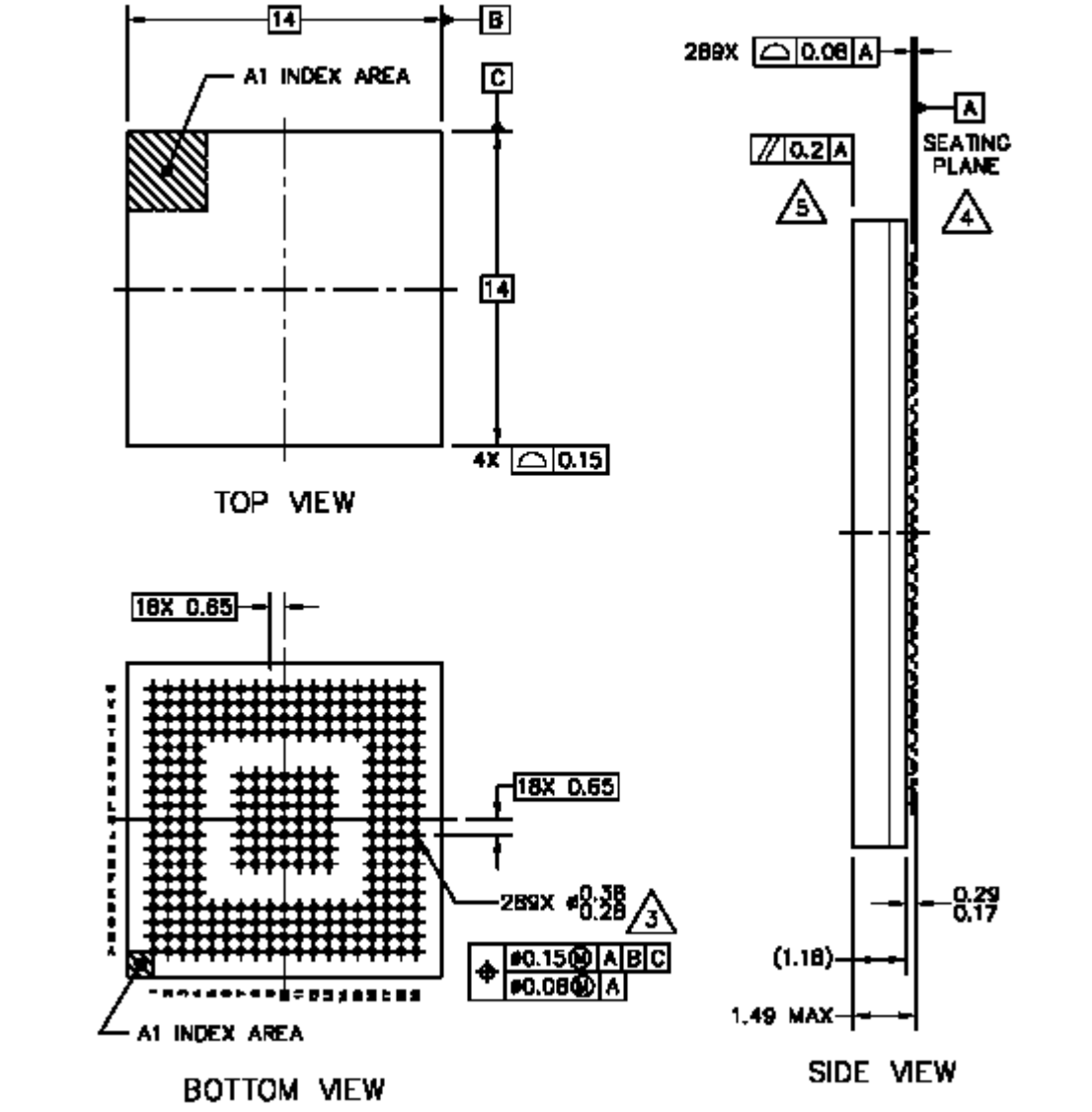
The CSI module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32 × 32 image data receive FIFO, and a 16 × 32 statistic data FIFO.

3.22.1 Gated Clock Mode

Figure 81 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 82 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 45. The formula for calculating the pixel clock rise and fall time is located in Section 3.22.3, “Calculation of Pixel Clock Rise/ Fall Time.”

4.1 MAPBGA Package Dimensions

Figure 85 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.



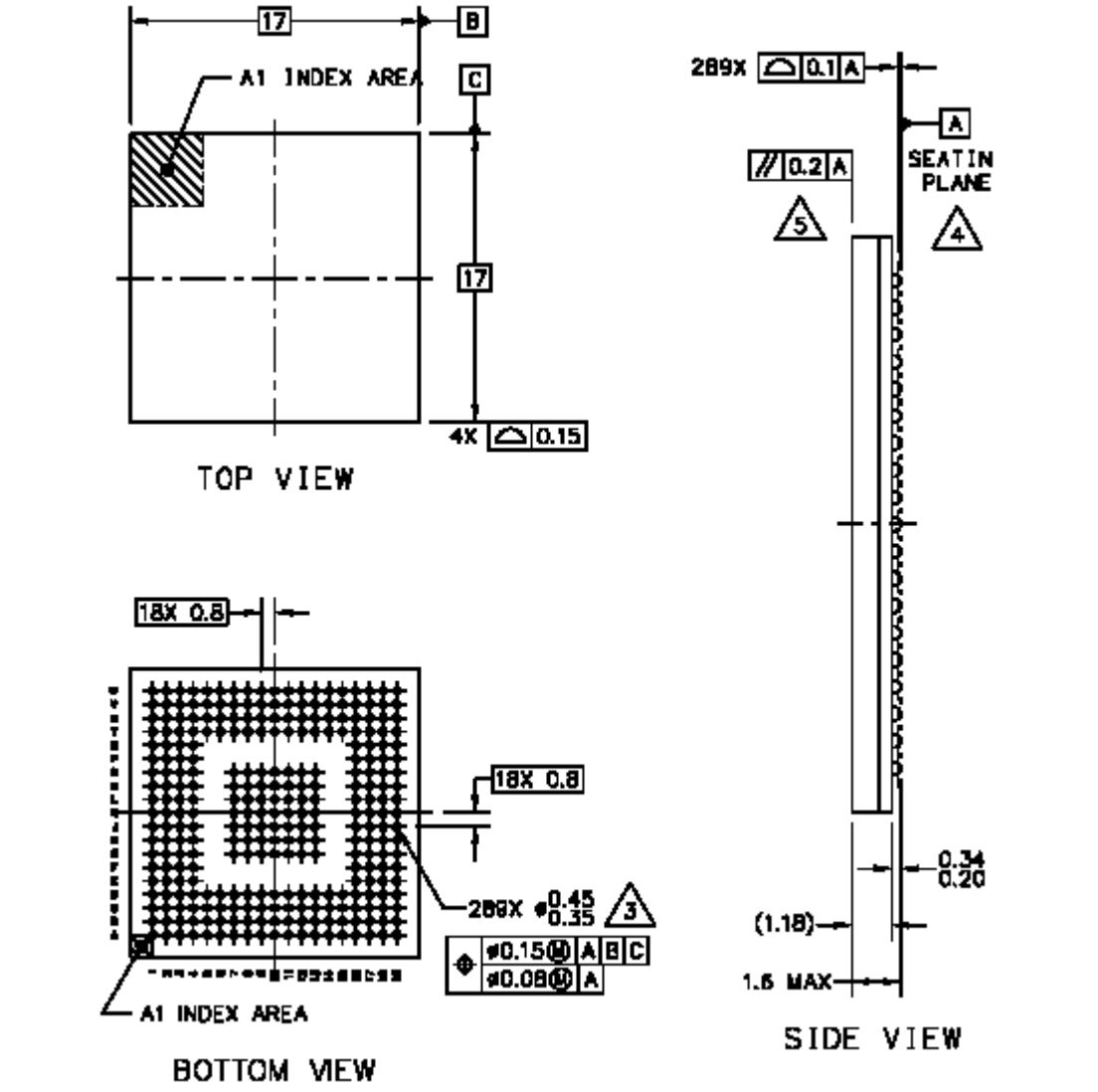
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 85. i.MX21 MAPBGA Mechanical Drawing

4.2 MAPBGA Package Dimensions

Figure 86 illustrates the MAPBGA 17 mm × 17 mm × 1.45 mm package, which has 0.8 mm spacing between the pads.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 86. i.MX21 MAPBGA Mechanical Drawing