Renesas Electronics America Inc - R5F51135ADFM#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51135adfm-30

Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
Comparator B	CMPB0	Input	Input pin for the analog signal to be processed by comparator B0.
	CVREFB0	Input	Analog reference voltage supply pin for comparator B0.
	CMPB1	Input	Input pin for the analog signal to be processed by comparator B1.
	CVREFB1	Input	Analog reference voltage supply pin for comparator B1.
	CMPOB0	Output	Output pin for comparator B0.
	CMPOB1	Output	Output pin for comparator B1.
LCD	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD.
	CAPH, CAPL	I/O	Capacitor connection pin for the LCD controller/driver.
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver.
	SEG00 to SEG39	Output	Segment signal output pins for the LCD controller/driver.
CTSU	TS0 to TS11	Input	Capacitive touch detection pins (touch pins).
	TSCAP	I/O	Secondary power supply pin for the touch driver.
I/O ports	P02, P04, P07	I/O	3-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P90 to P92	I/O	3-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD4	I/O	5-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF6, PF7	I/O	2-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ0, PJ2, PJ3, PJ6, PJ7	I/O	5-bit input/output pins.

Note 1. For external clock input.

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
36		P11	MTIC5U/POE0#	RXD12/RXDX12/SMISO12/ SSCL12/ RXD0/SMISO0/SSCL0	SEG02	IRQ7
37		P10	MTIC5V/POE1#	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/TXD0/SMOSI0/SSDA0	SEG03	IRQ6
38		P56	MTIOC1A/MTIC5W/ POE2#	TXD1/SMOSI1/SSDA1	SEG04	IRQ5
39		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
40		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
41		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
42		P50	MTIOC2A	MOSIA/TXD2/SMOSI2/SSDA2	SEG08	
43		P55	MTIOC4D/TMO3		VL1	
44		P54	MTIOC4B/TMCI1		VL2	
45		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
46		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
47		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
48		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	
50		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
51		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/ COM4	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
55		PB5	MTIOC1B/MTIOC2A/ POE1#/TMRI1	SCK9/SSISCK0	SEG13/ COM6	
56		PB4		CTS9#/RTS9#/SS9#	SEG14	
57		PB3	MTIOC0A/MTIOC3B/ MTIOC4A/POE3#/TMO0	SCK6/AUDIO_MCLK/ USB0_OVRCURA	SEG15/ COM7	
58		PB2		CTS6#/RTS6#/SS6#	SEG16	
59		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6/SSIWS0	SEG17	IRQ4
60	VCC					
61		PB0	MTIOC0C/MTIC5W/ RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/ SSCL6		IRQ2/ADTRG0#
62	VSS					
63		PA6	MTIC5V/MTCLKB/ MTIOC2A/POE2#/TMCI3	CTS5#/RTS5#/SS5#/SDA0/MOSIA/ RXD8/SMISO8/SSCL8		IRQ3
64		PA7		TXD8/SMOSI8/SSDA8	SEG18	
65		PA5		SCK8	SEG19	
66		PA4	MTIOC2B/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0/CTS8#/RTS8#/SS8#	SEG20	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTIOC1B/ MTCLKD/POE0#	RXD5/SMISO5/SSCL5/IRRXD5/ MISOA	SEG21	IRQ6/CMPB1

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
68		PA2		RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	SEG22	
69		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	SEG23	
70		PA0	MTIOC4A	SSLA1	SEG24	CACREF
71		PF7	MTIOC3A		SEG25	
72		PF6	MTIOC3C		SEG26	
73		PE5	MTIOC2B/MTIOC4C	MISOA/TXD9/SMOSI9/SSDA9	SEG27	IRQ5/AN013/ CMPOB1
74		PE4	MTIOC1A/MTIOC3A/ MTIOC4D	MOSIA/RXD9/SMISO9/SSCL9/ SSIWS0	SEG28	IRQ4/AN012
75		PE3	MTIOC0A/MTIOC1B/ MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA/ SCK9/AUDIO_MCLK	SEG29	IRQ3/AN011
76		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12/SSIRXD0	SEG30	IRQ7/AN010/ CVREFB0
77		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/SSITXD0	SEG31	IRQ1/AN009/ CMPB0
78		PE0	MTIOC2A/POE3#	SCK12/CTS9#/RTS9#/SS9#/ SSISCK0	SEG32	IRQ0/AN008
79		PE7			SEG33	IRQ7/AN015/ CMPOB0
80		PE6			SEG34	IRQ6/AN014
81		PD4	POE3#		SEG35	IRQ4
82		PD3	POE8#		SEG36	IRQ3
83		PD2	MTIOC4D		SEG37	IRQ2
84		PD1	MTIOC4B		SEG38	IRQ1
85		PD0			SEG39	IRQ0
86		P92*2				AN021
87		P91*2				AN007
88		P46*2				AN006
89		P90*2				AN005
90		P44*2				AN004
91		P43*2				AN003
92	VREFL	P42*2				AN002
93	VREFH	P41*2				AN001
94	VREFL0	PJ7*2				
95		P40*2				AN000
96	VREFH0	PJ6*2				
97	AVSS0					
98	AVCC0					
99		P07		TXD6/SMOSI6/SSDA6	TS0	ADTRG0#
100		PJ2				DA1

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
H1	XTAL					
H2	EXTAL					
H3		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
H4		P13	MTIOC0B/TMO3	CTS12#/RTS12#/SS12#/CTS0#/ RTS0#/SS0#	SEG00	IRQ3
H5		P11	MTIC5U/POE0#	RXD12/RXDX12/SMISO12/ SSCL12/RXD0/SMISO0/SSCL0	SEG02	IRQ7
H6		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
H7		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
H8		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/ COM4	
J1	VCL					
J2		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
J3		P32	MTIOC0C/RTCOUT/ TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#	TS11	IRQ2
J4	VCC_USB					
J5	VSS_USB					
J6		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
J7		P55	MTIOC4D/TMO3		VL1	
J8		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
J9		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
J10		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
K1	VSS					
K2	VDD					
K3		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
K4				USB0_DM		
K5				USB0_DP		
K6		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
K7		P54	MTIOC4B/TMCI1		VL2	
K8		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
K9		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
K10		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to I/O registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

While writing to an I/O register, the CPU starts executing subsequent instructions before the I/O register write access is completed. This may cause the subsequent instructions to be executed before the write value is reflected in the operation. The examples below show how subsequent instructions must be executed after a write access to an I/O register is completed.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value in the I/O register and write it to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

Example of instructions

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1 to 6

The number of bus cycles of internal peripheral buses 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral buses 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (5/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC Activation Enable Register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC Activation Enable Register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC Activation Enable Register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC Activation Enable Register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC Activation Enable Register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC Activation Enable Register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC Activation Enable Register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC Activation Enable Register 216	DTCER216	8	8	2 ICLK
0008 71DBh	ICU	DTC Activation Enable Register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKB
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKB
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB
0008 864Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKB
0008 8660h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKB
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB
0008 8684h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKB
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8693h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8694h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0840h	LCDC	LCD Display Data Register 00	SEG00	8	8	1 or 2 PCLKB
000A 0841h	LCDC	LCD Display Data Register 01	SEG01	8	8	1 or 2 PCLKB
000A 0842h	LCDC	LCD Display Data Register 02	SEG02	8	8	1 or 2 PCLKB
000A 0843h	LCDC	LCD Display Data Register 03	SEG03	8	8	1 or 2 PCLKB
000A 0844h	LCDC	LCD Display Data Register 04	SEG04	8	8	1 or 2 PCLKB
000A 0845h	LCDC	LCD Display Data Register 05	SEG05	8	8	1 or 2 PCLKB
000A 0846h	LCDC	LCD Display Data Register 06	SEG06	8	8	1 or 2 PCLKB
000A 0847h	LCDC	LCD Display Data Register 07	SEG07	8	8	1 or 2 PCLKB
000A 0848h	LCDC	LCD Display Data Register 08	SEG08	8	8	1 or 2 PCLKB
000A 0849h	LCDC	LCD Display Data Register 09	SEG09	8	8	1 or 2 PCLKB
000A 084Ah	LCDC	LCD Display Data Register 10	SEG10	8	8	1 or 2 PCLKB
000A 084Bh	LCDC	LCD Display Data Register 11	SEG11	8	8	1 or 2 PCLKB
000A 084Ch	LCDC	LCD Display Data Register 12	SEG12	8	8	1 or 2 PCLKB
000A 084Dh	LCDC	LCD Display Data Register 13	SEG13	8	8	1 or 2 PCLKB
000A 084Eh	LCDC	LCD Display Data Register 14	SEG14	8	8	1 or 2 PCLKB
000A 084Fh	LCDC	LCD Display Data Register 15	SEG15	8	8	1 or 2 PCLKB
000A 0850h	LCDC	LCD Display Data Register 16	SEG16	8	8	1 or 2 PCLKB
000A 0851h	LCDC	LCD Display Data Register 17	SEG17	8	8	1 or 2 PCLKB
000A 0852h	LCDC	LCD Display Data Register 18	SEG18	8	8	1 or 2 PCLKB
000A 0853h	LCDC	LCD Display Data Register 19	SEG19	8	8	1 or 2 PCLKB
000A 0854h	LCDC	LCD Display Data Register 20	SEG20	8	8	1 or 2 PCLKB
000A 0855h	LCDC	LCD Display Data Register 21	SEG21	8	8	1 or 2 PCLKB
000A 0856h	LCDC	LCD Display Data Register 22	SEG22	8	8	1 or 2 PCLKB
000A 0857h	LCDC	LCD Display Data Register 23	SEG23	8	8	1 or 2 PCLKB
000A 0858h	LCDC	LCD Display Data Register 24	SEG24	8	8	1 or 2 PCLKB
000A 0859h	LCDC	LCD Display Data Register 25	SEG25	8	8	1 or 2 PCLKB
000A 085Ah	LCDC	LCD Display Data Register 26	SEG26	8	8	1 or 2 PCLKB
000A 085Bh	LCDC	LCD Display Data Register 27	SEG27	8	8	1 or 2 PCLKB
000A 085Ch	LCDC	LCD Display Data Register 28	SEG28	8	8	1 or 2 PCLKB
000A 085Dh	LCDC	LCD Display Data Register 29	SEG29	8	8	1 or 2 PCLKB
000A 085Eh	LCDC	LCD Display Data Register 30	SEG30	8	8	1 or 2 PCLKB
000A 085Fh	LCDC	LCD Display Data Register 31	SEG31	8	8	1 or 2 PCLKB
000A 0860h	LCDC	LCD Display Data Register 32	SEG32	8	8	1 or 2 PCLKB
000A 0861h	LCDC	LCD Display Data Register 33	SEG33	8	8	1 or 2 PCLKB
000A 0862h	LCDC	LCD Display Data Register 34	SEG34	8	8	1 or 2 PCLKB
000A 0863h	LCDC	LCD Display Data Register 35	SEG35	8	8	1 or 2 PCLKB
000A 0864h	LCDC	LCD Display Data Register 36	SEG36	8	8	1 or 2 PCLKB
000A 0865h	LCDC	LCD Display Data Register 37	SEG37	8	8	1 or 2 PCLKB
000A 0866h	LCDC	LCD Display Data Register 38	SEG38	8	8	1 or 2 PCLKB
000A 0867h	LCDC	LCD Display Data Register 39	SEG39	8	8	1 or 2 PCLKB
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	1 or 2 PCLKB
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	1 or 2 PCLKB
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	1 or 2 PCLKB
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Time Register	CTSUSST	8	8	1 or 2 PCLKB
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	1 or 2 PCLKB
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	1 or 2 PCLKB
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	1 or 2 PCLKB
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	1 or 2 PCLKB
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	1 or 2 PCLKB
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	1 or 2 PCLKB
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	1 or 2 PCLKB
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	1 or 2 PCLKB

Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports P16, P17, port PA6, port PB0 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports P02, P04, P07, ports P10 to P15, ports P20 to P27, ports P30 to P32, P35, ports P50 to P56, ports PA0 to PA5, PA7 ports PB1 to PB7, ports PC0 to PC7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7, port PH7, ports PJ0*1, PJ2*1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	All pins	V_{IL}	–0.3	—	VCC × 0.2		
	All pins	ΔV_T	VCC × 0.01	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	XTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		AVCC0 × 0.7	—	AVCC0 + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	XTAL (external clock input)		–0.3	—	VCC × 0.2		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		–0.3	—	AVCC0 × 0.3		

Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports PJ0 and PJ2 multiplexed with DA0 and DA1 as general I/O ports, make sure that VCC ≤ AVCC0.

Table 5.5 DC Characteristics (3)

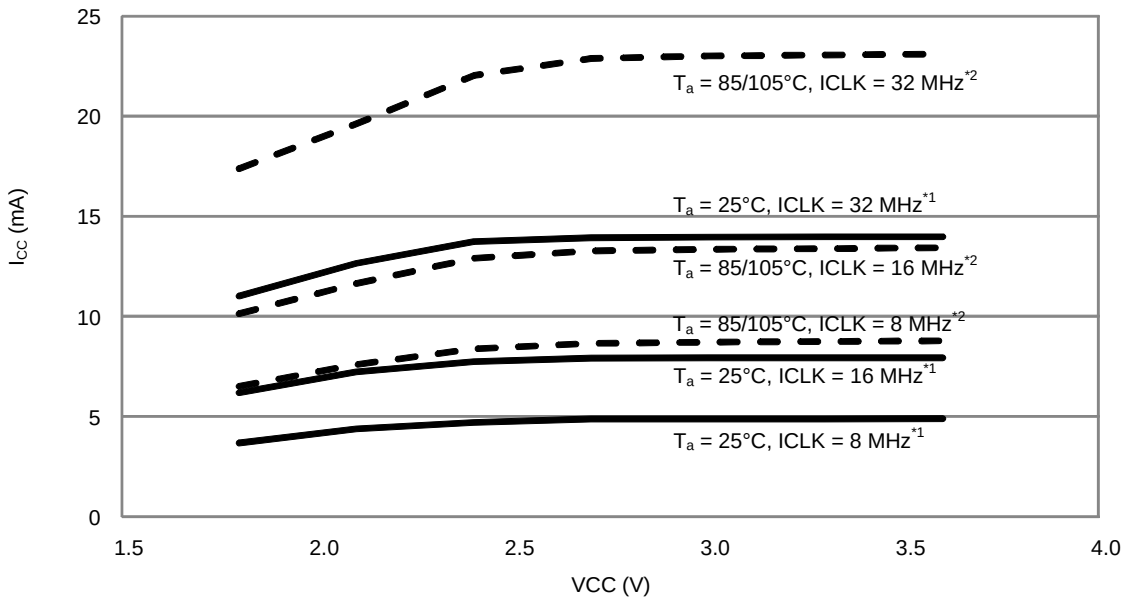
Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port P35, port PH7	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, 5.8 V
	Pins other than above		—	—	1.0		V_{in} = 0 V, VCC
Input capacitance	All input pins (except for port P16, port P35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	V_{in} = 0 V Frequency: 1 MHz T_a = 25°C
	Port P16, port P35, USB0_DM, USB0_DP		—	—	30		

Table 5.6 DC Characteristics (4)

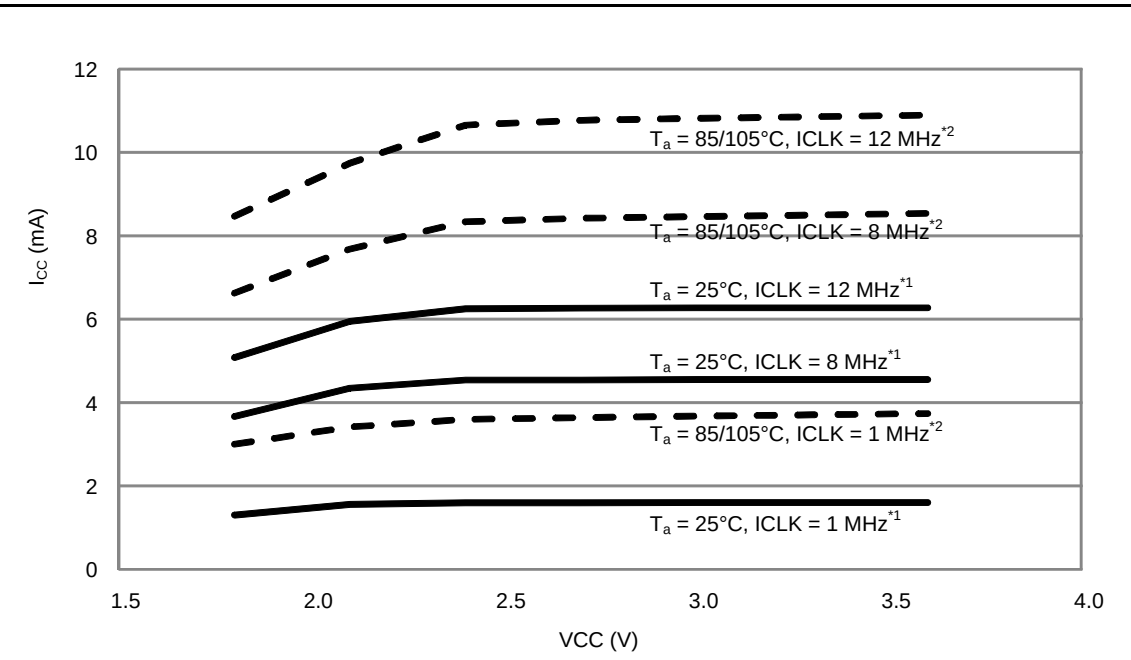
Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for ports P35, PH7)	R_U	10	20	100	kΩ	V_{in} = 0 V



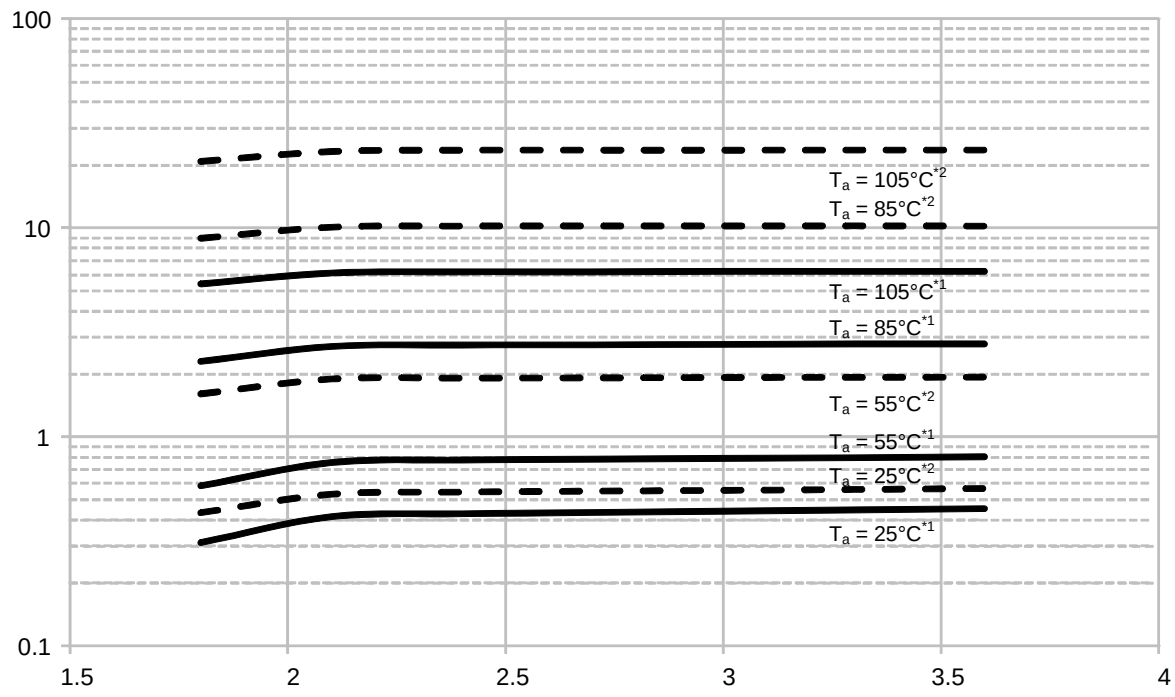
Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



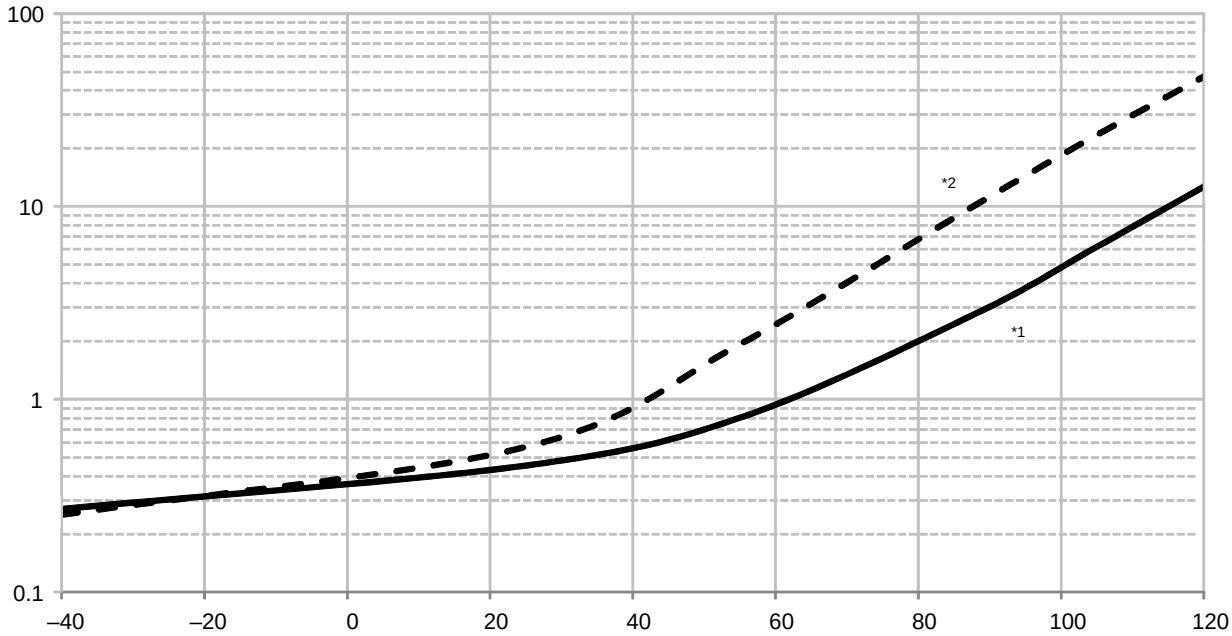
Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.7 to Figure 5.10 show the characteristics of general ports (except for the RIIC output pin, ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7).

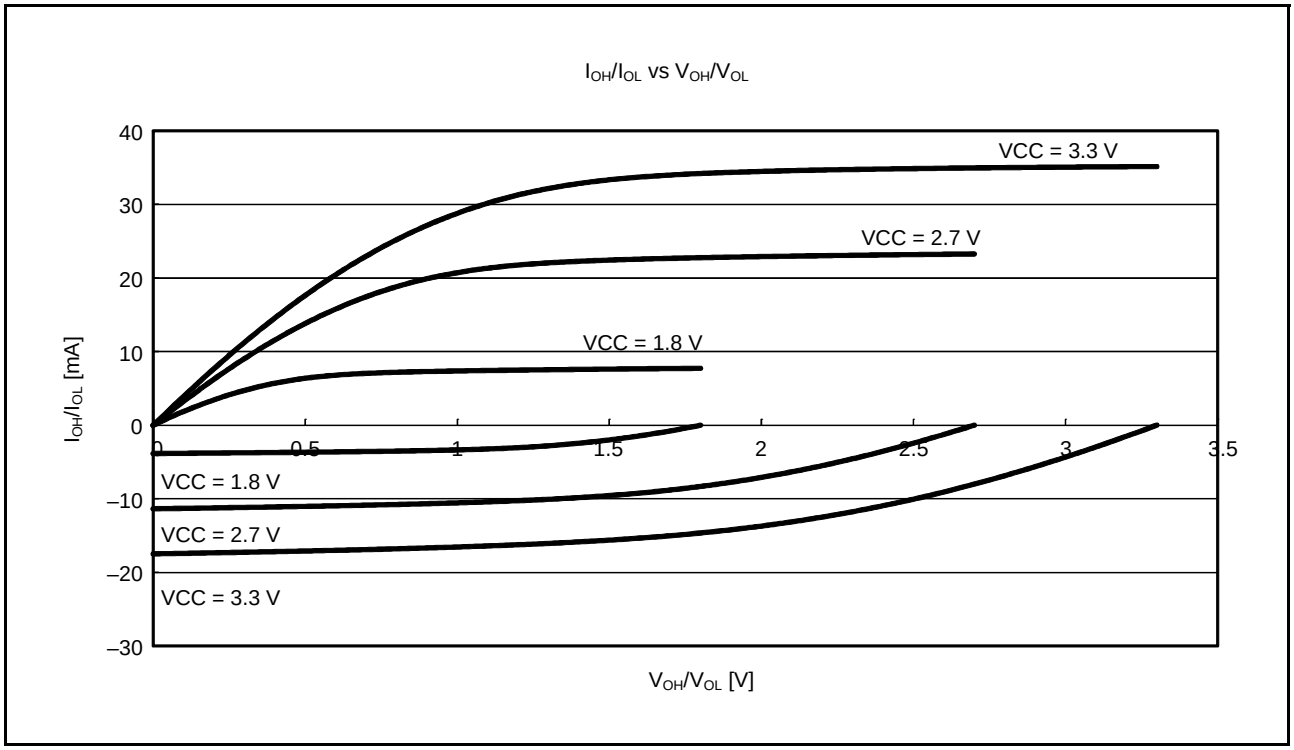


Figure 5.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of General Ports (Except for RIIC Output Pin, Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7) at T_a = 25°C (Reference Data)

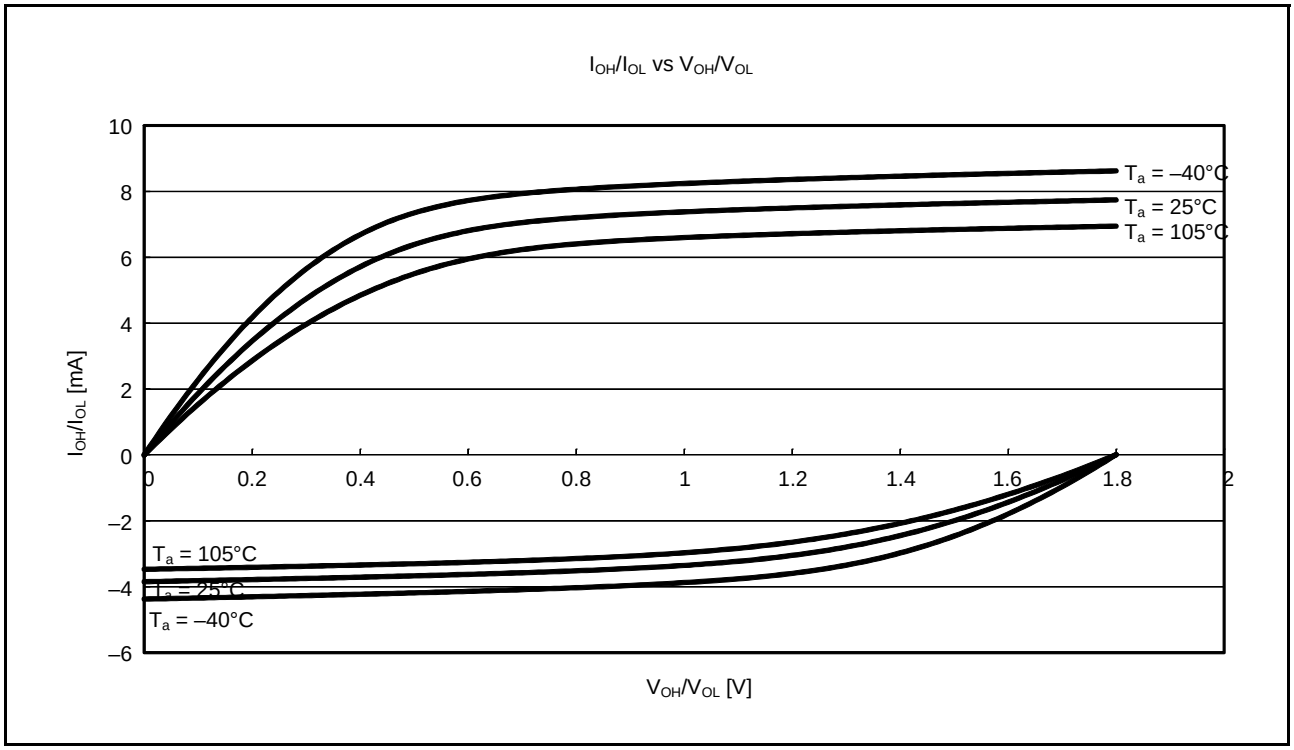


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for RIIC Output Pin, Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7) at VCC = 1.8 V (Reference Data)

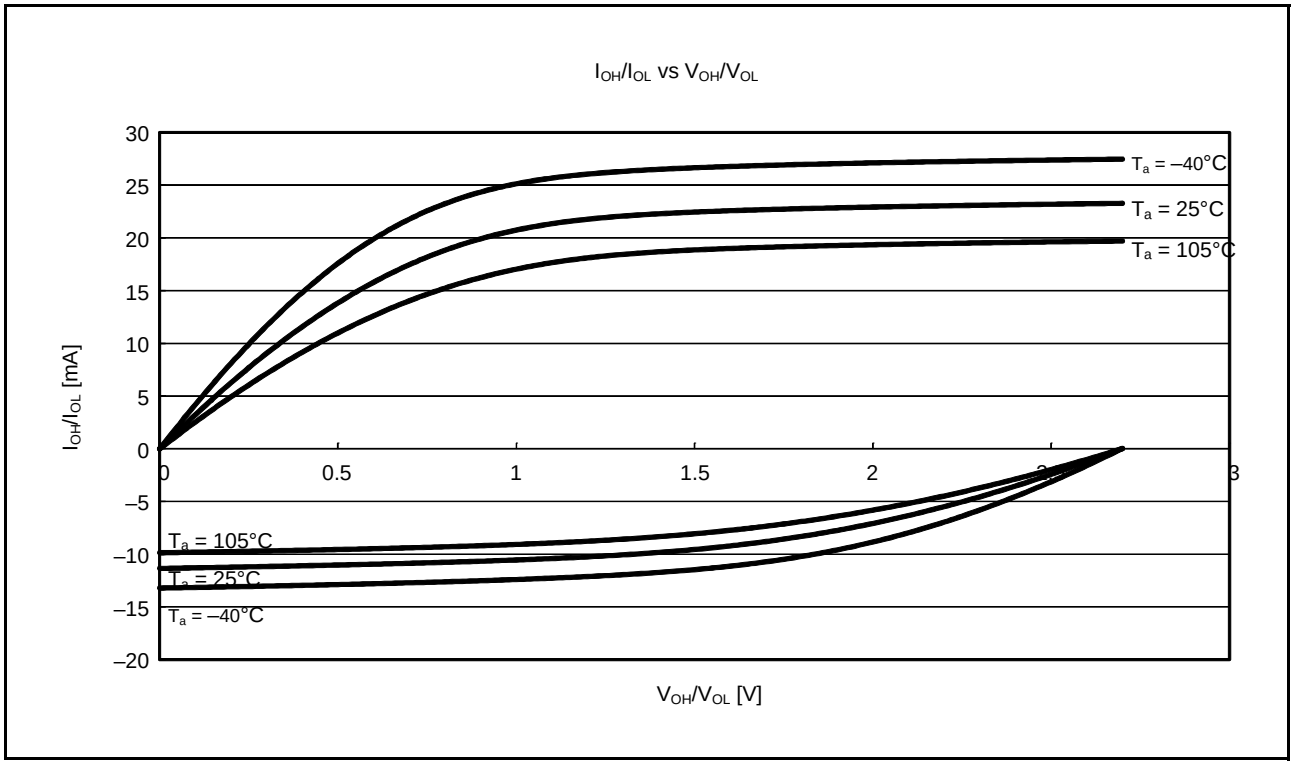


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for RIIC Output Pin, Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7) at VCC = 2.7 V (Reference Data)

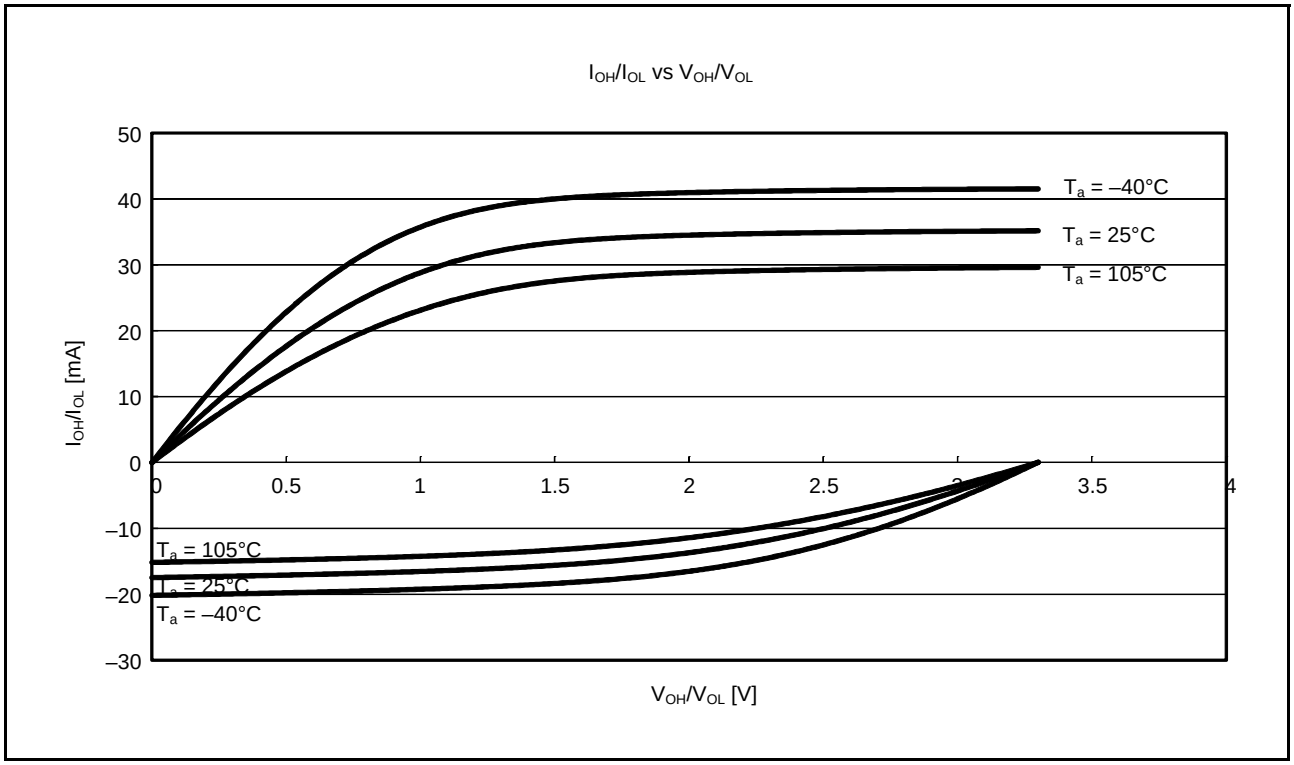


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for RIIC Output Pin, Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7) at VCC = 3.3 V (Reference Data)

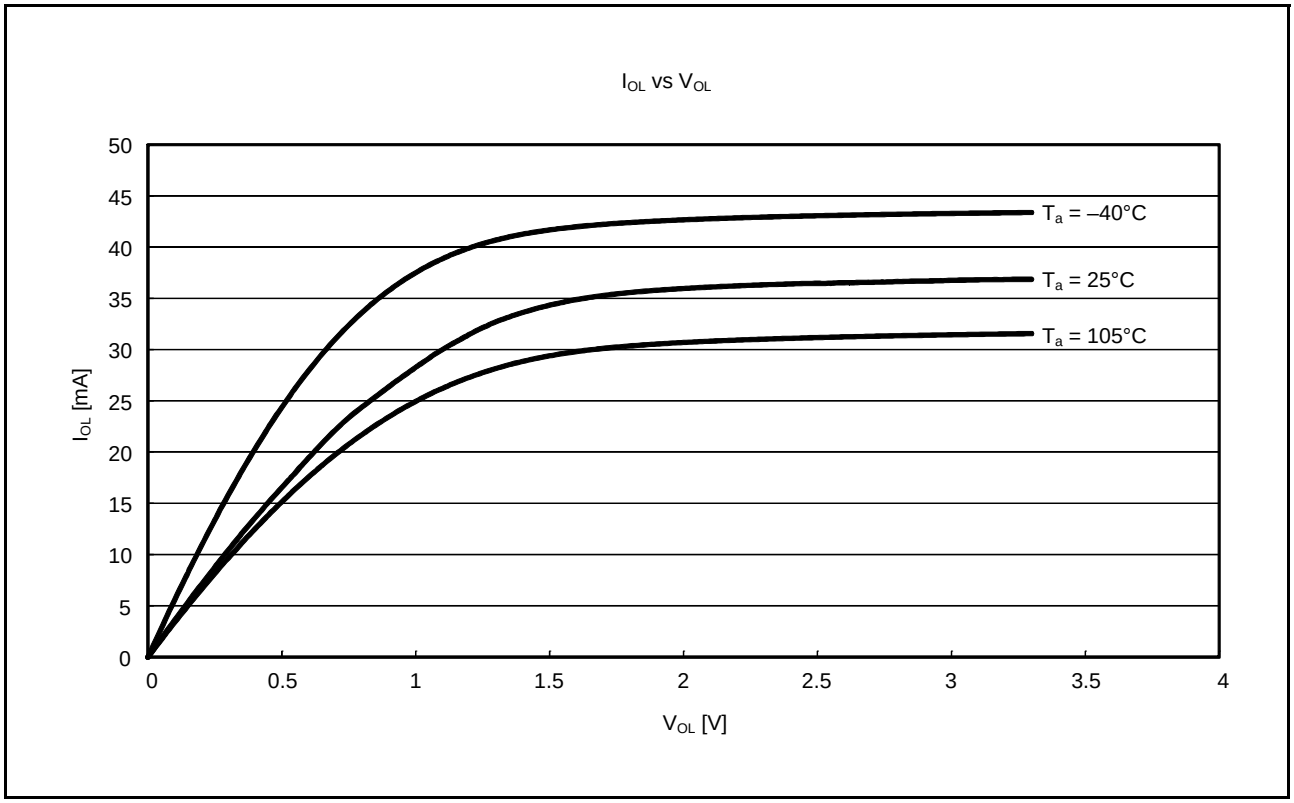


Figure 5.13 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

Table 5.22 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
XTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.18
XTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
XTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
XTAL external clock rising time		t_{Xr}	—	—	5	ns	
XTAL external clock falling time		t_{Xf}	—	—	5	ns	
XTAL external clock input wait time*1		t_{EXWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	2.4 ≤ VCC ≤ 3.6	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.19
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.20
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.21
HOCO clock oscillation frequency		f_{HOCO}	31.52	32	32.48	MHz	T_a = –40 to 85°C
			31.68	32	32.32		T_a = –20 to 85°C
			31.36	32	32.64		T_a = –40 to 105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	56	μs	Figure 5.23
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	32	—	48	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.25

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 3.6 V when the PLL is used.

Note 4. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Reference value when a 32.768-kHz resonator is used.

Note 5. The VCC range should be 3.0 to 3.6 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz only and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

Table 5.31 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.42
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.43 to Figure 5.48
			1.8 V or above		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	3 × t_{Pcyc} + 65		
			1.8 V or above		—	3 × t_{Pcyc} +105		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/ fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, tSSLf	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.47, Figure 5.48
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

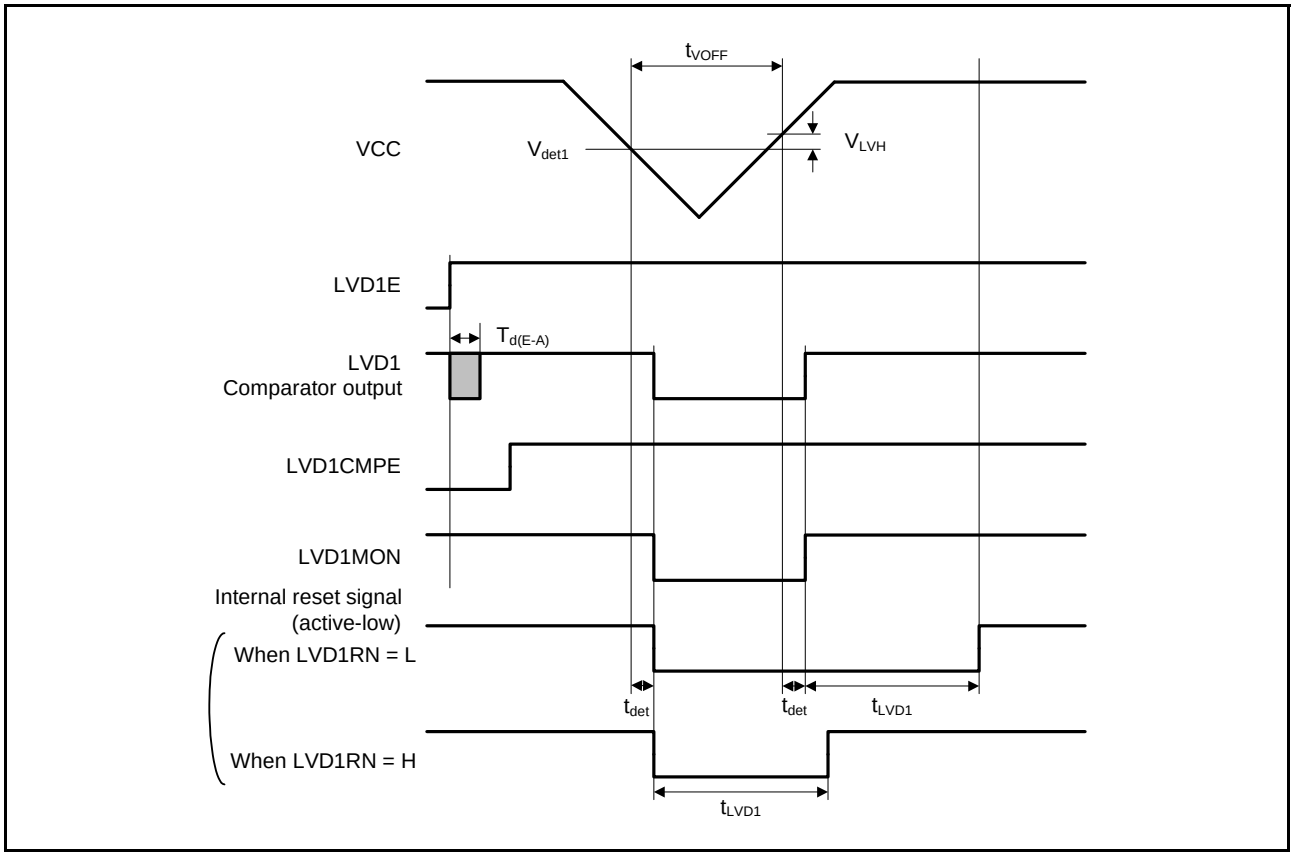


Figure 5.64 Voltage Detection Circuit Timing (V_{det1})

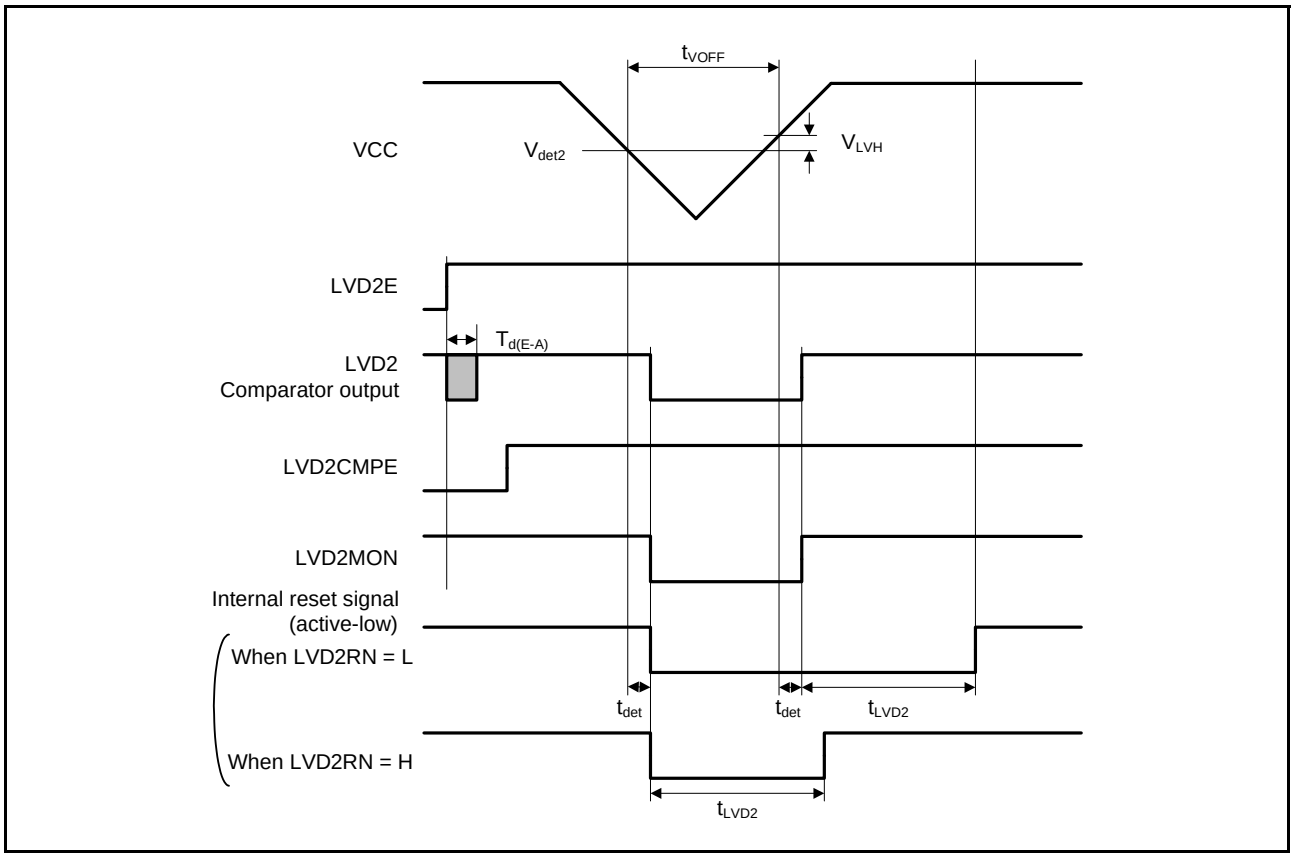


Figure 5.65 Voltage Detection Circuit Timing (V_{det2})

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.