Renesas Electronics America Inc - R5F51135ADFM#3A Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51135adfm-3a

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPI)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	USB 2.0 host/function module (USBc)	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (ON-The-Go) is supported. • Isochronous transfer is supported. • BC (Battery Charger) is supported.
	Serial Sound Interface (SSI)	• 1 channel • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
LCD controller/driver (LCDC)		• Internal voltage boosting method, capacitor split method, and external resistance division method are switchable. • Segment signal output × common signal output: 40 × 4, 36 × 8
12-bit A/D converter (S12ADb)		• 1 unit (1 unit × 17 channels) • 12-bit resolution • Minimum conversion time: 1.0 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Double trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
12-bit D/A converter (R12DAA)		• 2 channels • 12-bit resolution • Output voltage: 0.35 to AVCC - 0.47 V
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU)		Detection pin: 12 channels (for 100 pins only)
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz
Supply current		3.6 mA at 32 MHz (typ.)
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-A) 14 × 14 mm, 0.50 mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65 mm pitch 64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.50 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

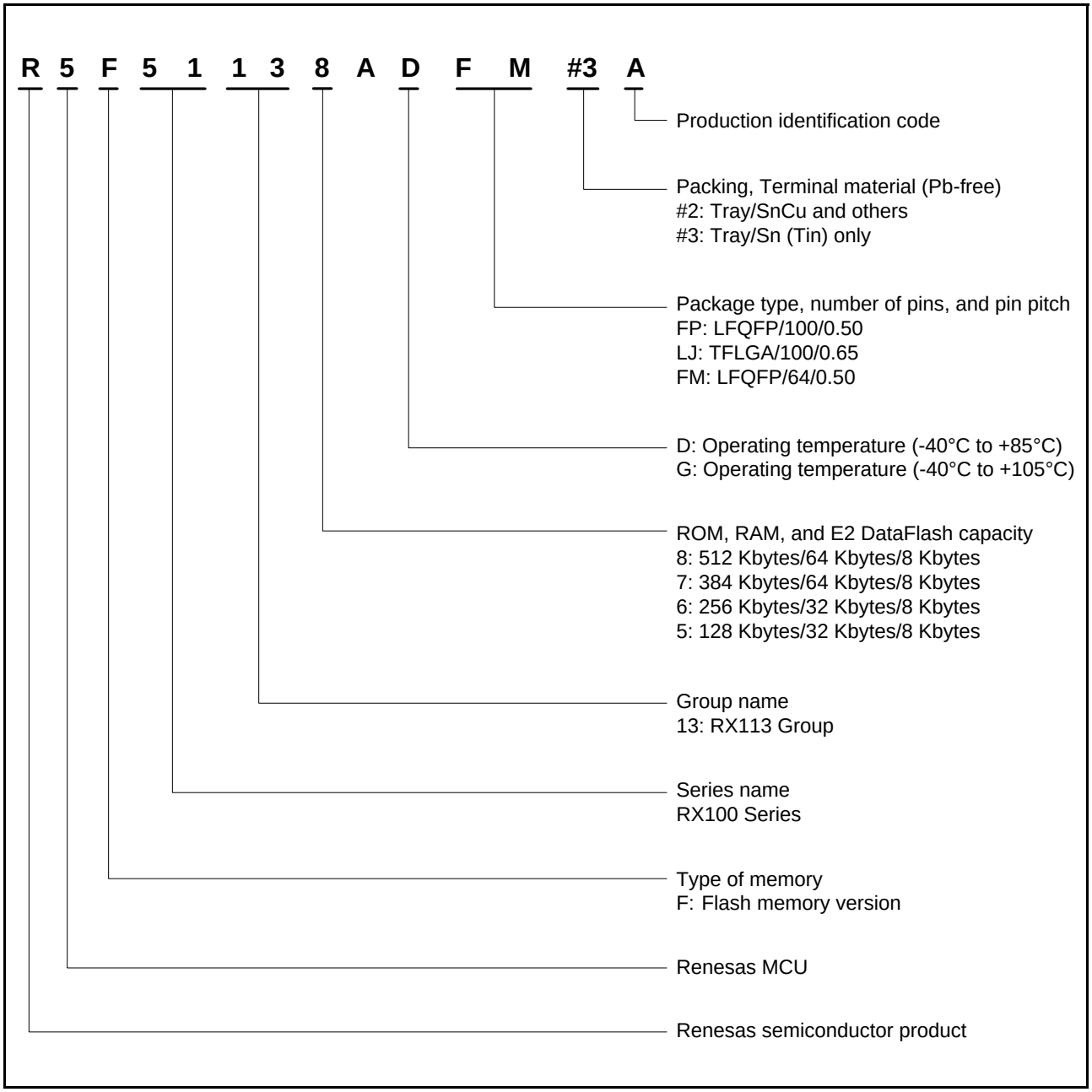


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

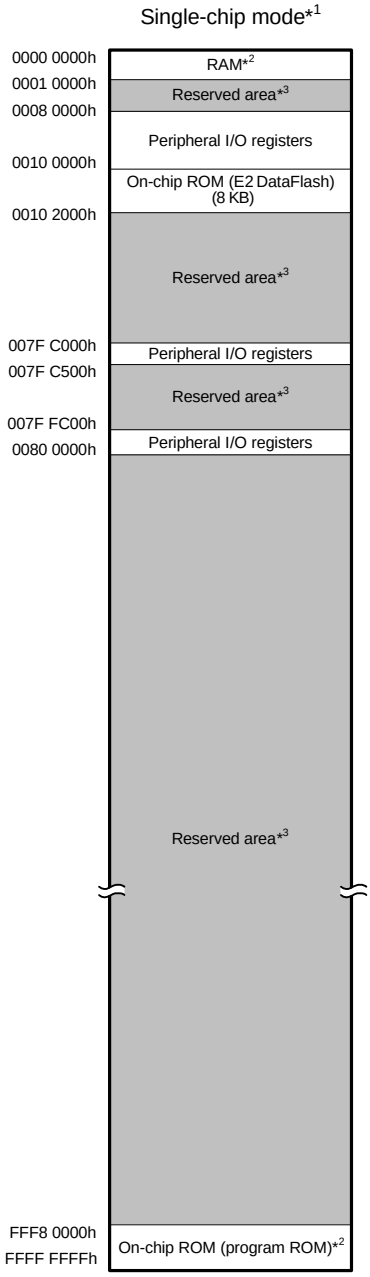
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
36		P11	MTIC5U/POE0#	RXD12/RXDX12/SMISO12/ SSCL12/ RXD0/SMISO0/SSCL0	SEG02	IRQ7
37		P10	MTIC5V/POE1#	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/TXD0/SMOSI0/SSDA0	SEG03	IRQ6
38		P56	MTIOC1A/MTIC5W/ POE2#	TXD1/SMOSI1/SSDA1	SEG04	IRQ5
39		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
40		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
41		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
42		P50	MTIOC2A	MOSIA/TXD2/SMOSI2/SSDA2	SEG08	
43		P55	MTIOC4D/TMO3		VL1	
44		P54	MTIOC4B/TMCI1		VL2	
45		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
46		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
47		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
48		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	
50		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
51		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/ COM4	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
55		PB5	MTIOC1B/MTIOC2A/ POE1#/TMRI1	SCK9/SSISCK0	SEG13/ COM6	
56		PB4		CTS9#/RTS9#/SS9#	SEG14	
57		PB3	MTIOC0A/MTIOC3B/ MTIOC4A/POE3#/TMO0	SCK6/AUDIO_MCLK/ USB0_OVRCURA	SEG15/ COM7	
58		PB2		CTS6#/RTS6#/SS6#	SEG16	
59		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6/SSIWS0	SEG17	IRQ4
60	VCC					
61		PB0	MTIOC0C/MTIC5W/ RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/ SSCL6		IRQ2/ADTRG0#
62	VSS					
63		PA6	MTIC5V/MTCLKB/ MTIOC2A/POE2#/TMCI3	CTS5#/RTS5#/SS5#/SDA0/MOSIA/ RXD8/SMISO8/SSCL8		IRQ3
64		PA7		TXD8/SMOSI8/SSDA8	SEG18	
65		PA5		SCK8	SEG19	
66		PA4	MTIOC2B/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0/CTS8#/RTS8#/SS8#	SEG20	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTIOC1B/ MTCLKD/POE0#	RXD5/SMISO5/SSCL5/IRRXD5/ MISOA	SEG21	IRQ6/CMPB1

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
A1		P02	MTIOC0D/POE3#/TMRI3	RXD6/SMISO6/SSCL6	TS2	
A2		P07		TXD6/SMOSI6/SSDA6	TS0	ADTRG0#
A3	AVCC0					
A4	AVSS0					
A5		P44*2				AN004
A6		P92*2				AN021
A7		PD3	POE8#		SEG36	IRQ3
A8		PE6			SEG34	IRQ6/AN014
A9		PE7			SEG33	IRQ7/AN015/ CMPOB0
A10		PE0	MTIOC2A/POE3#	SCK12/CTS9#/RTS9#/SS9#/ SSISCK0	SEG32	IRQ0/AN008
B1		P25	MTIOC4C/MTCLKB		TS4	ADTRG0#
B2		P04	MTIOC0A/POE2#/TMCI3	SCK6	TS1	
B3		PJ2				DA1
B4	VREFL0	PJ7*2				
B5		P90*2				AN005
B6		PD0			SEG39	IRQ0
B7		PD4	POE3#		SEG35	IRQ4
B8		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12/SSIRXD0	SEG30	IRQ7/AN010/ CVREFB0
B9		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/SSITXD0	SEG31	IRQ1/AN009/ CMPB0
B10		PE3	MTIOC0A/MTIOC1B/ MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA/ SCK9/AUDIO_MCLK	SEG29	IRQ3/AN011
C1		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	TS3	
C2		P24	MTIOC4A/MTCLKA/ TMRI1		TS5	
C3	VREFH0	PJ6*2				
C4	VREFH	P41*2				AN001
C5	VREFL	P42*2				AN002
C6		P91*2				AN007
C7		PD1	MTIOC4B		SEG38	IRQ1
C8		PD2	MTIOC4D		SEG37	IRQ2
C9		PE5	MTIOC2B/MTIOC4C	MISOA/TXD9/SMOSI9/SSDA9	SEG27	IRQ5/AN013/ CMPOB1
C10		PE4	MTIOC1A/MTIOC3A/ MTIOC4D	MOSIA/RXD9/SMISO9/SSCL9/ SSIWS0	SEG28	IRQ4/AN012
D1		P22	MTIOC3B/MTCLKC/ TMO0	SCK0	TS7	
D2		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	TS6	
D3		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	TS8	
D4		PJ0				DA0
D5		P43*2				AN003
D6		P46*2				AN006
D7		PF6	MTIOC3C		SEG26	
D8		PF7	MTIOC3A		SEG25	

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
D9		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	SEG23	
D10		PA0	MTIOC4A	SSLA1	SEG24	CACREF
E1		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	CAPH	IRQ0
E2		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	CAPL	IRQ1
E3		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/TXD6/SMOSI6/ SSDA6	TSCAP	
E4		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	TS9	
E5		P40*2				AN000
E6		PA2		RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	SEG22	
E7		PA4	MTIOC2B/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0/CTS8#/RTS8#/SS8#	SEG20	IRQ5/CVREFB1
E8		PA5		SCK8	SEG19	
E9		PA3	MTIOC0D/MTIOC1B/ MTCLKD/POE0#	RXD5/SMISO5/SSCL5/IRRXD5/ MISOA	SEG21	IRQ6/CMPB1
E10	VSS					
F1	XCOUT					
F2	UPSEL	P35				NMI
F3	RES#					
F4		P27	MTIOC2B/TMCI3	SCK12/SCK1/RXD6/SMISO6/ SSCL6	TS10	IRQ3/ ADTRG0#/ CACREF/ CMPA2
F5		P56	MTIOC1A/MTIC5W/ POE2#	TXD1/SMOSI1/SSDA1	SEG4	IRQ5
F6		PB4		CTS9#/RTS9#/SS9#	SEG14	
F7		PA7		TXD8/SMOSI8/SSDA8	SEG18	
F8		PB0	MTIOC0C/MTIC5W/ RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/ SSCL6		IRQ2/ADTRG0#
F9		PA6	MTIC5V/MTCLKB/ MTIOC2A/POE2#/TMCI3	CTS5#/RTS5#/SS5#/SDA0/MOSIA/ RXD8/SMISO8/SSCL8		IRQ3
F10	VCC					
G1	XCIN	PH7				
G2	UB#	P14	MTIOC0A/MTIOC3A/ MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA0/ TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA		IRQ4
G3		P12	TMCI1	SCK12/SCK0	SEG01	IRQ2
G4	MD					FINED
G5		P10	MTIC5V/POE1#	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/TXD0/SMOSI0/SSDA0	SEG03	IRQ6
G6		P50	MTIOC2A	MOSIA/TXD2/SMOSI2/SSDA2	SEG08	
G7		PB5	MTIOC1B/MTIOC2A/ POE1#/TMRI1	SCK9/SSISCK0	SEG13/ COM6	
G8		PB2		CTS6#/RTS6#/SS6#	SEG16	
G9		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6/SSIWS0	SEG17	IRQ4
G10		PB3	MTIOC0A/MTIOC3B/ MTIOC4A/POE3#/TMO0	SCK6/AUDIO_MCLK/ USB0_OVRCURA	SEG15/ COM7	



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh		

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map

Table 4.1 List of I/O Registers (Address Order) (2/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8	2 ICLK
0008 7325h	ICU	Interrupt Source Priority Register 037	IPR037	8	8	2 ICLK
0008 7326h	ICU	Interrupt Source Priority Register 038	IPR038	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Ah	ICU	Interrupt Source Priority Register 058	IPR058	8	8	2 ICLK
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 735Ah	ICU	Interrupt Source Priority Register 090	IPR090	8	8	2 ICLK
0008 735Ch	ICU	Interrupt Source Priority Register 092	IPR092	8	8	2 ICLK
0008 735Dh	ICU	Interrupt Source Priority Register 093	IPR093	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition Mode Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Converted Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A109h	SCI8	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A10Ah	SCI8	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A10Bh	SCI8	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A10Ch	SCI8	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A500h	SSI0	Control Register	SSICR	32	32	2 or 3 PCLKB
0008 A504h	SSI0	Status Register	SSISR	32	32	2 or 3 PCLKB
0008 A510h	SSI0	FIFO Control Register	SSIFCR	32	32	2 or 3 PCLKB
0008 A514h	SSI0	FIFO Status Register	SSIFSR	32	32	2 or 3 PCLKB
0008 A518h	SSI0	Transmit FIFO Data Register	SSIFTDR	32	32	2 or 3 PCLKB
0008 A51Ch	SSI0	Receive FIFO Data Register	SSIFRDR	32	32	2 or 3 PCLKB
0008 A520h	SSI0	TDM Mode Register	SSITDMR	32	32	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (21/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more
000A 0800h	LCDC	LCD mode register 0	LCDM0	8	8	1 or 2 PCLKB
000A 0801h	LCDC	LCD mode register 1	LCDM1	8	8	1 or 2 PCLKB
000A 0802h	LCDC	LCD Clock Control Register 0	LCDC0	8	8	1 or 2 PCLKB
000A 0803h	LCDC	LCD Boost Level Control Register	VLCD	8	8	1 or 2 PCLKB

Table 5.7 DC Characteristics (5) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.6	—	mA	
				ICLK = 16 MHz		2.4	—		
				ICLK = 8 MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		14.0	—		
				ICLK = 16 MHz		7.9	—		
				ICLK = 8 MHz		4.9	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	30.0		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—		
				ICLK = 16 MHz		1.5	—		
				ICLK = 8 MHz		1.3	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		8.2	—		
				ICLK = 16 MHz		4.8	—		
				ICLK = 8 MHz		3.1	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		0.95	—		
				ICLK = 8 MHz		0.86	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		6.4	—		
				ICLK = 16 MHz		3.8	—		
				ICLK = 8 MHz		2.4	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.1	—	mA	
				ICLK = 8 MHz		1.4	—		
				ICLK = 1 MHz		0.77	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		6.3	—		
				ICLK = 8 MHz		4.6	—		
				ICLK = 1 MHz		1.6	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	14.2		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.90	—		
				ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.9	—		
				ICLK = 8 MHz		2.9	—		
				ICLK = 1 MHz		1.4	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.1	—		
				ICLK = 8 MHz		0.63	—		
				ICLK = 1 MHz		0.55	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.3	—		
				ICLK = 8 MHz		2.4	—		
				ICLK = 1 MHz		1.2	—		
		Increase during flash rewrite*5				2.5	—		

Table 5.22 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
XTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.18
XTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
XTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
XTAL external clock rising time		t_{Xr}	—	—	5	ns	
XTAL external clock falling time		t_{Xf}	—	—	5	ns	
XTAL external clock input wait time*1		t_{EXWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	2.4 ≤ VCC ≤ 3.6	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.19
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.20
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.21
HOCO clock oscillation frequency		f_{HOCO}	31.52	32	32.48	MHz	T_a = –40 to 85°C
			31.68	32	32.32		T_a = –20 to 85°C
			31.36	32	32.64		T_a = –40 to 105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	56	μs	Figure 5.23
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	32	—	48	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.25

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 3.6 V when the PLL is used.

Note 4. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Reference value when a 32.768-kHz resonator is used.

Note 5. The VCC range should be 3.0 to 3.6 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz only and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

5.3.4 Control Signal Timing

Table 5.29 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

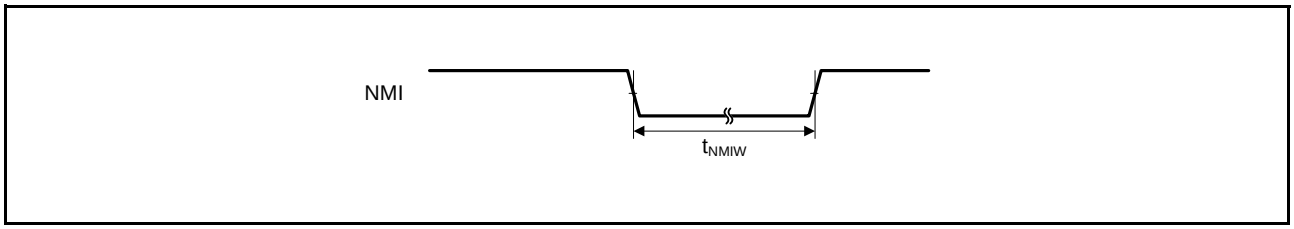


Figure 5.31 NMI Interrupt Input Timing

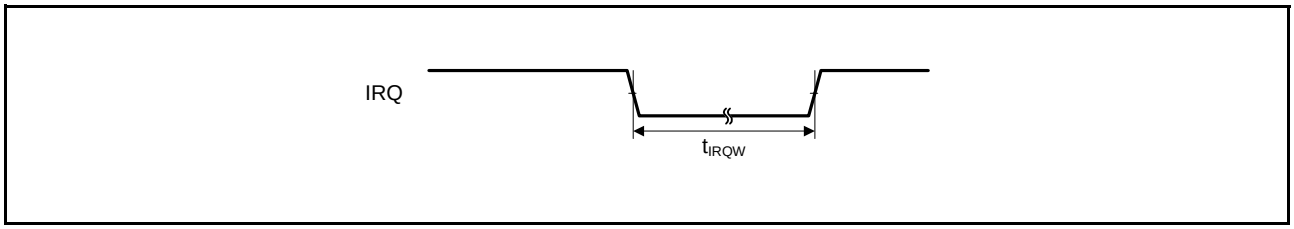


Figure 5.32 IRQ Interrupt Input Timing

5.4 USB Characteristics

Table 5.36 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 3.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V	
	Input low level voltage		V_{IL}	—	0.8	V	
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 5.54 Figure 5.55
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	—	V	
			V_{IL}	—	VCC × 0.2	V	
	VBUS (P16) input leakage current		| I_{VBUSIN} |	—	10	µA	USB0_VBUS = 5.5 V
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	USB0_DP sink current		I_{DP_SINK}	25	175	µA	
	USB0_DM sink current		I_{DM_SINK}	25	175	µA	
	DCD source current		I_{DP_SRC}	7	13	µA	
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	
	USB0_DP source current		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	USB0_DM source current		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

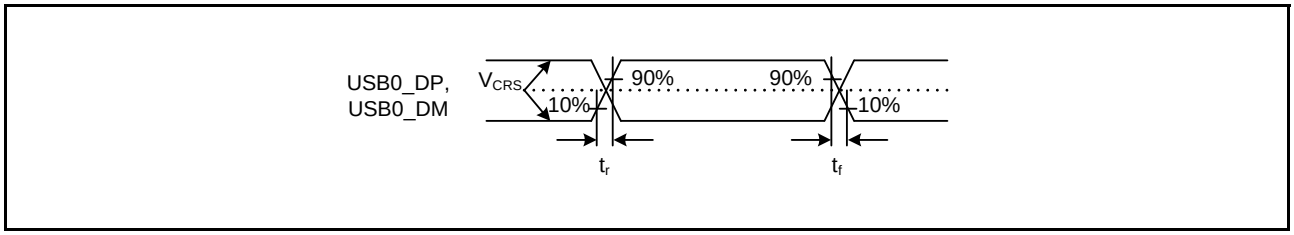


Figure 5.54 USB0_DP and USB0_DM Output Timing

Table 5.40 A/D Conversion Characteristics (4)

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
ADHVREFCNT.OCSVSEL = 1 (internal reference voltage selected as high-side reference voltage),
PJ7PFS.ASEL = 0 (AVSS0 pin selected as low-side reference power supply ground pin)
T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	2	MHz	
Resolution		—	—	12	Bit	
Internal reference voltage		1.36	1.43	1.50	V	
Conversion time*1 (Operation at PCLKD = 2 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	16 (1.5)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 02h
		17.5 (3.0)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 05h
Analog input effective range		0	—	Internal reference voltage	V	
Offset error		—	—	±24.0	LSB	
DNL differential nonlinearity error		—	±16.0	—	LSB	
INL integral nonlinearity error		—	±16.0	±32.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 5.41 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007, AN021	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN007 and AN021 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN008 to AN015		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

Table 5.42 A/D Internal Reference Voltage Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V*1, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

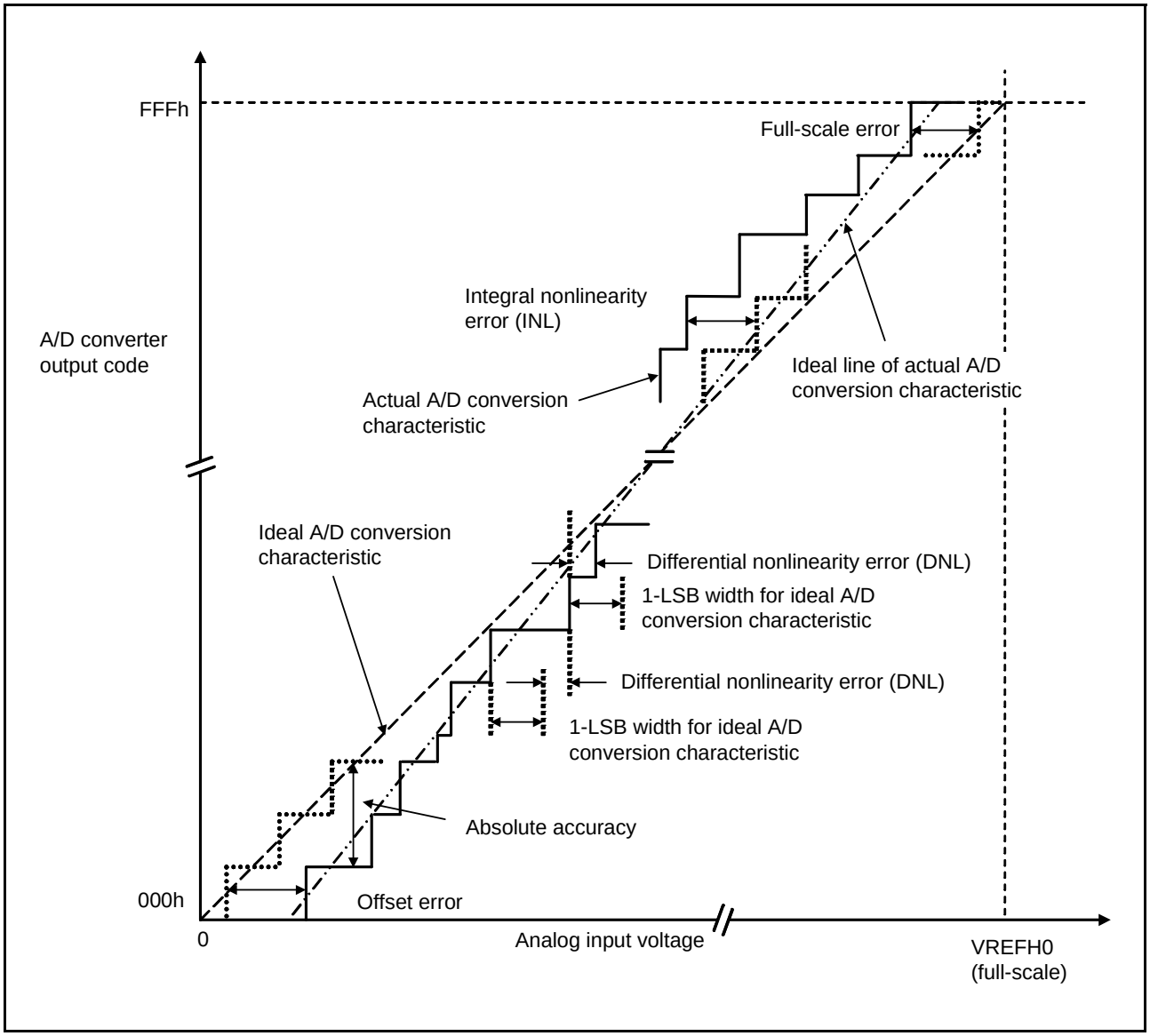


Figure 5.57 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

5.6 D/A Conversion Characteristics

Table 5.43 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, 1.8 V ≤ VREFH ≤ AVCC0, VSS = AVSS0 = VREFL = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = VREFH and VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range*1	0.35	—	VREFH	V	VREFH ≤ AVCC0 - 0.47 V
	0.35	—	AVCC0 - 0.47	V	VREFH > AVCC0 - 0.47 V
DNL differential nonlinearity error	—	±0.5	±1.0	LSB	
INL integral nonlinearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±20	mV	
Full-scale error	—	—	±20	mV	
Output resistance	—	75	—	Ω	
Conversion time	—	—	30	μs	

Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports J0 and J2 as DA0 and DA1 output, make sure that VCC ≥ D/A output voltage.

Table 5.44 D/A Conversion Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 = VREFH ≤ 3.6 V, VSS = AVSS0 = VREFL = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = AVCC0 and AVSS0 selected

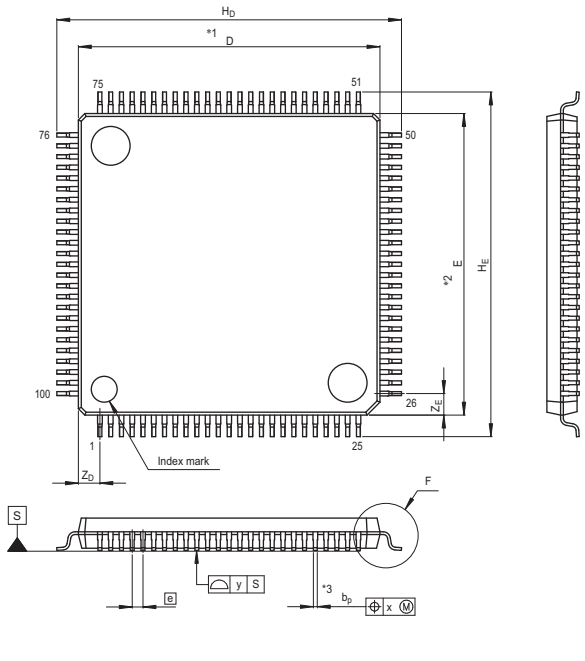
Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range*1	0.35	—	AVCC0 - 0.47	V	
DNL differential nonlinearity error	—	±0.5	±2.0	LSB	
INL integral nonlinearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±30	mV	
Full-scale error	—	—	±30	mV	
Output resistance	—	75	—	Ω	
Conversion time	—	—	30	μs	

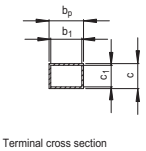
Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports J0 and J2 as DA0 and DA1 output, make sure that VCC ≥ D/A output voltage.

Appendix 1. Package Dimensions

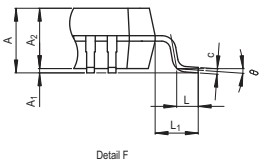
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





Terminal cross section



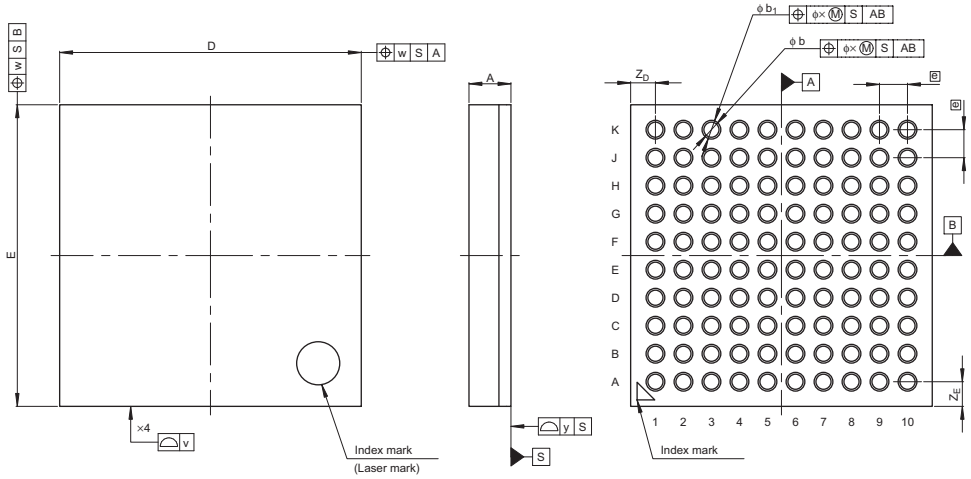
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure B 100-Pin TFLGA (PTLG0100JA-A)