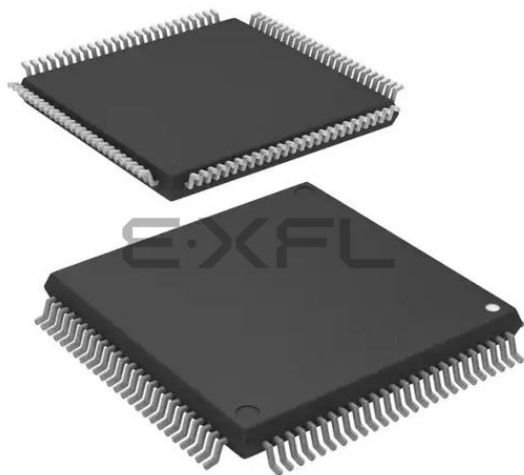




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51136adfp-3a

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 32 MHz 32-bit RX CPU - Minimum instruction execution time: One instruction per clock cycle - Address space: 4-Gbyte linear - Register set - General purpose: Sixteen 32-bit registers - Control: Eight 32-bit registers - Accumulator: One 64-bit register - Basic instructions: 73 - DSP instructions: 9 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit - On-chip divider: 32-bit ÷ 32-bit → 32 bits - Barrel shifter: 32 bits
Memory	ROM	- Capacity: 128 K /256 K /384 K /512 Kbytes 32 MHz, no-wait memory access - Programming/erasing method: - Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	- Capacity: 32 K /64 Kbytes 32 MHz, no-wait memory access
	E2 DataFlash	- Capacity: 8 Kbytes - Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	- Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator - Oscillation stop detection: Available - Clock frequency accuracy measurement circuit (CAC) - Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) - The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) - Peripheral modules run in synchronization with the PCLK: 32 MHz (at max.) - The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) - The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64).
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	- When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. - Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels - Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	- Module stop function - Three low power consumption modes - Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	- Operating power control modes - High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	- Interrupt vectors: 120 - External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) - Non-maskable interrupts: 4 (NMI pin, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDG interrupt) 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
DMA	Data transfer controller (DTCa)	- Transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Interrupts - Chain transfer function
I/O ports	General I/O ports	100-pin /64-pin - I/O: 82/46 - Input: 2/2 - Pull-up resistors: 69/38 - Open-drain outputs: 61/34 5-V tolerance: 4/4
	Event link controller (ELC)	- Event signals of 44 types can be directly connected to the module - Operations of timer modules are selectable at event input - Capable of event link operation for port B
	Multi-function pin controller (MPC)	Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	(16 bits × 6 channels) × 1 unit - Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines - Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. - Input capture function 21 output compare/input capture registers - Pulse output mode - Complementary PWM output mode - Reset synchronous PWM mode - Phase-counting mode - Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	(16 bits × 2 channels) × 2 units - Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	14 bits × 1 channel - Count clock: Dedicated low-speed on-chip oscillator for the IWDWT - Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCA)	- Clock source: Sub-clock - Calendar count mode or binary count mode selectable - Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	16 bits × 1 channel - Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDWT - Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	(8 bits × 2 channels) × 2 units - Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected - Pulse output and PWM output with any duty cycle are available - Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIE, SCIf)	8 channels (channel 0, 1, 2, 5, 6, 8, and 9: SCIE, channel 12: SCIf) - Serial communications modes: Asynchronous, clock synchronous, and smart card interface - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from MTU2 timers - Simple I²C - Simple SPI - Master/slave mode supported (SCIf only) - Start frame and information frame are included (SCIf only) - Start-bit detection in asynchronous mode: Low level or falling edge is selectable
	IrDA interface (IRDA)	1 channel (SCI5 used) - Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIIC)	1 channel - Communications formats: I²C bus format/SMBus format - Master mode or slave mode selectable - Supports fast mode

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX113 Group	
		100 Pins	64 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	
DMA	Data transfer controller	Supported	
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)	
	Port output enable 2	Supported	
	Compare match timer	2 channels × 2 units	
	Realtime clock	Supported	
	Low power timer	1 channel	
	8-bit timer	2 channels × 2 units	
	Independent watchdog timer	Supported	
Communication functions	Serial communications interfaces (SCIE) [simple I ² C, simple SPI]	7 channels (SCI0, 1, 2, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)
	IrDA interface	1 channel (SCI5)	
	Serial communications interface (SCIf) [simple I ² C, simple SPI]	1 channel (SCI12)	
	I ² C bus interface	1 channel	
	Serial peripheral interface	1 channel	
	USB 2.0 host/function module (USBc)	1 channel	
	Serial sound interface	1 channel	
12-bit A/D converter (including high-precision channels)		17 channels (9 channels)	11 channels (3 channels)
Temperature sensor		Supported	
Comparator B		2 channels	
12-bit D/A converter		2 channels	
CRC calculator		Supported	
Event link controller		Supported	
Capacitive touch sensing unit		12 channels	Not supported
LCD		40 SEG × 4 COM 36 SEG × 8 COM	20 SEG × 4 COM 16 SEG × 8 COM
Packages		100-pin LFQFP 100-pin TFLGA	64-pin LFQFP

1.3 Block Diagram

Figure 1.2 shows a block diagram.

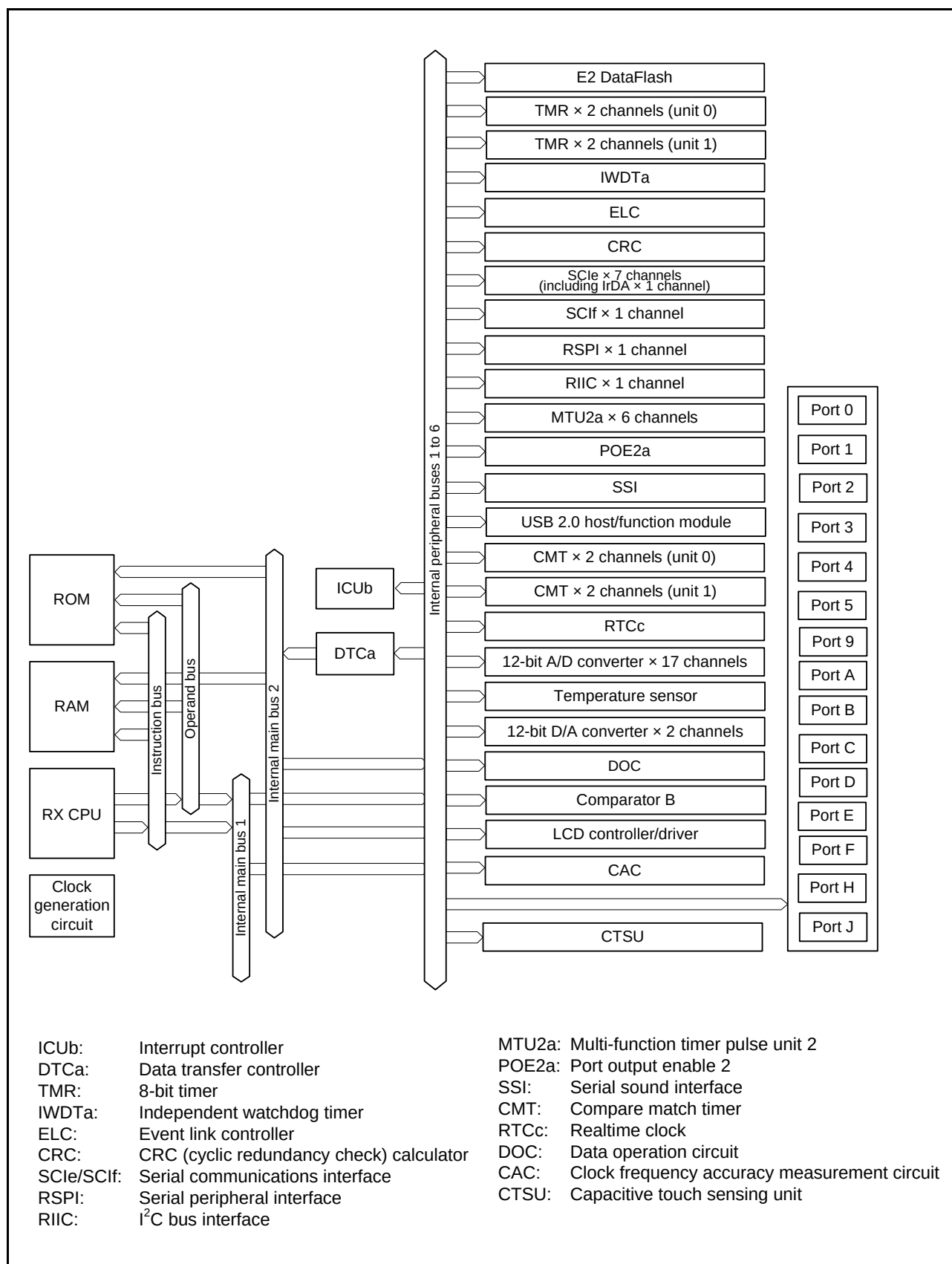


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
Clock	XTAL	Output/ Input *1	Pins for connecting a crystal. An external clock can be input through the XTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB#	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.

Table 4.1 List of I/O Registers (Address Order) (3/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I ² C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I ² C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8 *2	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I ² C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I ² C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I ² C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I ² C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB/2ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 860Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKB
0008 860Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (23/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0912h	CTSU	CTSU High-Pass Noise Spectrum Diffusion Control Register	CTSUSSC	16	16	1 or 2 PCLKB
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	1 or 2 PCLKB
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	1 or 2 PCLKB
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	1 or 2 PCLKB
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	1 or 2 PCLKB
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	1 or 2 PCLKB
007F C090h	FLASH	E2 DataFlash Control Register	DFCTL	8	8	2 or 3 FCLK
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	1 or 2 PCLKB
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	1 or 2 PCLKB
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C0B2h	FLASH	Flash Access Window Start Address Monitor	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 22.4 lists register allocation for 16-bit access in the User's Manual: Hardware.

Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCTL register. Table 30.6 lists register allocation for 16-bit access in the User's Manual: Hardware.

Table 5.27 Timing of Recovery from Low Power Consumption Modes (4)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	$t_{\text{DSL P}}$	—	2	μs	
	Middle-speed mode*3	$t_{\text{DSL P}}$	—	3	μs	
	Low-speed mode*4	$t_{\text{DSL P}}$	—	400	μs	

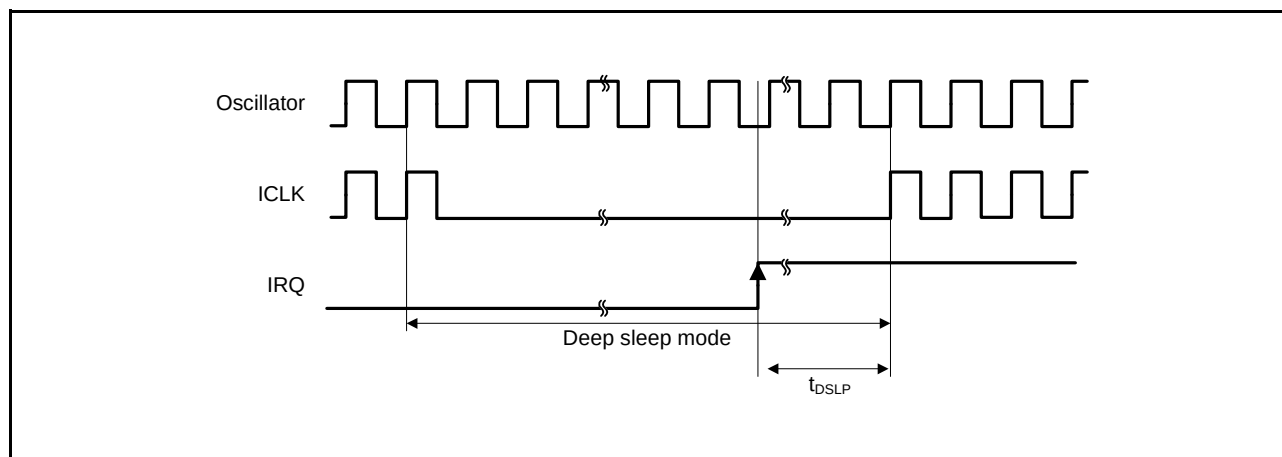
Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32.768 kHz.

**Figure 5.30 Deep Sleep Mode Recovery Timing****Table 5.28 Timing of Recovery from Low Power Consumption Modes (5)**
Operating Mode Transition TimeConditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	8 MHz	—	10	—	μs
Middle-speed operating mode	High-speed operating mode	8 MHz	—	37.5	—	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	213.62	—	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	183.11	—	μs

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Table 5.33 Timing of On-Chip Peripheral Modules (4)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL0 input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.49
	SCL0 input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL0 input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—	1000	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA0 input bus free time	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	START condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL0 input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 600$	—	ns	Figure 5.49
	SCL0 input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL0 input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—*2	300	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—*2	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA0 input bus free time	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	START condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference count clock (IIC ϕ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. The minimum t_{sr} and t_{sf} specifications for fast mode are not set.

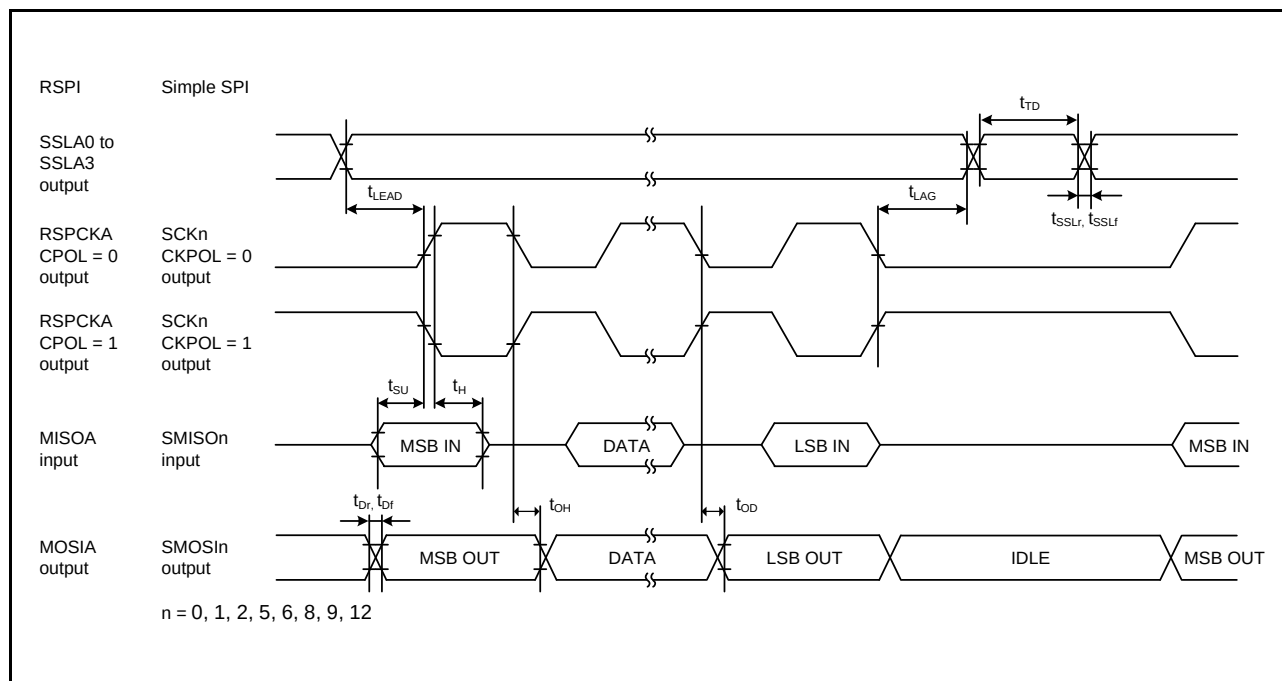


Figure 5.43 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

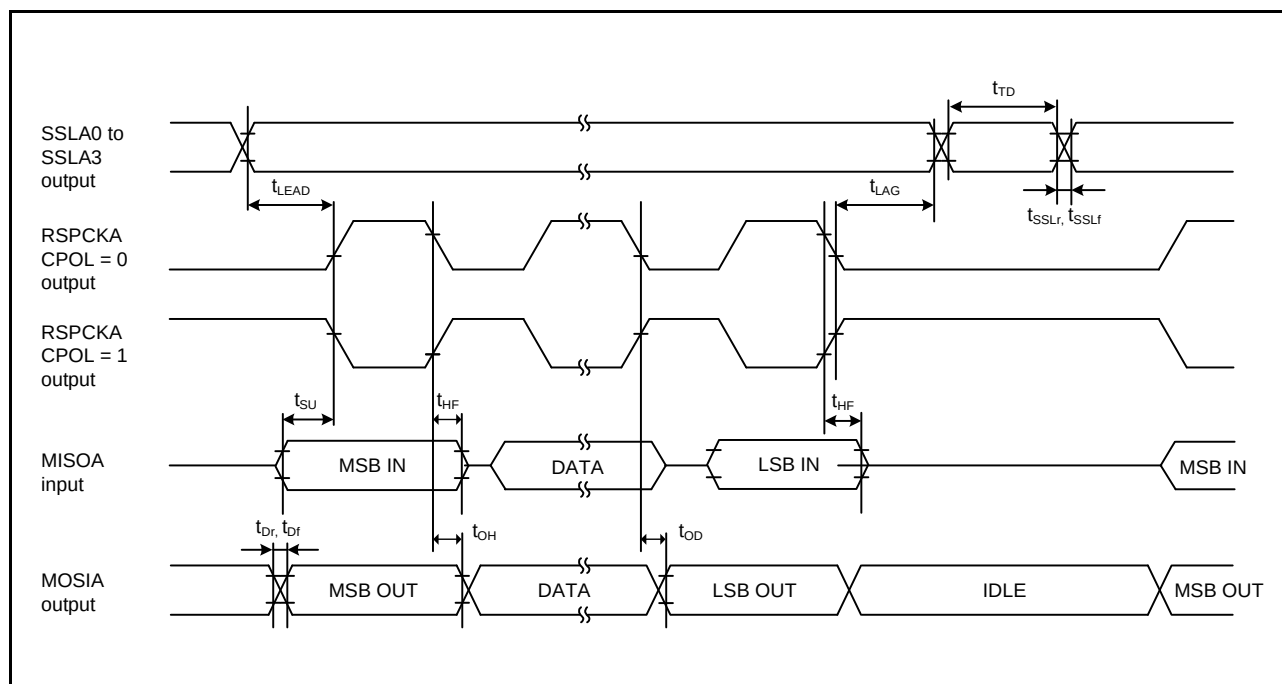


Figure 5.44 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

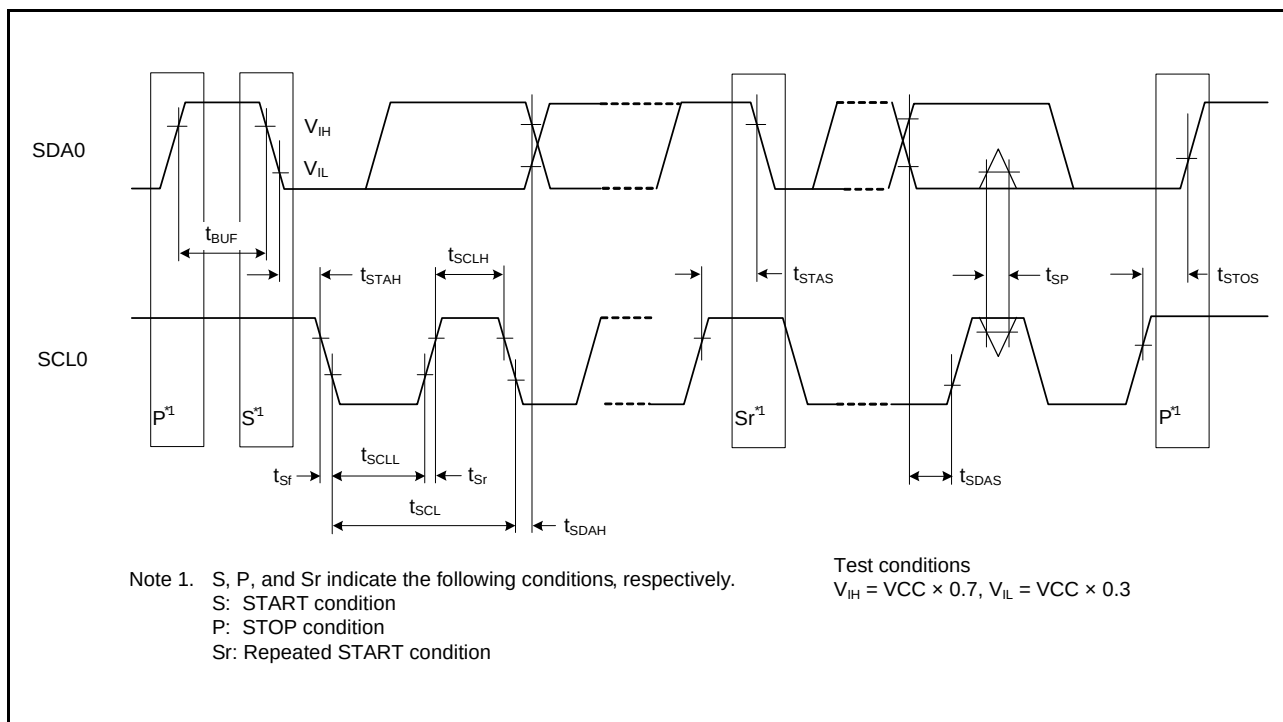


Figure 5.49 IIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

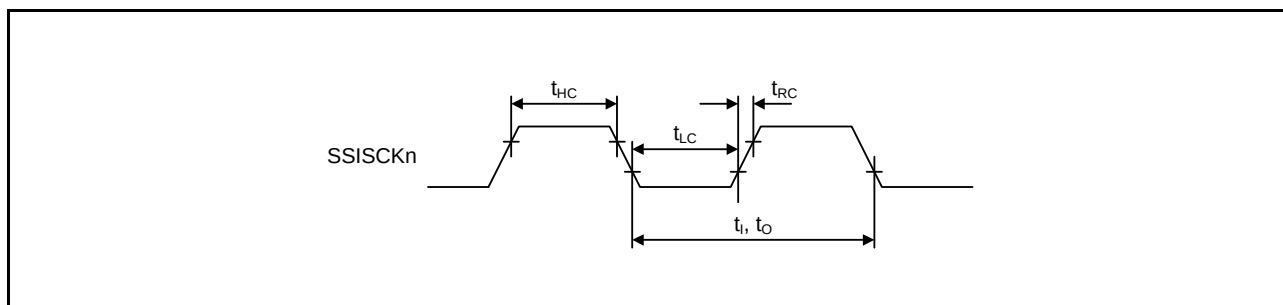


Figure 5.50 Clock Input/Output Timing

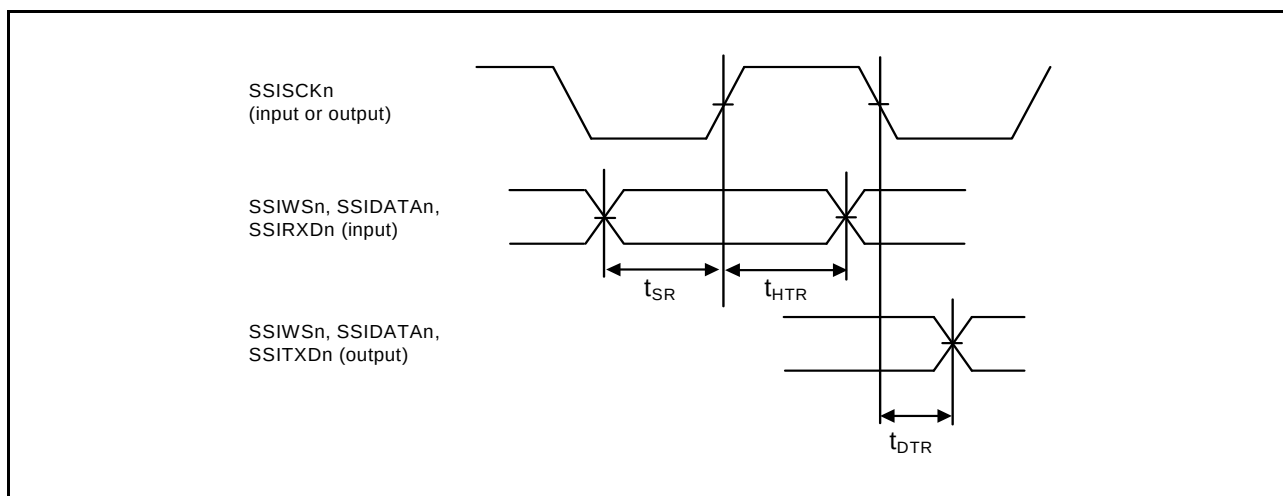


Figure 5.51 Transmission/Reception Timing (Synchronized with SSISCKn Rising Edge)

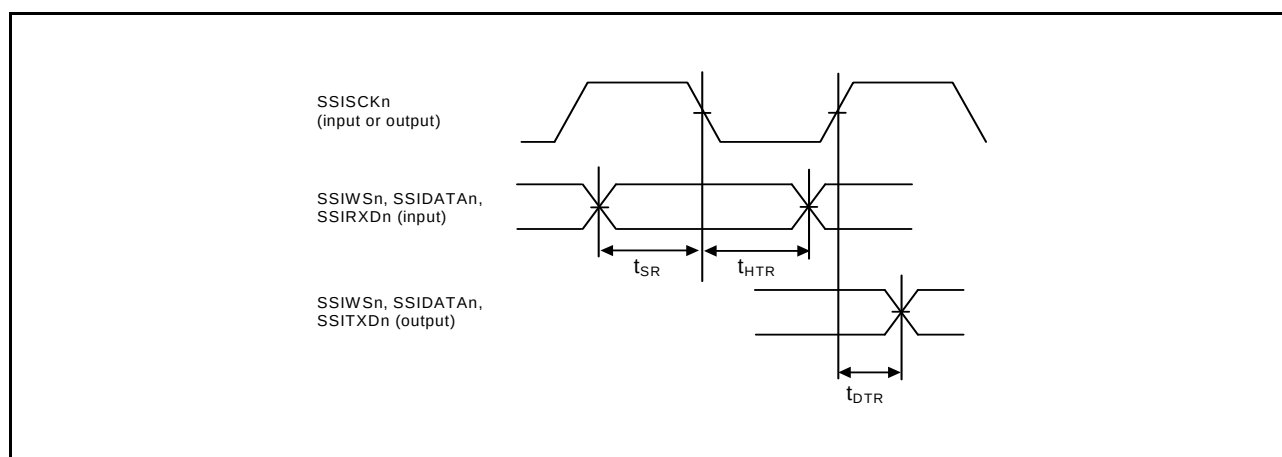


Figure 5.52 Transmission/Reception Timing (Synchronized with SSISCKn Falling Edge)

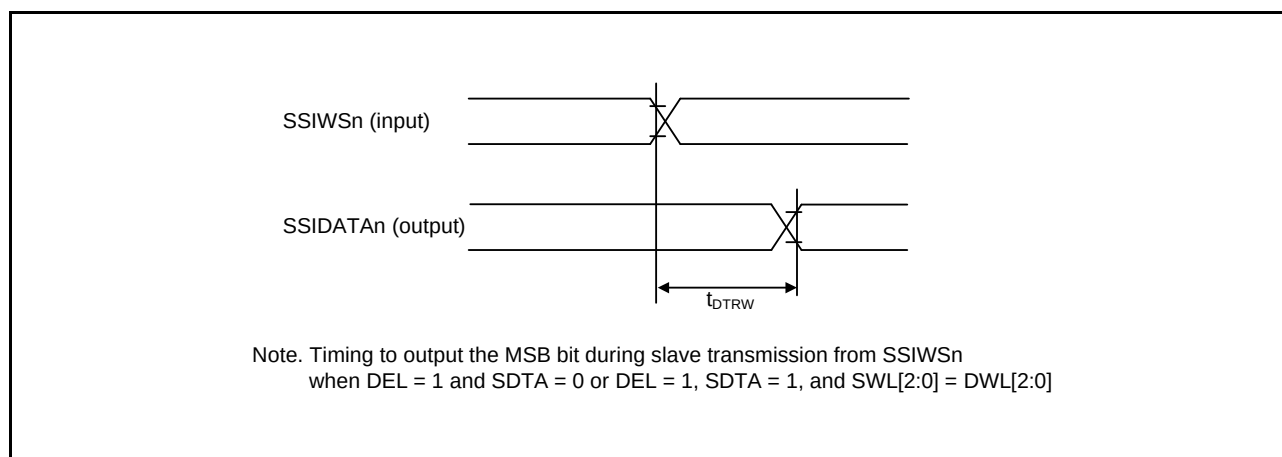


Figure 5.53 SSIDATA Output Delay After SSIWSn Changing Edge

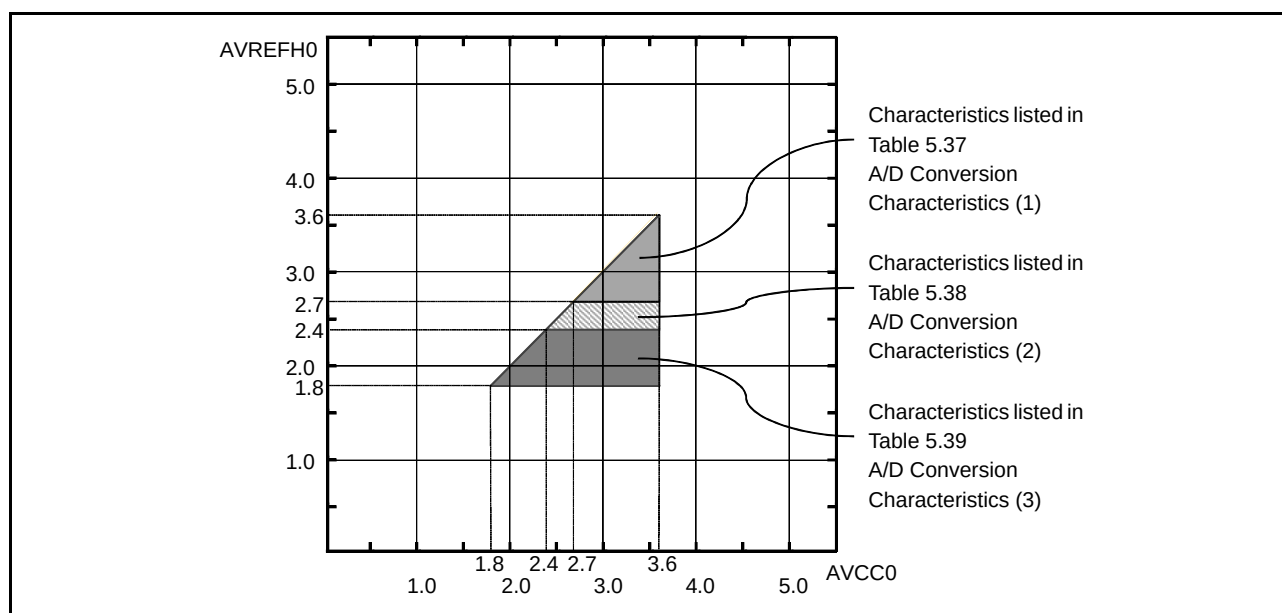


Figure 5.56 AVCC0 to AVREFH0 Voltage Range

Table 5.45 D/A Conversion Characteristics (3)

Conditions: $2.0\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.0\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
 Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential nonlinearity error	—	±2.0	±16.0	LSB	
INL integral nonlinearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	±30	mV	
Output resistance	—	75	—	Ω	
Conversion time	—	—	30	μs	

5.9 LCD Characteristics

5.9.1 External Resistance Division Method

(1) Static Display Mode

Table 5.48 LCD Characteristics

Conditions: $2.0\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.0\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	

(2) 1/2 Bias Method, 1/4 Bias Method

Table 5.49 LCD Characteristics

Conditions: $2.7\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	

(3) 1/3 Bias Method

Table 5.50 LCD Characteristics

Conditions: $2.5\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.5\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	

5.13 ROM (Flash Memory for Code Storage) Characteristics

Table 5.60 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erase cycle*1		N _{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N _{PEC}	t _{DRP}	20*2, *3	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.61 ROM (Flash Memory for Code Storage) Characteristics (2)

High-speed operating mode Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erase operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t _{P4}	—	103	931	—	52	489	μs
Erase time	1-Kbyte	t _{E1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t _{E256K}	—	407	925	—	39	457	ms
Blank check time	4-byte	t _{BC4}	—	—	48	—	—	15.9	μs
	1-Kbyte	t _{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t _{SED}	—	—	21.6	—	—	12.8	μs
Start-up area switching setting time		t _{SAS}	—	12.6	543	—	6.16	432	ms
Access window time		t _{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t _{DIS}	2	—	—	2	—	—	μs
ROM mode transition wait time 2		t _{MS}	5	—	—	5	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

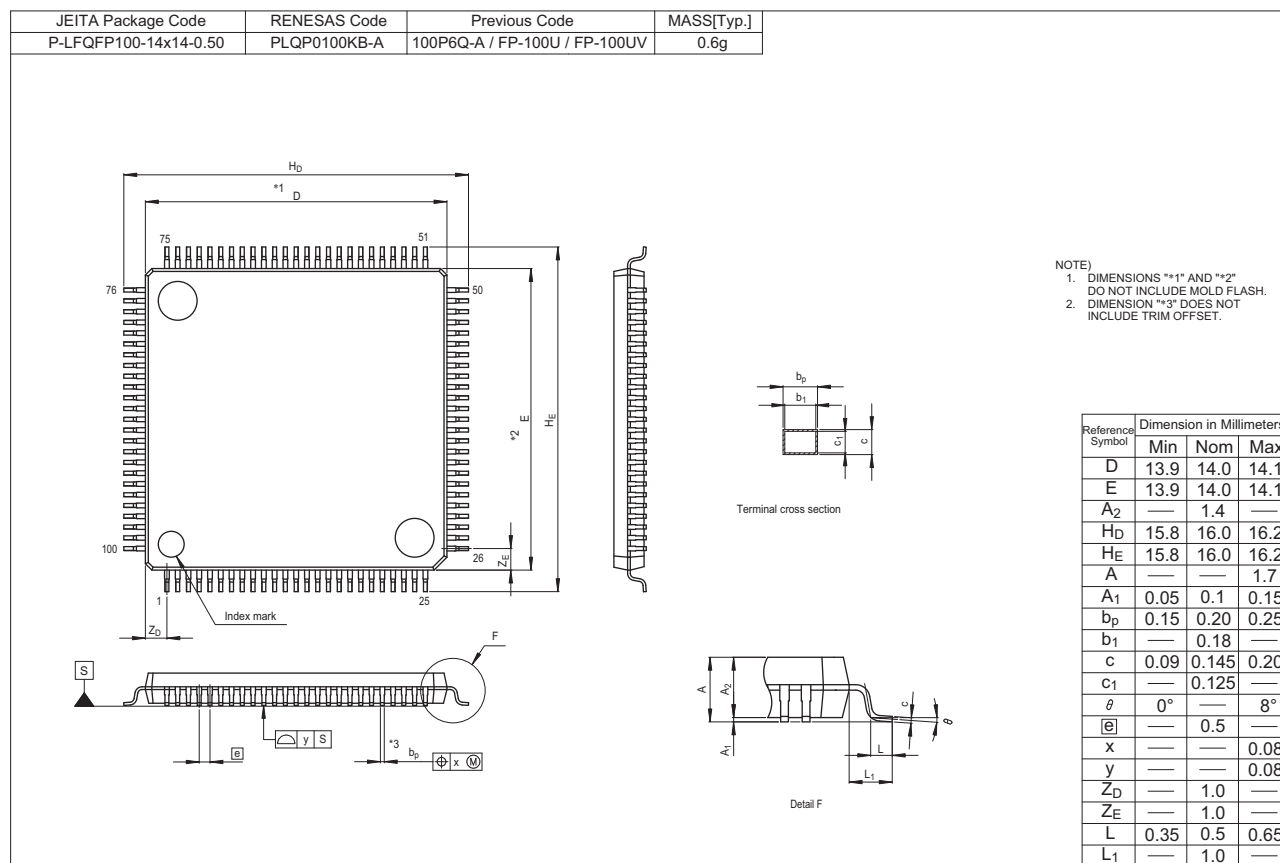


Figure A 100-Pin LFQFP (PLQP0100KB-A)

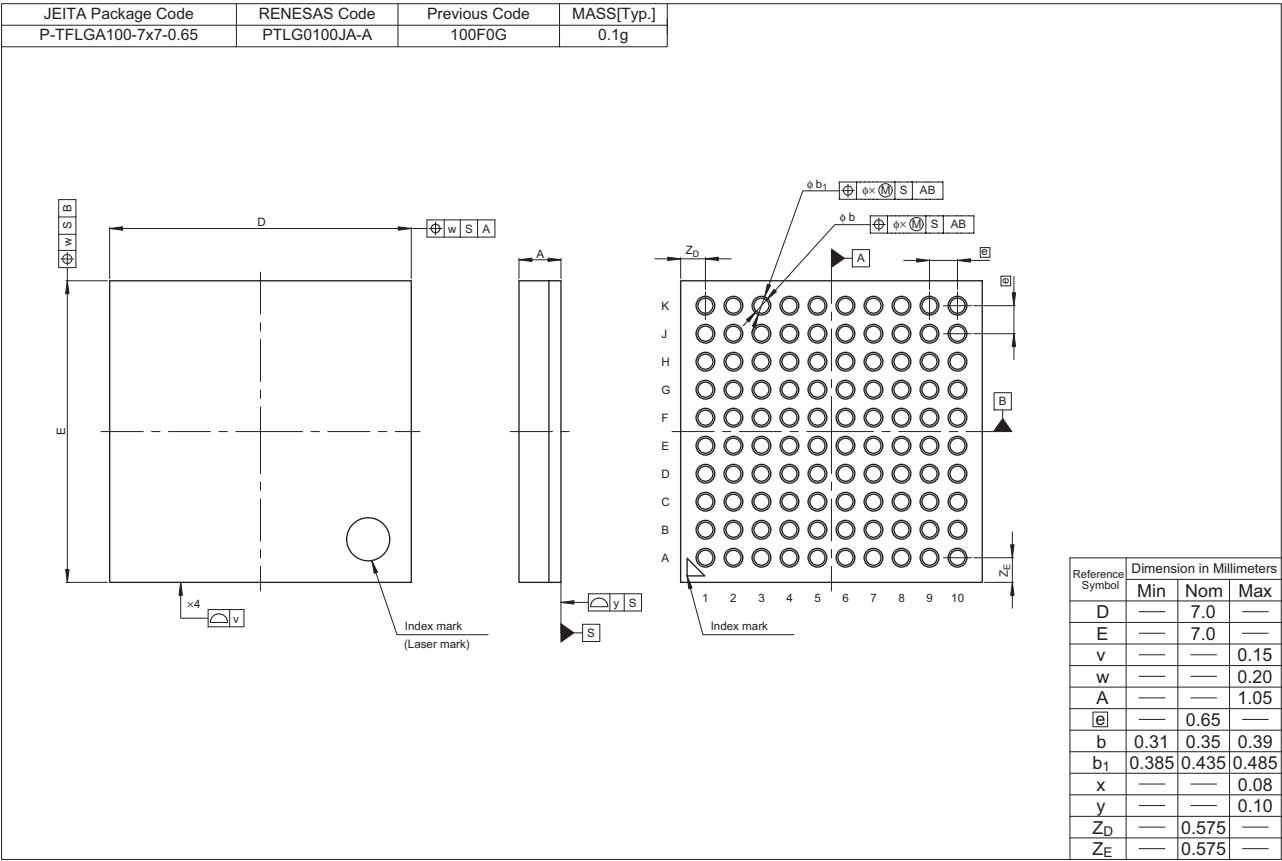


Figure B 100-Pin TFLGA (PTLG0100JA-A)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.