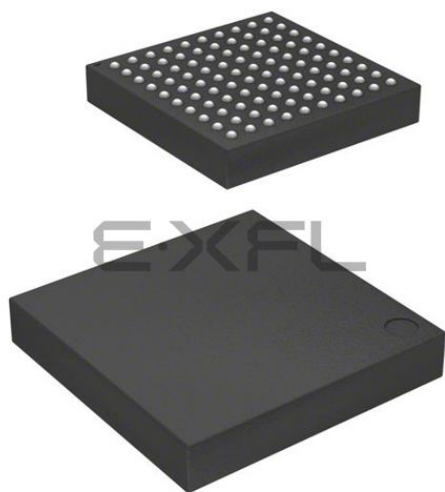




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Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51136adlj-2a

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIE, SCIF, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
36		P11	MTIC5U/POE0#	RXD12/RXD12/SMISO12/SSCL12/ RXD0/SMISO0/SSCL0	SEG02	IRQ7
37		P10	MTIC5V/POE1#	TXD12/TXD12/SIOX12/SMOSI12/SSDA12/TXD0/SMOSI0/SSDA0	SEG03	IRQ6
38		P56	MTIOC1A/MTIC5W/POE2#	TXD1/SMOSI1/SSDA1	SEG04	IRQ5
39		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
40		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
41		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
42		P50	MTIOC2A	MOSIA/TXD2/SMOSI2/SSDA2	SEG08	
43		P55	MTIOC4D/TMO3		VL1	
44		P54	MTIOC4B/TMCI1		VL2	
45		PC7	MTIOC3A/MTCLKB/TMO2	TXD1/SMOSI1/SSDA1/MISOA/TXD8/SMOSI8/SSDA8/USB0_OVRCURB	VL3	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD1/SMISO1/SSCL1/MOSIA/RXD8/SMISO8/SSCL8/USB0_EXICEN	VL4	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
48		PC4	MTIOC3D/MTCLKC/POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	
50		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/SSLA3	COM3	
51		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/COM4	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/COM5	
55		PB5	MTIOC1B/MTIOC2A/POE1#/TMRI1	SCK9/SSISCK0	SEG13/COM6	
56		PB4		CTS9#/RTS9#/SS9#	SEG14	
57		PB3	MTIOC0A/MTIOC3B/MTIOC4A/POE3#/TMO0	SCK6/AUDIO_MCLK/USB0_OVRCURA	SEG15/COM7	
58		PB2		CTS6#/RTS6#/SS6#	SEG16	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6/SSIWS0	SEG17	IRQ4
60	VCC					
61		PB0	MTIOC0C/MTIC5W/RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/SSCL6		IRQ2/ADTRG0#
62	VSS					
63		PA6	MTIC5V/MTCLKB/MTIOC2A/POE2#/TMCI3	CTS5#/RTS5#/SS5#/SDA0/MOSIA/RXD8/SMISO8/SSCL8		IRQ3
64		PA7		TXD8/SMOSI8/SSDA8	SEG18	
65		PA5		SCK8	SEG19	
66		PA4	MTIOC2B/MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/SSLA0/CTS8#/RTS8#/SS8#	SEG20	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTIOC1B/MTCLKD/POE0#	RXD5/SMISO5/SSCL5/IRRXD5/MISOA	SEG21	IRQ6/CMPB1

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3 ICLK
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0050h	SYSTEM	LCD Source Clock Control Register	LCDSCLKCR	8	8	3 ICLK
0008 0051h	SYSTEM	LCD Source Clock Control Register 2	LCDSCLKCR2	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (2/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 7018h	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 73AAh	ICU	Interrupt Source Priority Register 170	IPR170	8	8	2 ICLK
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK
0008 73E6h	ICU	Interrupt Source Priority Register 230	IPR230	8	8	2 ICLK
0008 73EAh	ICU	Interrupt Source Priority Register 234	IPR234	8	8	2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242	IPR242	8	8	2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243	IPR243	8	8	2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK
0008 73F5h	ICU	Interrupt Source Priority Register 245	IPR245	8	8	2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (19/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB
0008 C1BEh	MPC	PF6 Pin Function Control Register	PF6PFS	8	8	2 or 3 PCLKB
0008 C1BFh	MPC	PF7 Pin Function Control Register	PF7PFS	8	8	2 or 3 PCLKB
0008 C1D0h	MPC	PJ0 Pin Function Control Register	PJ0PFS	8	8	2 or 3 PCLKB
0008 C1D2h	MPC	PJ2 Pin Function Control Register	PJ2PFS	8	8	2 or 3 PCLKB
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)Conditions: $2.7\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	$\text{VCC} \times 0.7$	—	5.8	V
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)	V_{IH}	$\text{VCC} \times 0.8$	—	5.8	
	Ports P02, P04, P07, ports P10 to P15, ports P20 to P27, ports P30 to P32, P35, ports P50 to P56, ports PA0 to PA5, PA7, ports PB1 to PB7, ports PC0 to PC7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7, port PH7, ports PJ0*1, PJ2*1, PJ3, RES#	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	
	RIIC input pin (except for SMBus)	V_{IL}	-0.3	—	$\text{VCC} \times 0.3$	
	Other than RIIC input pin	V_{IL}	-0.3	—	$\text{VCC} \times 0.2$	
	RIIC input pin (except for SMBus)	$\Delta\text{V}_{\text{T}}$	$\text{VCC} \times 0.05$	—	—	
	Other than RIIC input pin	$\Delta\text{V}_{\text{T}}$	$\text{VCC} \times 0.1$	—	—	
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$\text{VCC} \times 0.9$	—	$\text{VCC} + 0.3$	V
	XTAL (external clock input)	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	V_{IH}	$\text{AVCC0} \times 0.7$	—	$\text{AVCC0} + 0.3$	
	RIIC input pin (SMBus)	V_{IH}	2.1	—	$\text{VCC} + 0.3$	
	MD	V_{IL}	-0.3	—	$\text{VCC} \times 0.1$	
	XTAL (external clock input)	V_{IL}	-0.3	—	$\text{VCC} \times 0.2$	
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	V_{IL}	-0.3	—	$\text{AVCC0} \times 0.3$	
	RIIC input pin (SMBus)	V_{IL}	-0.3	—	0.8	

Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports PJ0 and PJ2 multiplexed with DA0 and DA1 as general I/O ports, make sure that $\text{VCC} \leq \text{AVCC0}$.

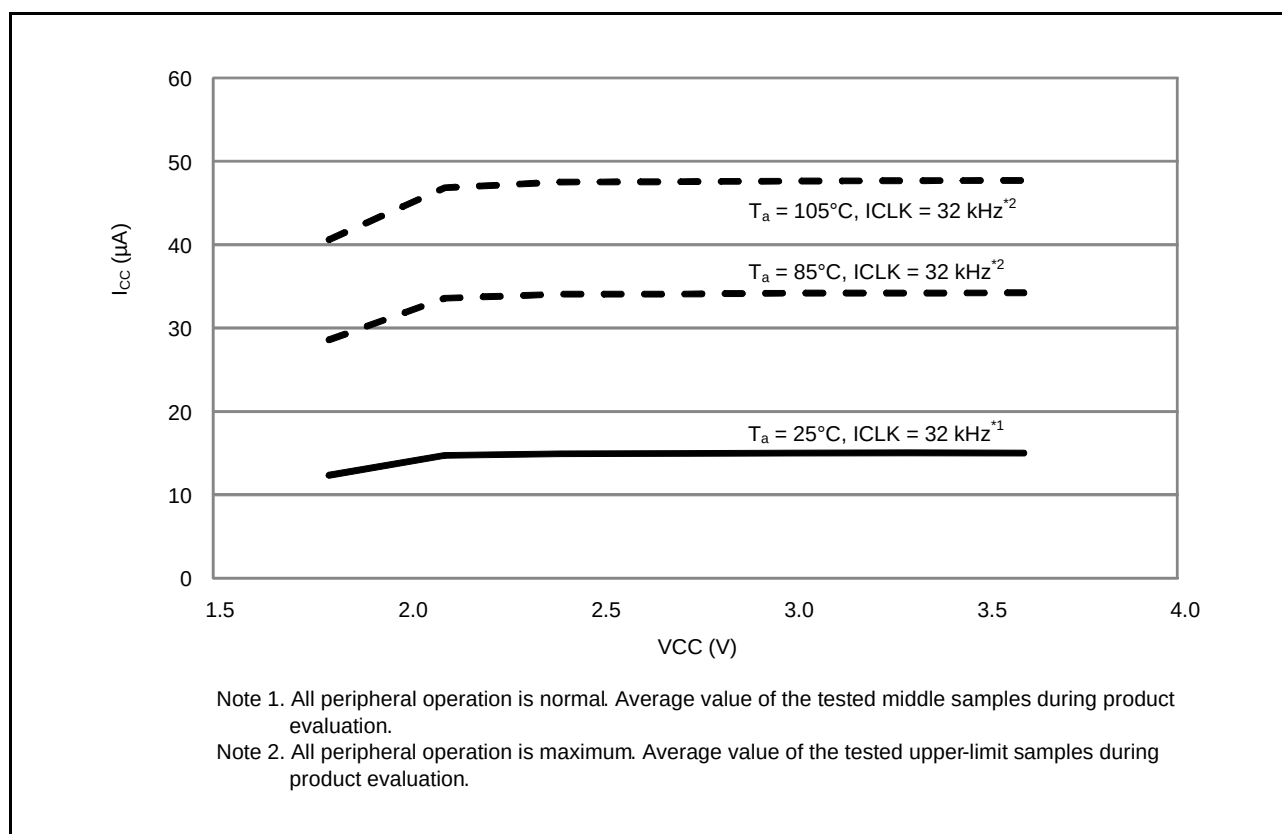


Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 5.8 DC Characteristics (6)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T _a = 25°C	I _{CC}	0.44	0.98	μA	
		T _a = 55°C		0.80	3.47		
		T _a = 85°C		2.7	12.0		
		T _a = 105°C		6.17	42.7		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for LPT operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT dedicated on-chip oscillator
	Increment for IWDT operation			0.37	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDT and LVD are stopped.

Note 3. $\text{VCC} = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.

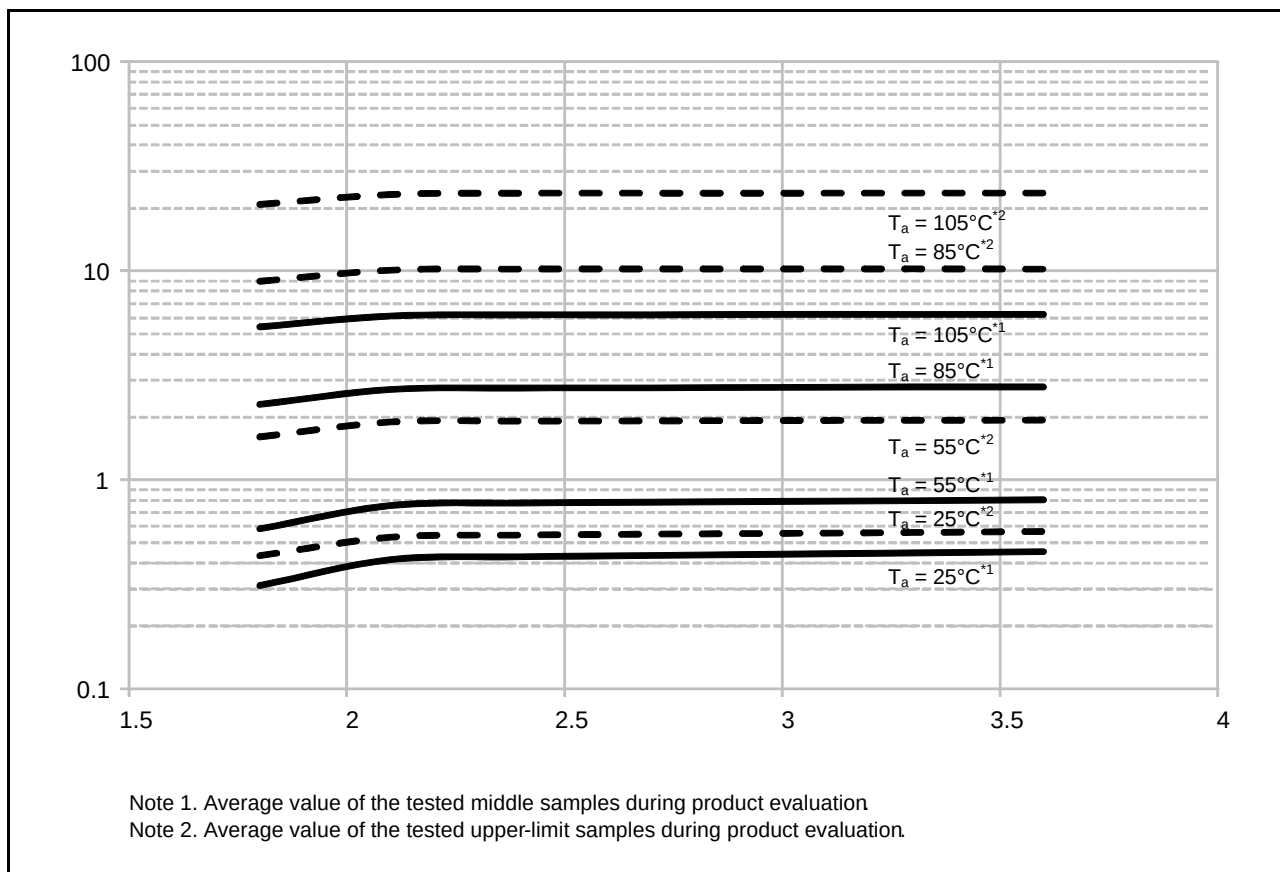


Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)

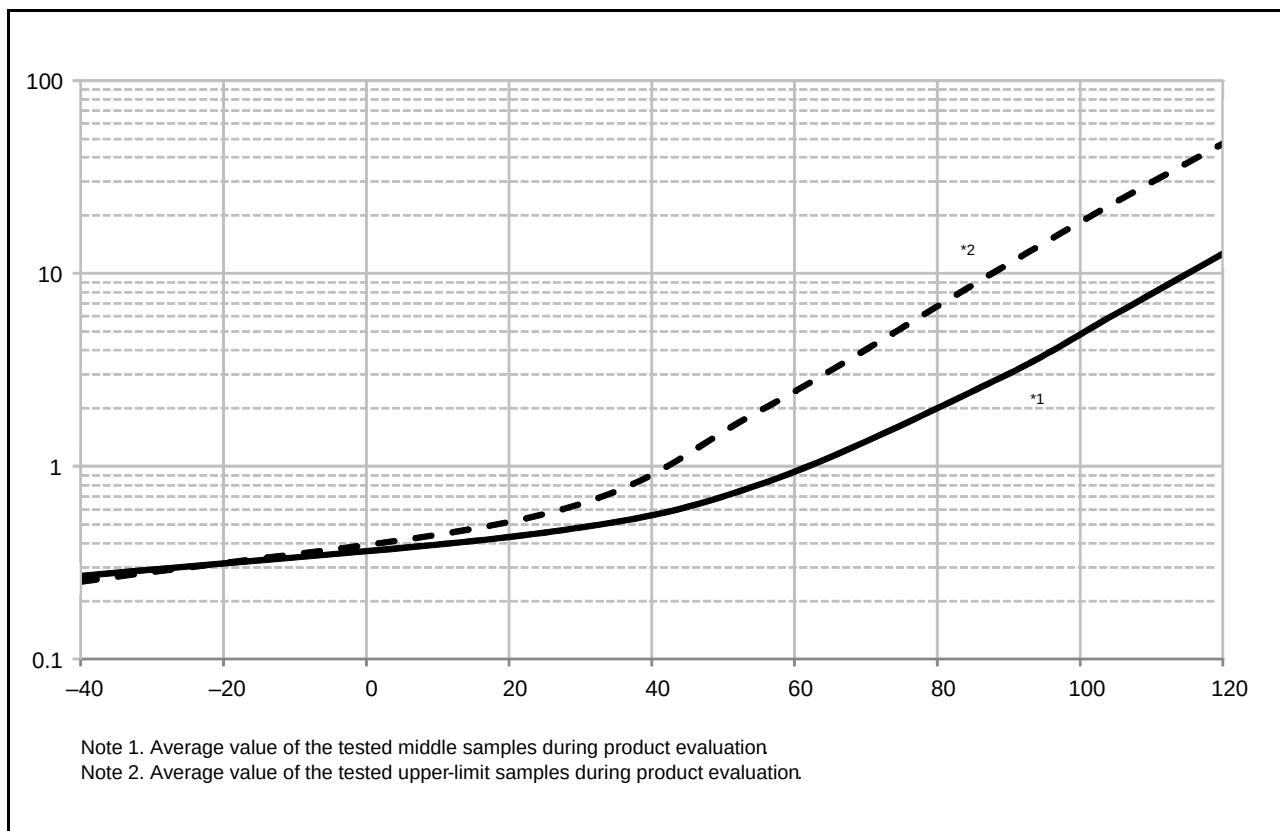


Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.16 Permissible Output Currents (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$ (G version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	ΣI_{OL}	1.6	
	Total of ports P02, P04, P07, P20 to P27, P30, P31, PJ0, PJ2, PJ3		20	
	Total of ports P10 to P17, port P32, ports P50 to P56, ports PB0 to PB7, ports PC0 to PC7		20	
	Total of ports PA0 to PA7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7		20	
	Total of all output pins		40	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	I_{OH}	-0.1	
	Ports other than above		-4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		-0.1	
	Ports other than above		-4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7	ΣI_{OH}	-0.6	
	Total of ports P02, P04, P07, P20 to P27, P30, P31, PJ0, PJ2, PJ3		-10	
	Total of ports P10 to P17, port P32, ports P50 to P56, ports PB0 to PB7, ports PC0 to PC7		-15	
	Total of ports PA0 to PA7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7		-15	
	Total of all output pins		-40	

Note: Do not exceed the permissible total supply current.

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.11 to Figure 5.13 show the characteristics of the RIIC output pin.

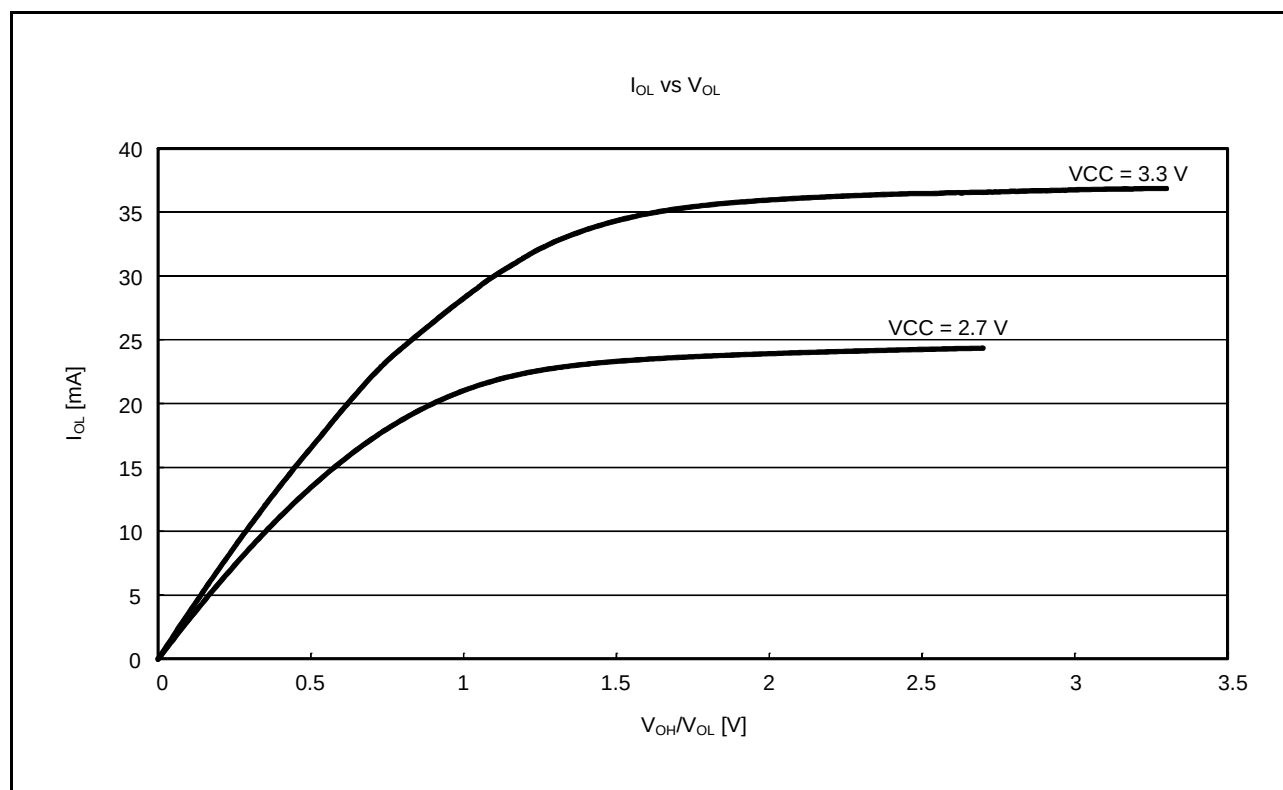


Figure 5.11 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

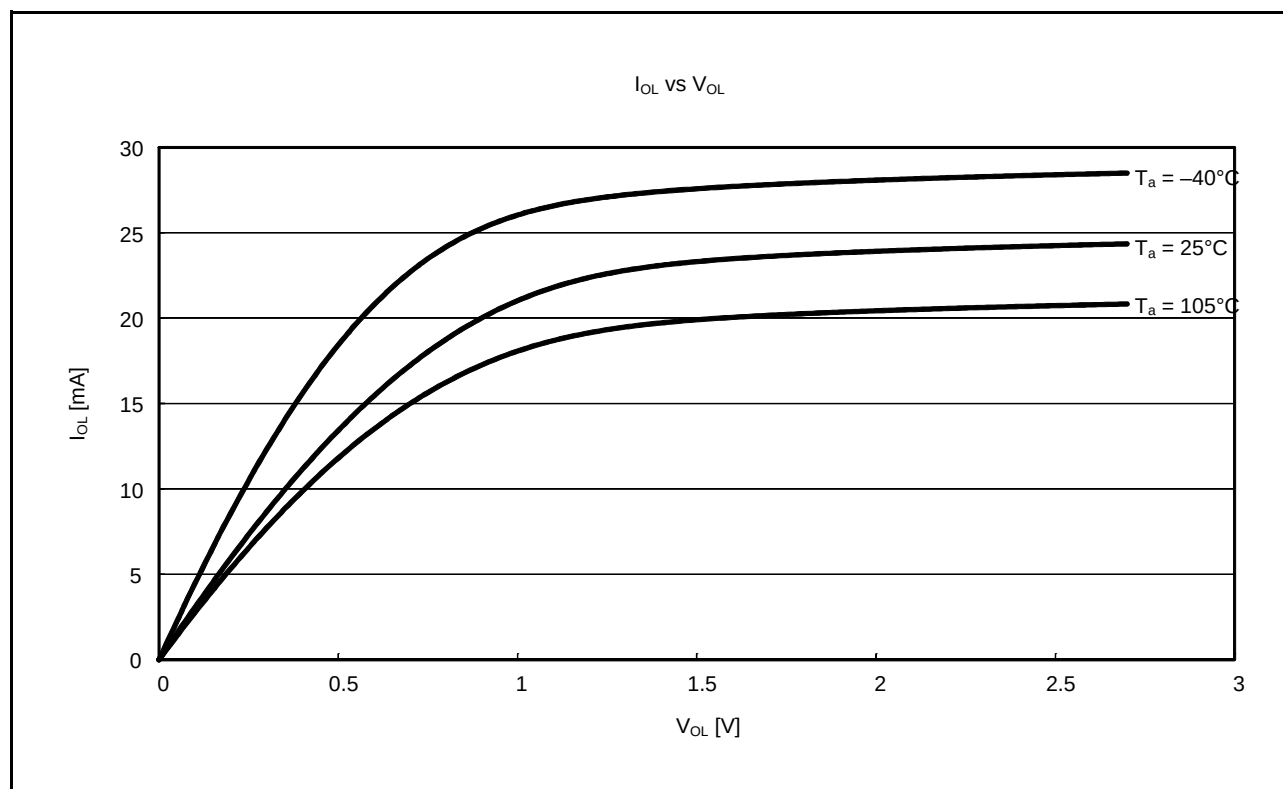


Figure 5.12 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.19 Operation Frequency Value (High-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)*3		8	16	32	32	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.20 Operation Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$.

Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.21 Operation Frequency Value (Low-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f _{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.

Note 2. The A/D converter cannot be used.

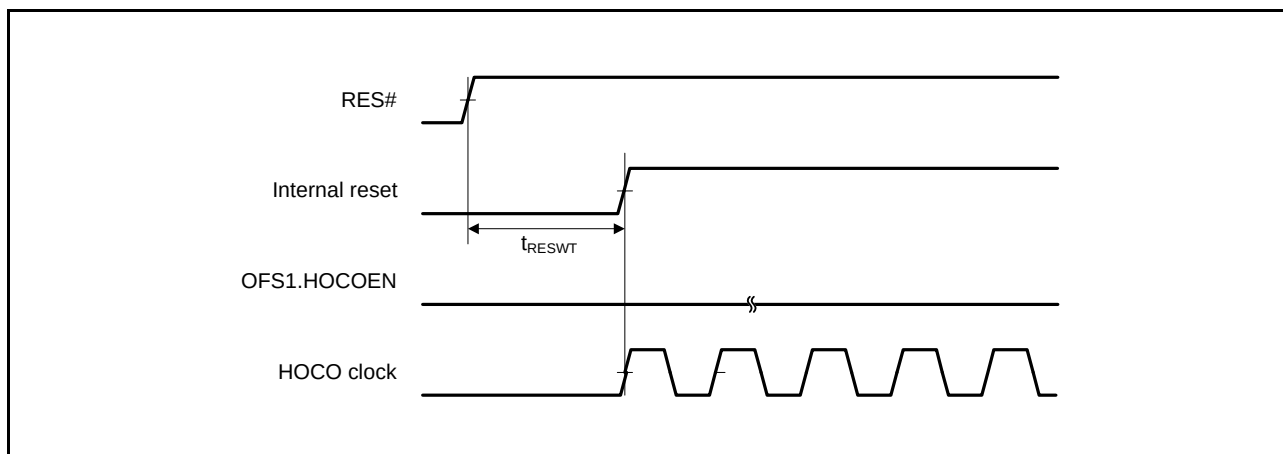


Figure 5.22 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

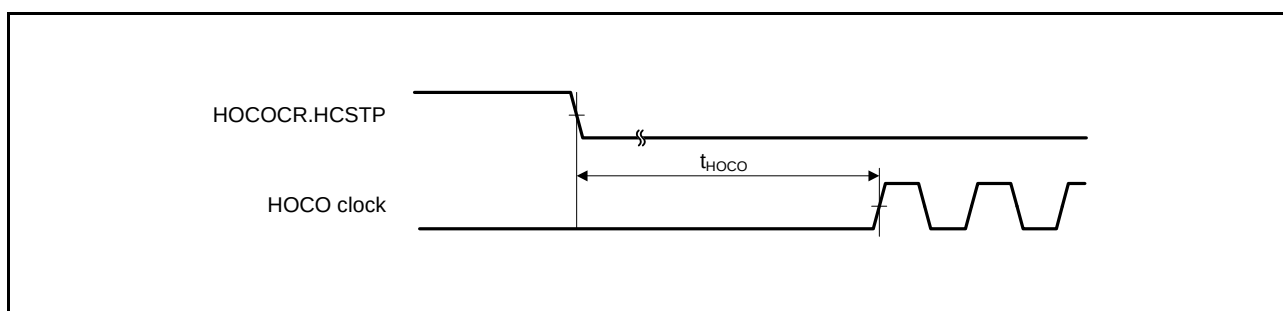


Figure 5.23 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

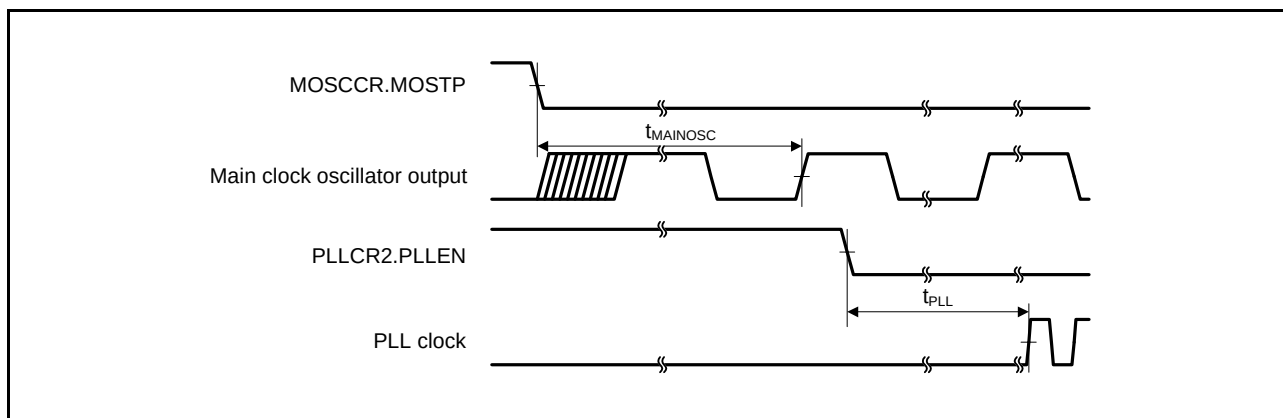


Figure 5.24 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

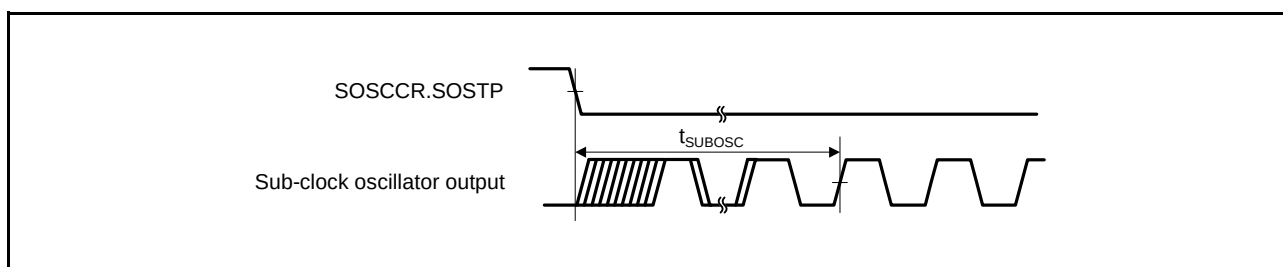


Figure 5.25 Sub-Clock Oscillation Start Timing

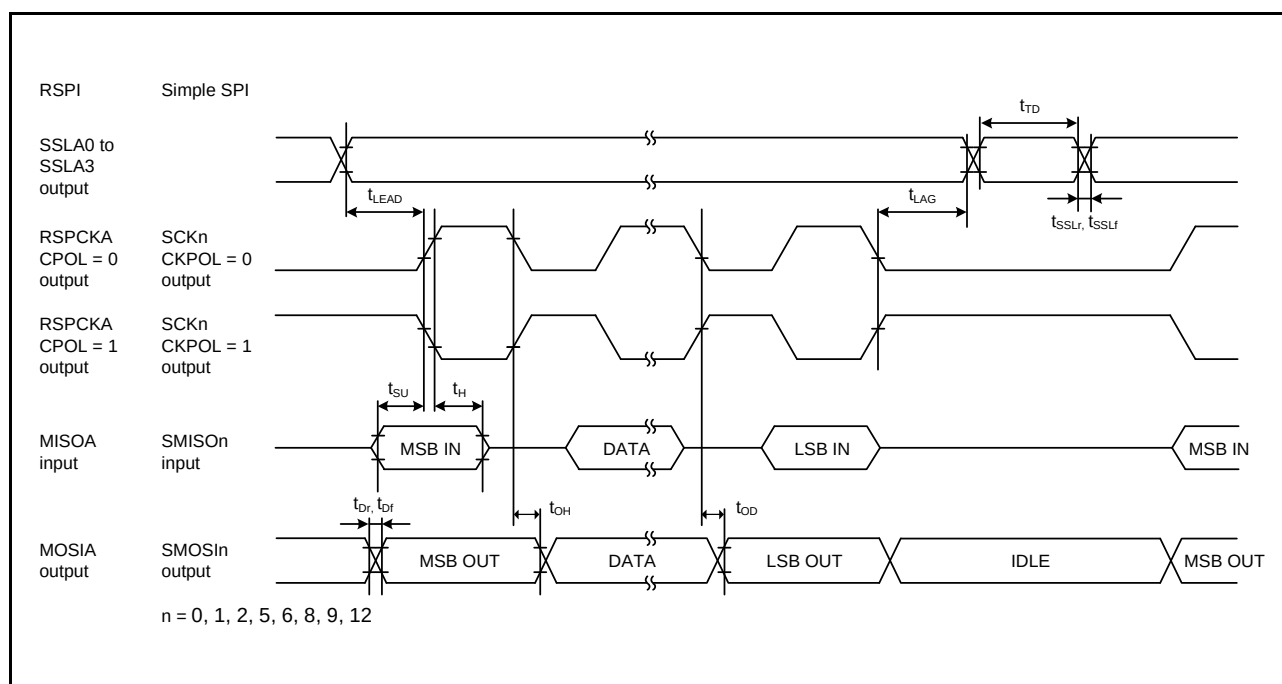


Figure 5.43 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

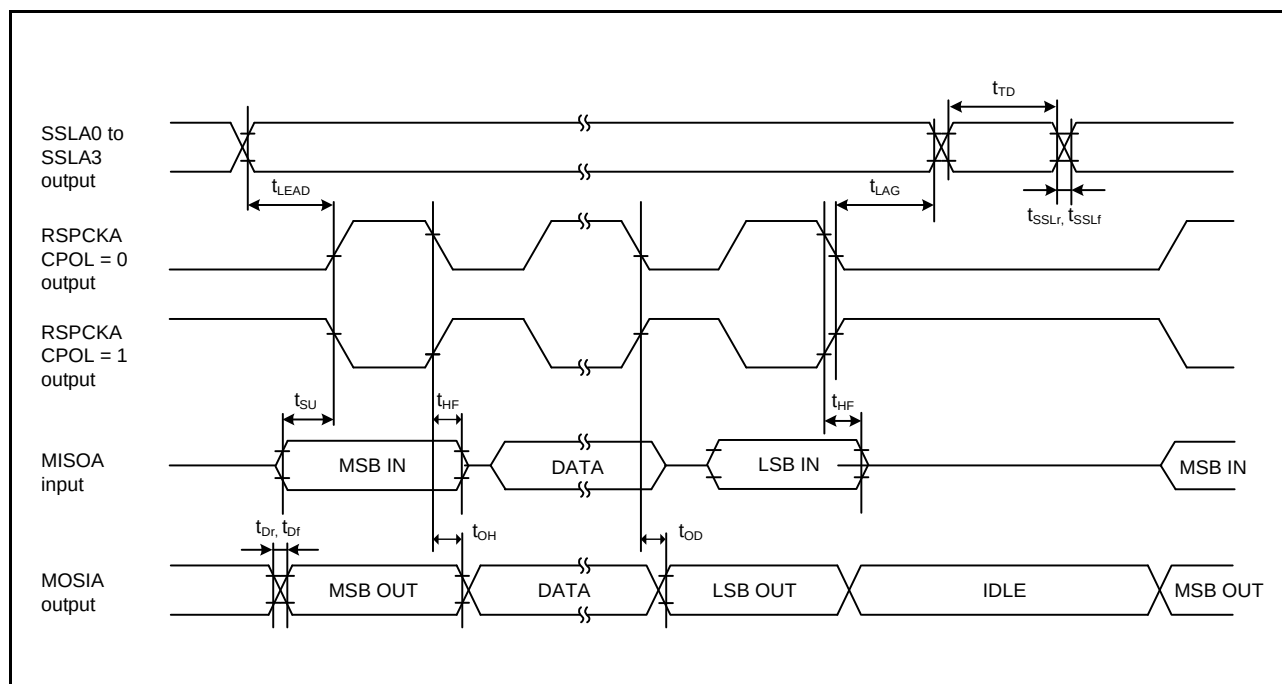


Figure 5.44 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

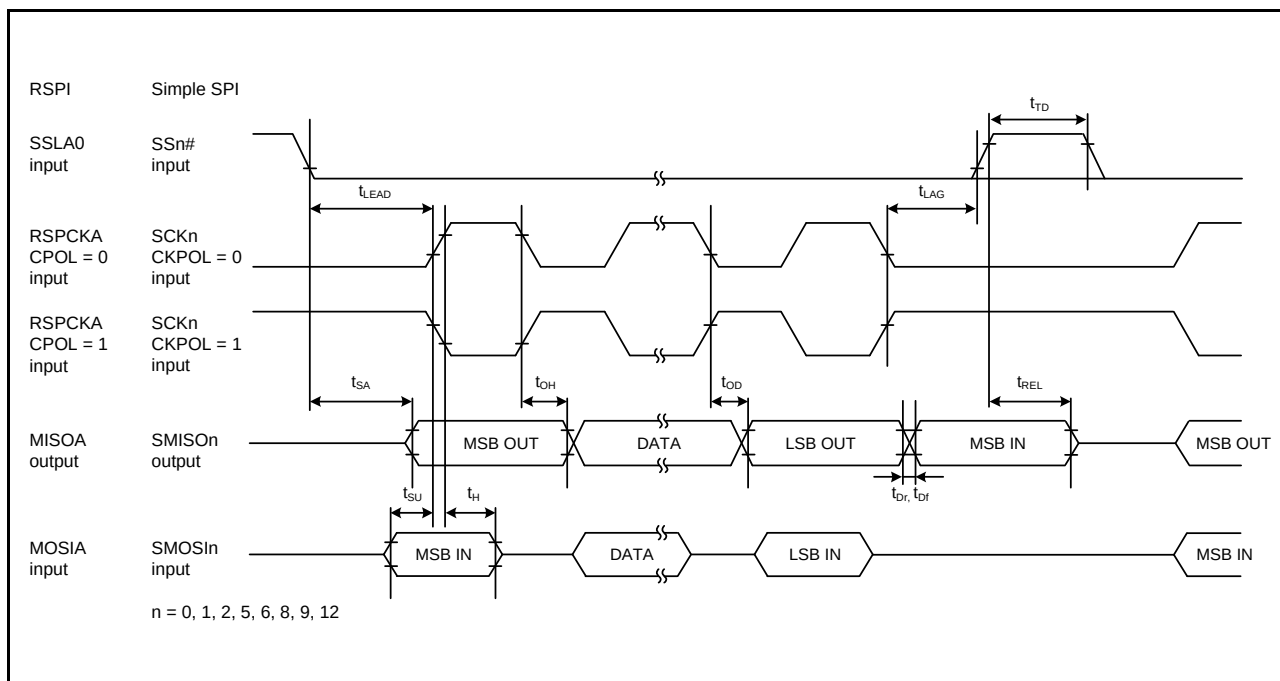


Figure 5.47 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

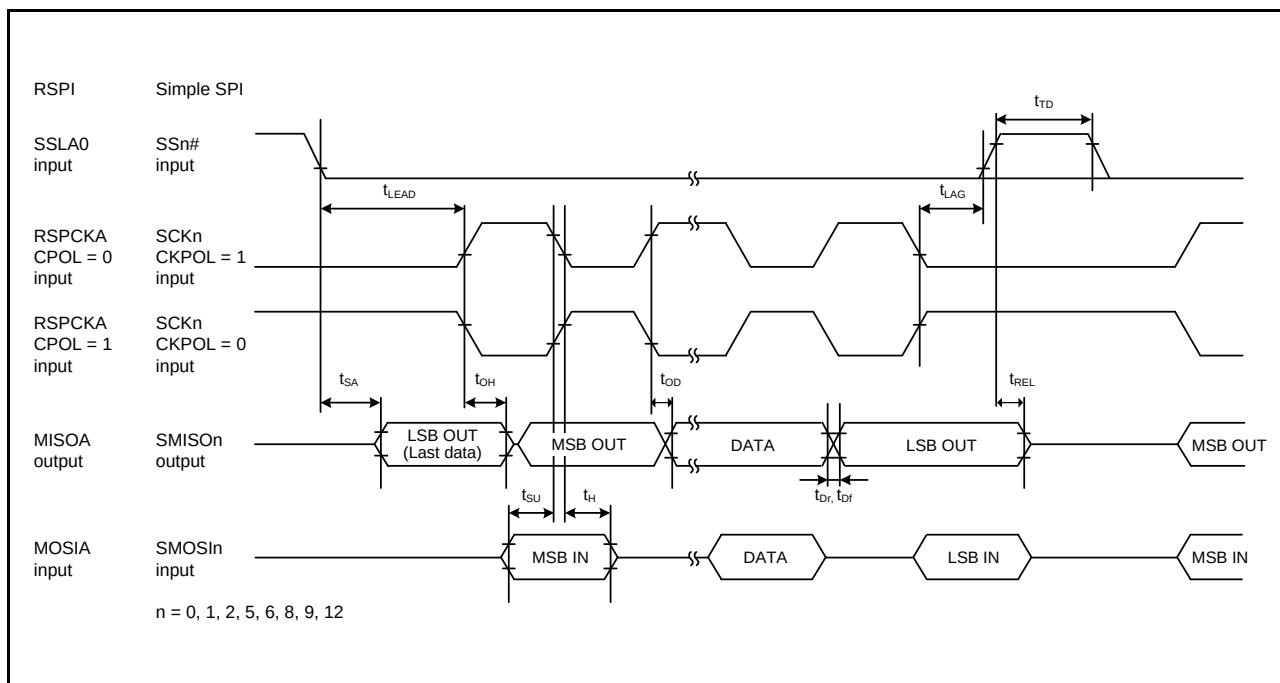


Figure 5.48 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

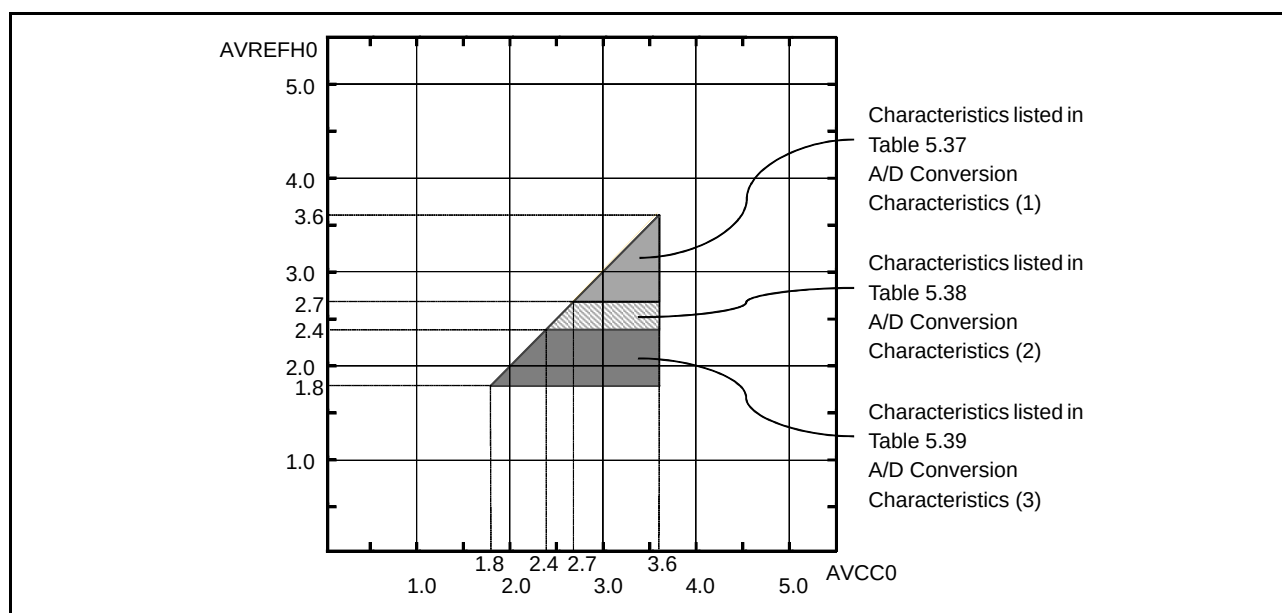


Figure 5.56 AVCC0 to AVREFH0 Voltage Range

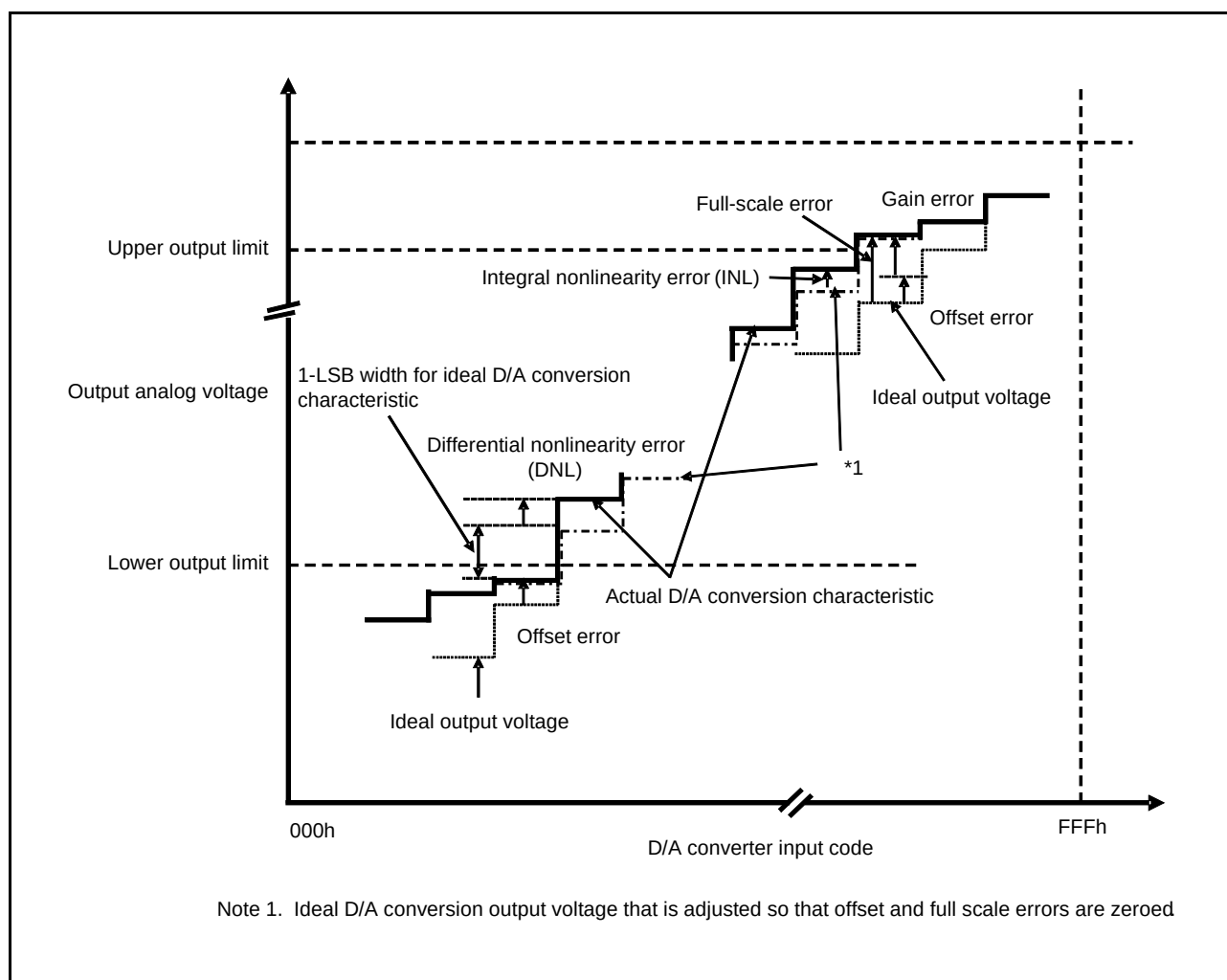


Figure 5.58 Illustration of D/A Converter Characteristic Terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

5.9.3 Capacitor Split Method

Table 5.54 Capacitor Split Method

Conditions: $2.2\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.2\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected between CAPH and CAPL pins	C1	0.33	0.47	0.61	μF	
External capacitor connected to V_{L1} pin	C2	0.33	0.47	0.61	μF	
External capacitor connected to V_{L2} pin	C3	0.33	0.47	0.61	μF	
External capacitor connected to V_{L3} pin	C4	0.33	0.47	0.61	μF	
External capacitor connected to V_{L4} pin	C5	0.33	0.47	0.61	μF	

(1) 1/3 Bias Method

Table 5.55 Capacitor Split Method LCD Characteristics

Conditions: $2.2\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.2\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Conditions
V_{L4} voltage*1	V_{L4}	C1 to C4 connected	—	VCC	—	V	
V_{L2} voltage*1	V_{L2}	C1 to C4 connected	$2/3\text{V}_{\text{L4}} - 0.07$	$2/3\text{V}_{\text{L4}}$	$2/3\text{V}_{\text{L4}} + 0.07$	V	
V_{L1} voltage**1	V_{L1}	C1 to C4 connected	$1/3\text{V}_{\text{L4}} - 0.08$	$2/3\text{V}_{\text{L4}}$	$2/3\text{V}_{\text{L4}} + 0.08$	V	
Capacitor split wait time*1	t_{WAIT}		100	—	—	ms	

Note 1. This is the wait time from when voltage bucking is started ($\text{VLCON} = 1$) until display is enabled ($\text{LCDON} = 1$).

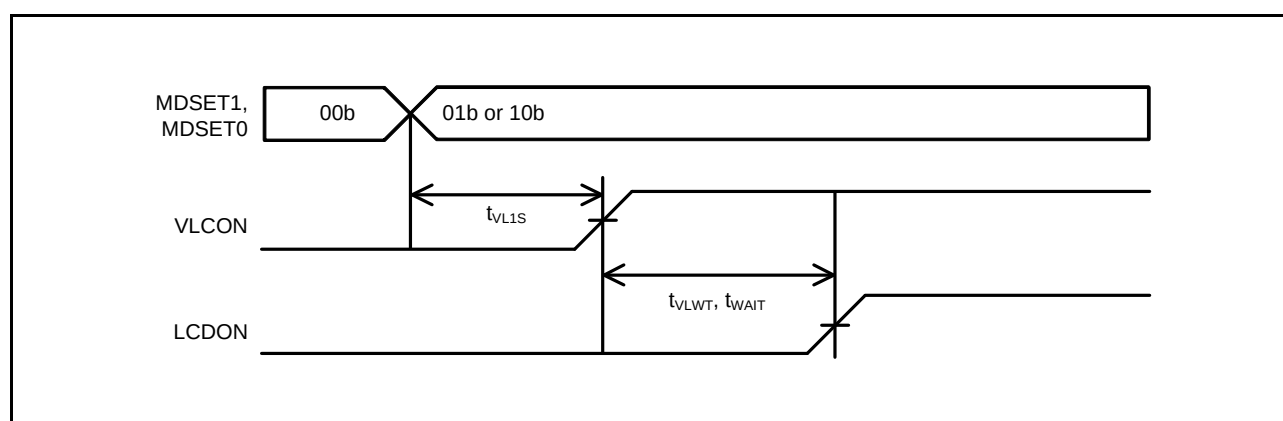


Figure 5.61 LCD Reference Voltage Setup Time, Voltage Boosting Wait Time, and Capacitor Split Wait Time

5.13 ROM (Flash Memory for Code Storage) Characteristics

Table 5.60 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erase cycle*1		N _{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N _{PEC}	t _{DRP}	20*2, *3	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.61 ROM (Flash Memory for Code Storage) Characteristics (2)

High-speed operating mode Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erase operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t _{P4}	—	103	931	—	52	489	μs
Erase time	1-Kbyte	t _{E1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t _{E256K}	—	407	925	—	39	457	ms
Blank check time	4-byte	t _{BC4}	—	—	48	—	—	15.9	μs
	1-Kbyte	t _{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t _{SED}	—	—	21.6	—	—	12.8	μs
Start-up area switching setting time		t _{SAS}	—	12.6	543	—	6.16	432	ms
Access window time		t _{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t _{DIS}	2	—	—	2	—	—	μs
ROM mode transition wait time 2		t _{MS}	5	—	—	5	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

REVISION HISTORY	RX113 Group Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.02	Dec 01, 2014	—	First edition, issued	
1.10	Mar 31, 2016	1. Overview		
		16 to 23	Table 1.5 to 1.7 Note 2 regarding I/O power source is AVCC0 for the ports (P4, P9, PJ6, and P7), added	
		5. Electrical Characteristics		
		53	Table 5.1 Absolute Maximum Ratings, Analog power supply voltage added	TN-RX*-A149A/E
		54	Table 5.2 Recommended Operating Conditions, VREFH0 / VREFH / AVCC0 / VREFL added	TN-RX*-A149A/E
		60	Table 5.8 DC Characteristics (6), Increment for LPT operation and Increment for IWDG operation added	TN-RX*-A149A/E
		62	Table 5.9 DC Characteristics (7) added	TN-RX*-A136A/E
		62, 63	Table 5.10 DC Characteristics (8), LDV1,2 and CTSU operating current added	TN-RX*-A149A/E
		65, 66	Table 5.15 Permissible Output Currents is divided into D version and G version	TN-RX*-A136A/E
		105	Table 5.43 D/A Conversion Characteristics (1), Output voltage range added	
		119	Table 5.61 ROM (Flash Memory for Code Storage) Characteristics (2), Erasure time - 256-Kbyte added	TN-RX*-A132A/E
		120	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (3), Temperature range for the programming/erasure operation changed and Erasure time - 256-Kbyte added	TN-RX*-A132A/E
		121	Table 5.64 E2 DataFlash Characteristics (2), Low speed FCLK changed and Erasure time - 8-Kbyte added	TN-RX*-A132A/E
		121	Table 5.65 E2 DataFlash Characteristics (3), Temperature range for the programming/erasure operation changed, Low speed FCLK changed and Erasure time - 8-Kbyte added	TN-RX*-A132A/E
		122 to 124	5.15 Usage Notes added	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.